11

CMOS-based DNA Sensor Arrays


Abstract
The invention of the transistor some 50 years ago, the subsequent realization of integrated circuits and today's availability of complete systems-on-a-chip have had an essential impact on today's way of life. The next revolution of similar impact may arise from developments in the area of biotechnology and life sciences. In this field, tools are required which can – in some cases only – be provided using techniques established by the semiconductor manufacturing world. Ongoing developments which intend to merge the know-how and potential of both disciplines, bio- and semiconductor technology, envision a way towards intelligent biosensor and actuator chips. In this chapter, CMOS-based DNA sensor chips with fully electronic readout are considered. The chapter is organized as follows. First, an introduction on basic DNA microarray techniques is given. Applications are briefly discussed and also the related technical requirements in terms of number of test sites, sensitivity, specificity and dynamic range. In Section 11.2, we address the motivation to develop electronic detection systems and the economic and technical boundary conditions for CMOS-based sensor arrays. A concrete example of a CMOS-based DNA sensor array is considered in detail in Section 11.3. There, after an introduction concerning the detection principle, CMOS process-related issues, architecture and circuit design issues, the interdependence of these areas in this nonstandard CMOS application and system aspects are discussed. A brief outlook towards label-free detection methods is given in Section 11.4 and finally, in Section 11.5, the chapter is summarized.

Keywords
DNA; sensor arrays; CMOS; DNA microarrays; DNA chips; redox-cycling detection.
11 Introduction

11.1 DNA Microarrays

The development of DNA microarray sensor chips in recent years has opened the way to high parallelism and high throughput in many biotechnology applications [1–9]. The most widely known fields are genome research and drug development; exploration of these tools in the field of medical diagnosis is under development. The purpose of DNA microarrays is to enable the parallel investigation of a given analyte concerning the presence of specific DNA sequences. Depending on the particular application, requirements range from relatively simple ‘presence or absence’ evaluations to quantitative analyses with a high dynamic range. In the following, the basic setup, the basic operation principle, the state-of-the-art optical readout method and application-driven specifications and requirements are briefly reviewed.
11.1.2  
**Basic Operation and Detection Principles**

A DNA microarray is a slide or a 'chip' typically made of glass or a polymer material [1–9]. Silicon is also used as carrier material, since the huge know-how on silicon manufacturing allows silicon-based chips to be obtained with specific advantageous properties [10–12]. Within an area of the order of square millimeters to square centimeters, single-stranded DNA receptor molecules are immobilized at predefined positions on such chips. These so-called probe molecules consist of different sequences of typically 20–40 bases. As depicted schematically in Fig. 11.1, these probe molecules can be deposited using microspotters [13, 14]. Today, such spotters are able to handle volumes in the sub-nanoliter range.

In Fig. 11.2a and b, two different sites within an array are considered after the immobilization phase. For simplicity, only five bases are drawn in this schematic illustration. As shown in Fig. 11.2c and d, in the next step the whole chip is flooded with an analyte containing the ligand or target molecules. Note that these molecules can be up to two orders of magnitude longer than the probe molecules. In case of complementary sequences of probe and target molecules, this match leads to hybridization (Fig. 11.2c). If probe and target molecules mismatch as shown in Fig. 11.2d, this chemical binding process does not occur. Finally, after a washing step, double-stranded DNA is obtained at the match positions (Fig. 11.2e) and single-stranded DNA (i.e. only the probe molecules as at the beginning of the whole procedure) remain at the mismatch sites.

Since the receptor molecules are known, the information whether double- or single-stranded DNA is found on the different test sites reveals the composition of the analyte. Hence the remaining demand is to make sites with double-stranded DNA visible. In the widely used state-of-the-art optics-based readout technique, the target molecules are labeled with fluorescence molecules before the analyte is applied to the chip. After hybridization and a subsequent washing step, the whole chip is illuminated or scanned with monochromatic light with a wave-

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**Fig. 11.1** Schematic plot showing a DNA microarray during the functionalization process. A microspotter deposits single-stranded DNA probe molecules (known DNA sequences) on the surface of the chip at predefined positions.
length matched to the absorption profile of the marker molecules (Fig. 11.3). A camera system with a blocking filter for the excitation wavelength takes an image of the array chip. Fluorescence light emitted at a considered position reveals successful hybridization and double-stranded DNA at this position.

We should mention that the spotting technique discussed here is only one of the methods to functionalize a microarray chip. In this case, the probe molecules

![Diagram](image.png)

**Fig. 11.2** (a), (b) Schematic consideration of two test sites after the immobilization process. For simplicity, probe molecules with five bases only are shown here. (c), (d) Hybridization phase. An analyte containing target molecules to be detected is applied to the whole chip. Hybridization occurs in the case of matching DNA strands (c). In the case of mismatching molecules (d) chemical binding does not occur. (e), (f) Situation after washing step

![Diagram](image.png)

**Fig. 11.3** State-of-the-art optical DNA microarray readout method (schematic plot). The target molecule is labeled with a fluorescence marker. The chip is illuminated with light of a defined wavelength $\lambda_1$. A camera system scans the whole chip or takes an image. The marker molecule which is only present at matching positions emits fluorescence light with a wavelength $\lambda_2 > \lambda_1$ which is detected by the camera system. Since the intensity of this light source is orders of magnitude lower compared with the stimulating light source, a filter with very good suppression characteristics at $\lambda_1$ is used to shield the camera system
are synthesized off-chip. This technique is adequate for low- and medium-density arrays with pitches of order 100 μm.

Using a lithography-based mask technique similar to that known from the semiconductor manufacturing world, in situ synthesis of the receptor molecules can be performed [15, 16]. There, the probe molecules are synthesized base-by-base on-chip. Ligation of a base at the strands under construction is triggered or blocked by the presence or absence of light at the respective sites. The required mask count is approximately equal to the number of different bases (cytosine, guanine, adenine, thymine) × length of the probe molecules. This optical technique, used by Affymetrix, is specifically advantageous if a large volume of high-density chips with a high or very high number of test sites (e.g. ≥100,000) is to be manufactured.

Febit has developed a system [17] where the light-triggered chemistry behind the in situ synthesis of the probes is similar to that of Affymetrix. The main difference compared with the Affymetrix approach is that no masks are required but illumination patterns are dynamically generated using a digital projector-based system.

The Nanogen principle allows one to move off-chip synthesized receptor molecules to their on-chip target position using a dielectrophoresis technique [18–20]. For this purpose, some logic CMOS circuitry is provided on the same chip to apply the required voltages at the sensor sites. Readout is based on optical detection.

Recently, Combimatrix has suggested a system for on-chip in situ synthesis applying electrical potentials to the test sites during the functionalization process [21, 22]. The required potentials are controlled by CMOS logic gates. Readout is done using an optical technique.

### 11.1.3 Applications and System Requirements

The goal of this section is roughly to define specifications and requirements for the different fields of DNA microarray application which must be considered during the configuration of a chip-based system. Two main application areas, gene expression profiling and genome-related investigations, are identified.

In case of gene expression chips [23–25], the change of cell metabolism functions is monitored after application of stress or drugs. The response of cell tissue is monitored using cDNA as the information-carrying species. The expression profiles achieved, for example, reveal whether cancer-suppressor genes are up- or down-regulated after a chemical compound is applied. Such applications require arrays with at least several hundred or even up to several thousand sites. Since the amount of regulation – or expression – is the main parameter of interest, quantitative analyses are necessary. The dynamic range should exceed 2.5 decades in most applications.

On the other hand, in the area of medical diagnosis, single nucleotide polymorphism (SNP) detection is of high interest [26–28]. SNPs, for example, determine the reaction of a patient’s metabolism after application of a certain drug. In
the future, SNP characterization may provide the doctor with the information on which drug and which dose of that drug should be applied. This scenario of individual personalized medication may significantly help to lower patients’ suffering, to lower adverse effects and to reduce costs. The cancer drug Herceptin is a first example where an SNP test has to be performed before application [29, 30].

Assuming probe molecules with 25 bases as an example, SNP detection platforms must be able to distinguish between a perfect match (where each of the 25 bases finds the complementary base at the correct position) from so-called weak mismatches (i.e. from hybridization events, where only 24 or 23 bases of probe and target molecule match) (see Fig. 11.4). The number of available target molecules is usually relatively high in such tests, since they are provided by a biochemical amplification process, the polymerase chain reaction (PCR) [31–35]. Hence the main requirement for such sensor arrays is high specificity, whereas high sensitivity or large dynamic range are of less importance. The number of sites required is typically between about 50 and a few hundred.

Finally, it should be emphasized that the use of DNA microarrays alone does not help to develop a new drug or to heal a patient. A DNA chip is only a tool which helps to provide us efficiently and at reasonable cost with a huge amount of valuable data. The sampled information, however, must be interpreted using the methods from the field of bioinformatics. Exploration of the full potential of microarrays therefore also depends on further progress in the already ongoing parallel development in both areas.
11.2 Electronic DNA Chips

11.2.1 Motivation

So far, DNA array chips based on optical readout techniques have been discussed. DNA sensor array chips with fully electronic readout promise several advantages over the optical type, since they allow easier handling by the user and avoid expensive optical setups comprising CCD cameras, lenses, etc. These properties have the potential to allow access to new fields of application and to new markets (e.g. diagnosis in hospitals and doctors' offices, point-of-care and outdoor applications, food control). On the other hand, today's status of development is less advanced compared with the optical platforms.

11.2.2 CMOS-based DNA Chips

11.2.2.1 Economical Boundary Conditions

There are numerous suggestions in the literature for electronic DNA sensors focusing on the realization of a few test sites per chip only. These approaches utilize a suitable biocompatible substrate material carrying the transducer elements. The electrical terminals of the electronic sensor(s) on-chip are connected to an off-chip read-out apparatus which provides and measures all necessary electronic signals to operate the chip. Due to the fact that such chips do not contain any active electronic device they will be referred to as ‘passive chips’ in the following.

This is the most cost-effective concept as long as only few sites per investigation are required so that the amount of interconnects to the external read-out apparatus is not too high. Although a CMOS chip would help to further enhance the sensor signal(s) on-chip, there is no mandatory need for this measure in most applications. The costs of a CMOS chip are usually considered to be too high in these low-density applications to compete with passive, low-cost, test stripe-like electronic systems.

With increasing number of test sites per chip, an interconnect problem arises for passive chip-based approaches. The large number of interconnects needed to contact a medium-density passive chip lowers the available area per contact pad on-chip. As a consequence, reliability and yield decrease. Since the total area of such chips is limited, the available area and thus the signal strength per sensor also decrease. The lowered interconnect reliability at decreasing signal strengths finally leads to a complete loss of signal integrity. In this case ‘active chips’ (with active on-chip circuitry) are required, to amplify and process the weak sensor signals on-chip, i.e. in the direct neighborhood where the sensor signals are generated. Moreover, adequate on-chip circuitry allows operation of large microarray chips with a small number of contact pads independent of the numbers of test sites per chip.
Note that in this case higher costs per chip are not only acceptable owing to occurrence of a technical brick wall, but that another metric must be considered here: Whereas the costs per chip are increasing, the costs per data point decrease. Consequently, in the case of applications where a number of data points of the order of 100 or higher is required, active CMOS-based sensor array chips represent the technically and economically better choice compared with their passive counterparts.

A summary of these arguments is given in Tab. 11.1.

### Tab. 11.1 Economic aspects and technical boundary conditions of passive and active DNA sensor arrays

<table>
<thead>
<tr>
<th></th>
<th>Passive electronic DNA chips (only electronic transducer elements + interconnect lines on chip)</th>
<th>Active electronic DNA chips (electronic transducer elements + active on-chip circuitry for signal pre-processing, electronic multiplexing, ...)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>Low</td>
<td>Medium–high</td>
</tr>
<tr>
<td>Test sites per chip</td>
<td>~10</td>
<td>≥100</td>
</tr>
<tr>
<td>Costs per chip</td>
<td>Low</td>
<td>Increased processing costs:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- CMOS processing costs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Process to provide transducer elements must be compatible with CMOS process</td>
</tr>
<tr>
<td>Cost per data point</td>
<td>Approximately constant</td>
<td>Decrease with:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Increasing number of test sites per chip</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Increasing number of required data points per investigation</td>
</tr>
<tr>
<td>Electrical performance</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td>Electronic signal integrity</td>
<td>- Limited robustness</td>
<td>- By far increased robustness</td>
</tr>
<tr>
<td></td>
<td>- Loss of signal integrity at high test site count per chip</td>
<td>- Independent of number of test sites per chip</td>
</tr>
</tbody>
</table>

Note that in this case higher costs per chip are not only acceptable owing to occurrence of a technical brick wall, but that another metric must be considered here: Whereas the costs per chip are increasing, the costs per data point decrease. Consequently, in the case of applications where a number of data points of the order of 100 or higher is required, active CMOS-based sensor array chips represent the technically and economically better choice compared with their passive counterparts.

A summary of these arguments is given in Tab. 11.1.

#### 11.2.2.2 Technical Boundary Conditions

The realization of active electronic biosensor arrays requires the integration of bio-compatible interface, sensor and transducer materials into standard CMOS environments [36–40]. The chips have to be equipped with a passivation, which allows them to be operated in contact with wet media. Moreover, the material used to realize the transducer must be provided. Unfortunately, the materials available in standard CMOS lines are often not suitable to fulfill all biological and chemical requirements. In the case of sensor arrays based on electrochemical principles, the transducer material is usually a noble metal, in many cases gold. Gold, however, and other noble metals are not part of standard CMOS production lines. In-
tegration of these materials in a CMOS production line is crucial, since they may lead to contamination problems which have a significant impact on the performance of the CMOS devices and on the yield.

A reasonable concept to deal with this challenge is to fabricate CMOS wafers using the full standard CMOS process without any extra steps up to standard passivation. Standard or slightly modified Si$_3$N$_4$ passivations from CMOS production lines often meet the biological requirements, i.e., they are suitable to shelter the chip from the wet media which are to be analyzed. The specific transducer materials are then provided in a post-CMOS process implemented outside the CMOS production line.

In addition to the already discussed wafer- and chip-related manufacturing aspects, innovative packaging solutions are needed which differ from standard concepts used in the semiconductor world. The total sensor area, i.e., the area with the fluid interface, must be isolated from the region with pads used to contact the chip electrically. Moreover, the package must provide an electronic and a fluidic interface to the readout apparatus.

A further condition for robust and reliable operation of chips with a large number of positions is to provide array-compatible high-precision analog circuitry. The challenges usually arise from relatively low signals to be pre-processed within a given area per sensor site at sufficient dynamic range. Control logic and digital circuitry are also needed on-chip, but the total area consumption and design challenges of the pure digital parts are relatively low.

11.3 CMOS-based DNA Sensor Array Using a Redox-cycling Detection Technique

In this section, concrete development steps of a fully electronic CMOS-based DNA microarray platform are described. Starting with the detection principle used, experimental data concerning the extended CMOS process, circuit design issues, DNA experiments and system integration aspects are discussed.

11.3.1 Detection Principle

The electrochemical sensor principle used is shown schematically in Fig. 11.5. It is based on an electrochemical redox-cycling technique [41–45]. A single sensor (Fig. 11.5, left) consists of interdigitated gold electrodes (generator and collector electrode). Probe molecules are spotted and immobilized on the surface of the gold electrodes and chemical bonding is achieved by, e.g., thiol coupling. The target molecules in the analyte which is applied to the chip are tagged with an enzyme label (alkaline phosphatase). After the hybridization and washing phases, a suitable chemical substrate ($p$-aminophenyl phosphate) is applied to the chip. The enzyme label, available at the sites where hybridization occurred, cleaves the phosphate group and the electrochemically active $p$-aminophenol is generated (Fig. 11.5, right).
Applying simultaneously an oxidation and a reduction potential to the sensor electrodes ($V_{gen}$ and $V_{col}$ in Fig. 11.5, e.g. +300 and −100 mV with respect to the reference potential), $p$-aminophenol is oxidized to quinonimine at one electrode and quinonimine is reduced to $p$-aminophenol at the other. The activity of these electrochemically redox-active compounds translates into an electron current at the gold electrodes and the electronic measurement devices or circuits connected to the electrodes (symbolized by $I_{gen}$ and $I_{col}$ in Fig. 11.5).

This idealized schematic description of the redox-cycling process suggests a balanced charge situation at the two working electrodes. However, in reality not all particles oxidized at the generator reach the collector electrode. A measure for this phenomenon is the collection efficiency [44, 45]:

$$ce = \frac{I_{col}}{I_{gen}}$$

Measured data reveal values down to 80–90%. A potentiostat circuit, whose output and input are connected to a counter and to a reference electrode, respectively, provides the difference currents to the electrolyte. In particular, it forms a regulation loop which holds the potential of the electrolyte at a constant value. The complete four-electrode system is shown in Fig. 11.5 (left).
The current flow at the sensor electrodes is a function of the contribution initially generated by the enzyme label and of the redox-cycling related contribution at the sensor electrodes. These two mechanisms lead to a simple differential equation whose solution predicts an electrode current which increases in proportion to the measurement time (Fig. 11.6, top, curve A). With increasing concentration of \( p \)-aminophenol, saturation of the measurement currents occur due to diffusion effects in the analyte (Fig. 11.6, top, curve B). Owing to electrochemical artifacts, an offset current may also contribute to the detection current (Fig. 11.6, top, curve C). For this reason, as suggested in [41], often the derivatives of the sensor current with respect to the measurement time, \( \partial I_{\text{col}}/\partial t_{\text{meas}} \) and \( \partial I_{\text{gen}}/\partial t_{\text{meas}} \), are evaluated instead of the absolute values (Fig. 11.6, bottom, curve C).

### 11.3.2 Extended CMOS Process

In Fig. 11.7, the process used to provide the gold electrodes is schematically depicted [39]. We start on the basis of a 6 inch \( n \)-well CMOS process specifically optimized for analog applications (high-ohmic polysilicon resistors, poly–poly-capacitors). The minimum gate length is 0.5 \( \mu \)m, the oxide thickness is 15 nm and the supply voltage is 5 V.

The steps depicted in Fig. 11.7 show the process flow beginning at the point where processing of the standard CMOS flow is completed. The CMOS flow ends with encapsulation of the second aluminum layer by an oxide (\( \text{SiO}_2 \)), application of a chemical–mechanical planarization (CMP) step and nitride (\( \text{Si}_3\text{N}_4 \)) passivation (Fig. 11.7a). In the next step, via holes are etched down to the aluminum layer (Fig. 11.7b). A Ti/TiN barrier layer is deposited and the holes are filled with tungsten by a CVD process (Fig. 11.7c). The tungsten is etched back stopping at the barrier layer. The Ti/TiN layer at the surface of the wafer is also etched with an RIE process (Fig. 11.7d). Finally, the gold electrodes are fabricated in a lift-off process after evaporation of a Ti/Pt/Au stack with layer thicknesses of 50/50/300–500 nm each (Fig. 11.7e). Gold metallization is also used for the output pads.
Optionally, a compartment can be provided surrounding the sensor area of each test site (Fig. 11.7 f). In our case, it is made of polybenzoxazole (PBO) and processed as a resist, i.e. exposed, developed and baked. The purpose of this hydrophobic compartment is to avoid contamination of neighboring sensors during the spotting process. In particular, the need for processing the compartment depends on the specific spotting technique used [13, 14].

The SEM photograph in Fig. 11.8 shows the second aluminum layer from the CMOS process, via contact and sensor electrode. Fig. 11.9 shows a tilted SEM cross-section photograph with sensor finger electrodes and CMOS elements after the complete process run. (The nitride layer on top of the sensor electrodes is only used for preparation of the SEM photograph.) A top view of a sensor with interdigitated gold electrodes embedded within a PBO ring is depicted in Fig. 11.10. Width and spacing of the gold electrodes is 1 μm in all cases.

Fig. 11.11a shows a fully processed demonstrator chip with 128 (16×8) positions and Fig. 11.11b shows a blow-up of the sensor area of a fully processed demonstrator chip with 32 (8×4) positions.
11.3.3 Demonstrator Chip: Architecture and Circuit Design Issues

The architecture of the demonstrator chip depicted in Fig. 11.11a is shown in Fig. 11.12. Sensor site selection is done by column and row decoders and a multiplexer. A common potentiostat circuit is used for all sensor sites in parallel, measuring the potential of the electrolyte at its input (reference electrode) and driving a counter electrode at its output to keep the potential of the electrolyte at a prede-
fined voltage. Considering stability, this circuit is designed to be robust against the widely varying electrical properties of the electrolyte. Further detailed discussions on CMOS potentiostat circuits can be found elsewhere [46–49].

The potentials of the sensor electrodes of each sensor are controlled by the circuits located underneath the sensor sites (Fig. 11.13). In order to cover a wide band of possible applications, the circuit is designed to be operated with sensor currents from 1 pA to 100 nA. It consists of two regulation loops to control the potentials of both electrodes, whose currents are both recorded. They are amplified by a factor of 100 using two cascaded current mirrors in series within each branch.

The transfer characteristics of each pixel can optionally be calibrated. This is achieved by forcing reference currents into both branches of the circuit through tran-
11.3 CMOS-based DNA Sensor Array Using a Redox-cycling Detection Technique

Fig. 11.12 Chip architecture of a demonstrator chip with 16×8 sensor sites

Fig. 11.13 Sensor site circuit

Lines / Signals:
1: reference voltage generator electrode
2: reference voltage collector electrode
3: select output generator electrode
4: select output collector electrode
5: output current generator electrode
6: output current collector electrode
7: select calibration generator electrode
8: select calibration collector electrode
9: input calibration current generator electrode
10: input calibration current collector electrode
sisters Mn51 and Mp51 at the same nodes, where the sensor currents are applied \[38, 39, 50\] and measuring the circuit response (output current) for different operating points.

The variation of the transfer characteristics is determined by the variation of the current gain of the current mirrors (Mn11–Mn14, Mp11–Mp14, Mn31–Mn34, Mp31–Mp34). The variation of the current gain originates mainly from the variation of the transistor threshold voltage, \(V_t\), which can be modeled as \[51, 52\]

\[
\sigma(V_t) = \frac{A(V_t)}{\sqrt{W \times L}}
\]

where \(\sigma(V_t)\) is the transistor area (width \(W\)\times length \(L\))-dependent standard deviation of the threshold voltage and \(A(V_t)\) is the process-dependent threshold voltage related matching constant. For the considered process, \(A(V_t) = 14 \text{ mV} \text{ } \mu\text{m}\) holds for both n- and p-MOS transistors [53].

Owing to the very high dynamic range of five decades in current required here, the transistors of the current mirrors are operated in the subthreshold regime in most cases. In the subthreshold region, the transistor drain current, \(I_D\), can be modeled as

\[
I_D = I_0 \times \frac{W}{L} \times 10^{(V_G - V_t)/S}
\]

where \(I_0\) is a process and device type (n- or p-MOS)-dependent constant, \(V_G\) the transistor's gate voltage and \(S\) the transistor's subthreshold slope (a constant weakly dependent on the process and the device type).

Since the devices Mn13 and Mn14, Mp13 and Mp14, Mn33 and Mn34, and Mp33 and Mp34 only ensure that the devices Mn11 and Mn12, Mp11 and Mp12, Mn31 and Mn32, and Mp31 and Mp32 are operated at similar drain voltages, respectively, the main contribution to the mismatch of the current gain is provided by the latter group of devices.

Considering the collector electrode related part of the circuit as an example and using Equation (3) we can calculate the gain of the two current mirrors Mn11–Mn14 and Mp31–Mp34 in series:

\[
\frac{I_{out}}{I_{cal}} = \frac{W_{Mn12}}{W_{Mn11}} \times \frac{W_{Mp32}}{W_{Mp31}} \times 10^\left[\left(\Delta V_{t,Mn12,Mn11}/S_n\right) + \left(\Delta V_{t,Mp32,Mp31}/S_p\right)\right]
\]

The relative error of the gain of the two current mirrors is given by

\[
\frac{\Delta(I_{out}/I_{cal})}{I_{out}/I_{cal}} = 10^\left[\left(\Delta V_{t,Mn12,Mn11}/S_n\right) + \left(\Delta V_{t,Mp32,Mp31}/S_p\right)\right]
\]

where \(S_n\) and \(S_p\) are the n- and p-MOS transistor’s subthreshold slopes, \(\Delta V_{t,Mn12,Mn11}\) and \(\Delta V_{t,Mp32,Mp31}\) are the threshold voltage differences of devices Mn11 and Mn12 and Mp31 and Mp32, respectively. Length \(L\) is constant for all devices and parameter variations of \(L\) can be neglected.
An important output of Equations (4) and (5) is that the gain mismatch is independent of the transistors’ gate voltages. As a consequence, the gain error is constant independent of the sensor current/the circuit’s output current as long as the transistors in the current mirrors are operated in the subthreshold region.

Assuming that all current mirror transistors are operated under strong inversion conditions, which is given for sensor currents in the upper region,

\[ I_D = k \times \frac{W}{L} \times (V_G - V_t)^2 \]  

holds for the transistors’ drain currents, with \( k \) being a process and device type (n- or p-MOS)-dependent constant. On the basis of this relation, the gain of the two current mirrors is approximately given by

\[ \frac{I_{\text{out}}}{I_{\text{cal}}} = \frac{W_{Mn12}}{W_{Mn11}} \times \frac{W_{Mp32}}{W_{Mp31}} \times \left[ 1 - \frac{2 \times \Delta V_{t,Mn12,Mn11}}{V_{G,n} - V_{t,n}} - \frac{2 \times \Delta V_{t,Mp32,Mp32}}{V_{G,p} - V_{t,p}} \right] \]  

where \( V_{t,n} \) and \( V_{t,p} \) are the mean values of n- and p-MOS transistor threshold voltages, respectively. Since the denominator in the last two terms in brackets in Equation (7) is proportional to the square root of the transistor current (following Equation (6)), we can describe the relative error of the gain of the two current mirrors as

\[ \frac{\Delta (I_{\text{out}}/I_{\text{cal}})}{I_{\text{out}}/I_{\text{cal}}} = \frac{a}{\sqrt{I_{\text{cal}}}} \]  

with \( a \) being a process- and design-dependent constant.

On the basis of Equations (5) and (8), the gain error can be easily modeled for the whole operating range: In Fig. 11.14, the gain error is plotted schematically as a function of \( 1/\sqrt{I_{\text{cal}}} \). The behavior can be approximated by two straight lines: one in the inversion region increasing in proportion to \( 1/\sqrt{I_{\text{cal}}} \) and the other one in the subthreshold region with zero slope. In the weak inversion regime, i.e. where the transistors’ operation points change from strong inversion to the subthreshold region, a transition of the two lines into each other occurs.

Fig. 11.14  Schematic plot of the gain error as a function of \((\text{calibration current})^{-1/2}\) induced by parameter variations of the current mirror transistors of the circuit depicted in Fig. 11.13
These relations allow easy calibration of the circuit and of the whole array. Using two values for the calibration current the behavior in the inversion regime can be determined. These currents, labeled A and B in Fig. 11.14, must be chosen in the upper region of the range of specified sensor currents. In the subthreshold regime, one calibration data point (labeled C in Fig. 11.14) is sufficient. The value of this current may, for example, lie in the middle or in the lower half of the specified current window. Storing the measured output currents for these three calibration points for each test site, the whole array can be calibrated.

11.3.4

Process Optimization

Using the calibration option described above, the fabricated chips can also be electrically tested [38, 39, 50]. The chips are then operated without a fluid or biological material applied, but in the same electrical configuration as in the calibration mode. Here we use the option of pure electrical operation to evaluate the CMOS process properties.

Figs. 11.15 and 11.16 show the measured transfer characteristics and the gain as a function of the input current of all test sites from a 16×8 chip as shown in Figs. 11.11a and 12. Processing is performed as described in Section 11.3.2; PBO compartments are not processed here, characterization is done at wafer level. The plots reveal that for input currents below 10 pA a deviation of the gain is obtained compared with higher input currents. This effect coincides with a bending of the transfer characteristics in Fig. 11.15 in the region below 10 pA.

This artifact results from a degradation of the transistor properties compared with the pure CMOS process. Using charge-pumping characterizations [54, 55],
the interface state density \( N_{it} \) of the transistors is measured. For the pure CMOS process without extra process steps, a value of \( N_{it} = 1 \times 10^{10} \text{ cm}^{-2} \) is found for both p- and n-MOS transistors [39]. This is a reasonable value; values of the same order are found for most standard commercial CMOS processes. After gold processing, a more than 20-fold increase is measured (\( N_{it} > 2 \times 10^{11} \text{ cm}^{-2} \)). This excessive value translates into an increased, i.e. deteriorated, subthreshold slope \( S \) of the transistors, worsened off-state characteristics and thus to increased leakage currents. These increased leakage currents lead to the bending of the transfer characteristics in Figs. 11.15 and to the increase of the ratio of output and input current in Fig. 11.16. Consequently, this effect must not be interpreted as a true increase in the gain.

In standard CMOS processes, a forming gas (\( \text{N}_2, \text{H}_2 \)) anneal is applied to reduce damage at the MOS transistor interface. In order to avoid the effects described above, such an annealing step is also applied here after the gold process module. \( \text{N}_2/\text{H}_2 \) annealing is performed at different temperatures for 30 min. Characterization of the interface state density reveals an excellent value of \( N_{it} < 2 \times 10^9 \text{ cm}^{-2} \) after annealing at 400°C; 350°C annealing leads to slightly higher but still good values. As shown in Fig. 11.17, the decreased number of interface states turns into proper transfer characteristics.

We should also discuss the standard variations of transfer characteristics and gain at this point. The statistical variations in Figs. 11.15–11.17 are approximately independent of the input current between 1 pA and 1 nA; for higher currents a slight decrease is found. Comparing these measured data with analytically calculated values on the basis of Equations (2)–(8) using transistor matching parameters extracted for the pure CMOS process [53], very good agreement is found. For example, the standard variation of the measured gain for operating points in the subthreshold region amounts to \( \sim 20\% \); the calculated value is 18\%. We therefore conclude that the gold process does not influence this important analog device property.

Up to now, we have considered CMOS process front-end parameters in this section. However, the characteristics of the gold electrodes with and without annealing...
must also be investigated. Measured resistance data for gold and aluminum 2 lines and of the related via connections are given in Tab. 11.2. The data without an annealing step and with annealing at 350°C are similar for all parameters. With annealing at 400°C, a 20% increase in the gold resistance occurs. The SEM photographs in Fig. 11.18 reveal that this increase coincides with a rearrangement of grains within the gold layer. On the other hand, there is no change to the as-deposited Au stack up to 350°C annealing. Consequently, annealing at 350°C is chosen as a process window where both device and electrode properties are optimized.

Tab. 11.2 Resistances of gold and aluminum 2 lines and of the related via connections without and with annealing steps at different temperatures after the Au process

<table>
<thead>
<tr>
<th>Anneal (N₂/H₂)</th>
<th>Square resistance Au lines (mΩ/square)</th>
<th>Resistance via holes (0.8 x 0.8 μm) (mΩ)</th>
<th>Square resistance Al 2 lines (mΩ/square)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without</td>
<td>48</td>
<td>370</td>
<td>79</td>
</tr>
<tr>
<td>350°C, 30 min</td>
<td>51</td>
<td>360</td>
<td>76</td>
</tr>
<tr>
<td>400°C, 30 min</td>
<td>61</td>
<td>340</td>
<td>74</td>
</tr>
</tbody>
</table>

Fig. 11.17 Same plot as in Fig. 11.16, but with an N₂/H₂ annealing step after Au process at 350°C for 30 min

Fig. 11.18 SEM photographs showing the Au sensor electrodes without and with annealing steps at different temperatures after the Au process
11.3.5

**Measured Results**

In this section, results with biology applied to the chips are reported. We start with a simple oligo experiment. In this experiment, on one part of the sensor sites single-stranded DNA oligo molecules are immobilized which are exactly complementary to DNA oligo sequences in the analyte. On the other part of sensor sites, non-specific random sequences of probe DNA are immobilized. The experiment is performed at wafer level. The fluidic contact is provided via a flow cell positioned above the chip under test.

Two positions with matching strands and two positions with random sequences are considered. Since the absolute values of collector and generator current look very similar, only the collector current is shown in Fig. 11.19. As can be seen, match and mismatch clearly lead to different amounts of currents, but the offset currents (at $t_{\text{meas}} \approx 38$ s, where the dashed line is plotted) for the matching positions differ by a factor of 2 (see discussion in Section 11.3.1). Using the derivative $\partial I_{\text{col}}/\partial t_{\text{meas}}$ (Fig. 11.20), as discussed in [41], the data for the two matches and for the two mismatches are in very good agreement.

Further measurements with PCR products performed by project partners have demonstrated proper operation down to $10^{-13}$ mol.

11.3.6

**System Design Aspects**

11.3.6.1 **Extended System Architecture**

The results and achievements discussed above describe a demonstrator chip. This configuration is adequate to perform experiments from proof-of-principles towards...
benchmarking investigations with competitive approaches. Furthermore, the architecture shown in Fig. 11.12 allows one to study many further important properties of this CMOS-based approach and to collect a huge amount of information which is required to design a user-friendly prototype version.

The next generation of these chips will consist of the kernel described here and further on-chip peripheral circuits to increase functionality and to provide robust and easy applicability. For this purpose, analog signal processing will be completely kept on-chip thanks to the addition of reference circuits and analog-to-digital and digital-to-analog converters. The introduction of further control logic circuitry allows the chip to be operated with a pure digital interface. Moreover, the number of external interconnects will be reduced by this approach (e.g. down to six or eight) independent of the number of test sites per chip.

11.3.6.2 Alternative Circuit Design Approaches

Alternative circuit design and architecture approaches may be required if larger arrays are needed (e.g. with 1000 test sites or more). In this case, the sequential analog readout of each test site (e.g. using the circuit in Fig. 11.13) results in the fact that the data are sampled in different time intervals. Owing to the very low minimum currents to be monitored, the readout time interval per test site cannot fall below a given minimum value.

A concept which uses the same detection principle but circumvents this problem independent of the array size is described in the following [54]. CMOS process and sensor design are the same as above. The concept is based on the realization of a specifically adapted analog-to-digital converter within each sensor site. The realized sensor circuit consists of two complementary parts for the generator and collector electrodes. The principle is shown in Fig. 11.21. The voltage of the sensor electrode is controlled by a regulation loop via an operational amplifier and
transistor M1. For A/D conversion, a sawtooth generator concept is used, where an integrating capacitor C is charged by the sensor current. When the switching level of the comparator is reached, a reset pulse is generated and the capacitor is discharged by transistor M2 again.

Equation (9) describes the frequency behavior as a function of the sensor current including parasitic and device mismatch effects:

\[
\frac{1}{f} = \frac{(V_{\text{ref,comp}} + V_{\text{offset,comp}}) \times C}{I_{\text{electrode}} + I_{\text{leak}}} + t_{\text{delay}} \tag{9}
\]

where \(f\) is the oscillation frequency, \(V_{\text{ref,comp}}\) the comparator switching level, \(V_{\text{offset,comp}}\) the comparator input offset voltage, \(C\) the total capacitance (i.e. including parasitic capacitances), \(I_{\text{electrode}}\) the sensor electrode current, \(I_{\text{leak}}\) the leakage current (e.g. due to transistor junction leakage) at the circuit node connected to the comparator input (labeled with an asterisk in Fig. 11.21) and \(t_{\text{delay}}\) the comparator delay time. Equation (10) gives an approximation for the measured frequency:

\[
f \approx \frac{I_{\text{electrode}}}{(V_{\text{ref,comp}} \times C)} \tag{10}
\]

The chosen sawtooth amplitude \(V_{\text{ref,comp}}\) is 1 V here and \(C \approx 140 \text{ fF}\), so that frequencies between 7 Hz and 700 kHz are obtained for a sensor current range from \(10^{-12}\) to \(10^{-7}\) A. The number of reset pulses is counted with an in-sensor-site counter (24 stages in [54]). For readout, the counter circuit is converted into a shift register by a control signal and the data are provided to the output.

For test purposes, an array with \(16 \times 8\) test sites is fabricated. Two different comparator circuit designs are used for the generator and for the collector branch. Both comparators are based on a Miller-type operational amplifier. They differ in the reset pulse-shaping circuit.

These test arrays also provide a test/calibration current input similar to the case of the arrays discussed above. This option is used to characterize the electrical be-
behavior of the chips. Evaluation is done for a specified range of currents between 1 pA and 100 nA. Fig. 11.22 shows the result of an experimental evaluation of the homogeneity (i.e. the relative accuracy) of the array. The 3σ standard variations of the measured frequencies are plotted for the different comparator circuits and both electrodes. As can be seen, the 3σ values are <2% in the current range from $10^{-10}$ to $2 \times 10^{-8}$ A. In the range from $10^{-11}$ to $10^{-7}$ A, the 3σ variations are <6% for all circuits. At $10^{-12}$ A, 3σ values between 12 and 20% are obtained depending on the circuit type considered.

This behavior can easily be understood using the Gaussian equation for error propagation:

$$\sigma^2[F(p_1, p_2, p_3, \ldots)] = \sum_i \left[ \left( \frac{\partial F}{\partial p_i} \right)^2 \times \sigma^2(p_i) \right]$$

with $F$ being a function of parameters $p_1, p_2, p_3, \ldots$. Applying this relation to Equation (9), the relative standard deviation of the measured frequencies is obtained:

$$\frac{\sigma(f)}{f} \approx \sqrt{\frac{\sigma^2(I_{\text{leak}})}{I_{\text{electrode}}^2} + \frac{\sigma^2(V_{\text{offset,comp}})}{V_{\text{ref,comp}}^2} + \frac{\sigma^2(C)}{C^2} + \sigma^2(t_{\text{delay}}) \times \left( \frac{I_{\text{electrode}}}{V_{\text{ref,comp}} \times C} \right)^2}$$

In the mid-frequency/mid-current range, the variations are dominated by the current- and frequency-independent terms in Equation (12), i.e. by mismatch of the integrating capacitor and by the comparator offset voltage. For low currents/low frequencies, leakage current mismatch leads to a contribution proportional to $1/I_{\text{electrode}}$. In the high-current/high-frequency region, the delay mismatch dominates because the contribution of this parameter increases in proportion to $I_{\text{electrode}}$.

Overall, the data from Fig. 11.22 represent tolerable levels for most applications without calibration at a high dynamic range. If higher accuracy is required, calibration of the individual sensor site circuits as described above can be performed to compensate for these deviations.

---

**Fig. 11.22** Standard variations of the measured frequencies as a function of the input (calibration) current for the two different comparator circuits (types A and B) and both electrodes. The plot is shown for input currents up to 1 µA (specified range: 1 pA–100 nA) to demonstrate the frequency dependence in the high current region more clearly.
In order to demonstrate biological measurements, two sensor rows are spotted with two different DNA probe sequences. An analyte containing target molecules matching one of the probes is applied. A flow cell is used in this experiment which covers only 5 columns and 16 rows of the sensor field, so that only 80 positions are shown in Fig. 11.23. There, a clear increase in count rate is observed at the matching positions (row 8), whereas no response is seen at the mismatching positions (row 7) as compared with the uncovered positions. The gradient in the column direction is assumed to originate from microfluidic nonidealities in the flow cell.

11.4 Label-free Detection Methods

The readout methods discussed so far are based on labeling the target molecules. In this section, we briefly address approaches which allow electronic label-free detection. The goal of such approaches is the simplification of the biochemical procedure needed to operate a DNA sensor since the labeling step applied to the target molecules is avoided here.

It is not the purpose of this section to discuss comprehensively all known suggestions concerning label-free sensor principles including all possible advantages and disadvantages. Here, only some of the most promising and advanced approaches in this area are briefly sketched.

The basic principle of impedance based approaches is depicted schematically in Fig. 11.24. There, the electrical impedance between a sensor electrode and the electrolyte (or between neighboring electrodes) is measured [55–57]. Hybridization events lead to a change in the electrical properties of the electrode–electrolyte in-
Using the first-order equivalent circuit also shown in the figure, hybridization results in a decrease in the capacitive part of the impedance.

The impedance and the impedance change of such sensors are not only determined by a capacitive effect, but also a resistive contribution is found. Both contributions depend on the quality of the layer of probe molecules. If the density of this layer is not sufficient, the resistive element may even shunt the capacitive contribution so that evaluation of this parameter is aggravated. For this reason, phase-sensitive amplifiers (lock-in amplifiers) are usually used to measure amplitude and phase of the sensor signal [57], or resistive and capacitive contributions are distinguished using other discriminating measurement principles [58].

The realization of mass-sensitive approaches [60–63] is usually based on the change of the resonance frequency of an electromechanical sensor due to the increase in the mass attached to the sensor surface in the case of binding events at the sensor surface. A further contribution to the change of the oscillation frequency originates from viscosity changes at the sensor surface after binding events.

An example is depicted in Fig. 11.25, where the topology of a film bulk acoustic wave resonator (FBAR) is shown [60]. A piezoelectric layer is sandwiched between two metal electrodes. The top electrode is coated with a biochemical coupling layer. The resonance frequency of the resonator is determined by the thickness of the piezoelectric layer and the mass of the electrodes. To prevent leakage of acoustic energy into the substrate, an acoustic mirror (similar to an optical Bragg reflector) is formed by several layers with alternating low and high acoustic impedances.

The resonance frequencies of the FBAR oscillator circuit in water and after forming a BSA layer on the sensor surface are shown in Fig. 11.26. A shift of 850 kHz compared with the pure water case is observed. Since frequencies are measurable with very high accuracy, this approach promises highly sensitive sensors. Moreover, the principle is robust against imperfect properties such as pinholes of the probe molecule layer.
A very similar sensor principle uses cantilevers instead of film bulk acoustic wave resonators [62, 63]. In particular, it has been demonstrated [63] how active CMOS circuitry is used to enhance significantly the quality factor ($Q$) of oscillation-based systems.

11.5 Conclusions

The development of CMOS-based DNA sensor arrays with fully electronic readout promises to provide tools with several advantages over DNA microarrays based on optical readout techniques, but today’s state of development is lower for the electronic devices. Recent achievements, however, envision application scenarios using CMOS sensor arrays for the near future, such as individual medication, point-of-care DNA diagnosis and high dynamic range gene expression at attractive
costs. In this chapter, the potential of a fully electronic CMOS-based DNA sensor array based on an electrochemical redox-cycling method has been shown. The integration of specific transducer materials for building the sensor and sensor-related circuit design issues have been discussed in detail. The future challenge is to develop a complete, robust and user-friendly system consisting of an advanced chip, a related package, the readout apparatus including software and biochemical assays specifically developed for the different applications. The next-but-one step may be to switch to label-free detection-based sensors to reduce further the complexity of biotechnological pre-processing.

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11.7 References

3 http://www.nature.com/ng/chips_interstitial.html.
11.7 References
11 CMOS-based DNA Sensor Arrays


## List of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Units</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A(V_t)$</td>
<td>[mV μm]</td>
<td>transistor threshold voltage-related matching constant</td>
</tr>
<tr>
<td>$a$</td>
<td>[A$^{1/2}$]</td>
<td>process- and circuit design-dependent constant used to describe the relative error of the transfer characteristics of a sensor test site circuit</td>
</tr>
<tr>
<td>$C$</td>
<td>[F]</td>
<td>capacitance</td>
</tr>
<tr>
<td>$ce$</td>
<td>[I]</td>
<td>collection efficiency</td>
</tr>
<tr>
<td>$\Delta V_{t,Mn12,Mn11}$</td>
<td>[V]</td>
<td>difference of transistor threshold voltages of n-MOS transistors Tn11 and Tn12</td>
</tr>
<tr>
<td>$\Delta V_{t,Mp32,Mp31}$</td>
<td>[V]</td>
<td>difference of transistor threshold voltages of p-MOS transistors Tp32 and Tp31</td>
</tr>
<tr>
<td>$F(p_1, p_2, p_3, \ldots)$</td>
<td></td>
<td>function of parameters $p_1$, $p_2$, $p_3$, \ldots</td>
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<tr>
<td>$f$</td>
<td>[s$^{-1}$]</td>
<td>oscillation frequency</td>
</tr>
<tr>
<td>$I_0$</td>
<td>[A]</td>
<td>process- and device type (n- or p-MOS)-dependent constant used to model the transistors subthreshold current</td>
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<td>$I_{cal}$</td>
<td>[A]</td>
<td>calibration current used to calibrate the sensor site related gain stages</td>
</tr>
<tr>
<td>$I_{col}$</td>
<td>[A]</td>
<td>collector electrode current</td>
</tr>
<tr>
<td>$I_D$</td>
<td>[A]</td>
<td>transistor drain current</td>
</tr>
<tr>
<td>$I_{electrode}$</td>
<td>[A]</td>
<td>sensor electrode current</td>
</tr>
<tr>
<td>$I_{gen}$</td>
<td>[A]</td>
<td>generator electrode current</td>
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<tr>
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<td>[A]</td>
<td>leakage current</td>
</tr>
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<td>[A]</td>
<td>output current of sensor site-related gain stage</td>
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<td>[A/V$^2$]</td>
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<tr>
<td>$L$</td>
<td>[μm]</td>
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<td>[V]</td>
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<tr>
<td>$V_{G,n}$</td>
<td>[V]</td>
<td>n-MOS transistor gate voltage</td>
</tr>
<tr>
<td>$V_{G,p}$</td>
<td>[V]</td>
<td>p-MOS transistor gate voltage</td>
</tr>
<tr>
<td>$V_{ref,comp}$</td>
<td>[V]</td>
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<tr>
<td>Symbol</td>
<td>Unit</td>
<td>Description</td>
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<tr>
<td>-----------------</td>
<td>------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td>$V_{\text{offset,comp}}$</td>
<td>[V]</td>
<td>comparator input offset voltage</td>
</tr>
<tr>
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<td>[V]</td>
<td>transistor threshold voltage (mean value)</td>
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<tr>
<td>$V_{t,n}$</td>
<td>[V]</td>
<td>n-MOS transistor threshold voltage (mean value)</td>
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<td>$V_{t,p}$</td>
<td>[V]</td>
<td>p-MOS transistor threshold voltage (mean value)</td>
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<td>[µm]</td>
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<tr>
<td>$W_{Mn11}$</td>
<td>[µm]</td>
<td>width of n-MOS transistor Mn11</td>
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