# 1
# Fabrication Technology

*O. Brand, School of Electrical and Computer Engineering,*
*Georgia Institute of Technology, Atlanta, GA, USA*

**Abstract**
This chapter provides an overview on fabrication technologies for CMOS-based microelectromechanical systems (MEMS). The first part briefly introduces the basic microfabrication steps, highlights a CMOS process sequence and how CMOS materials can be used for microsystems design. While a number of microsystems can be fabricated within the regular CMOS process sequence, the focus of the chapter is on combining CMOS technology with micromachining process modules. CMOS-compatible bulk and surface micromachining techniques are introduced in the second part of the chapter together with an overview of the design challenges faced when combining mechanical microstructures and electronics on the same substrate. The micromachining modules can either precede (pre-CMOS), follow (post-CMOS) or be performed in between (intra-CMOS) the regular CMOS process steps. The last part of the chapter provides an extensive overview on the different CMOS-based MEMS approaches found in the literature.

**Keywords**
Micromachining; CMOS-based MEMS; MEMS fabrication; microsystem fabrication



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## 1.1 CMOS Technology

State-of-the-art CMOS processes, such as IBM's 9S2 process based on SOI (silicon-on-insulator) technology on 300 mm wafers, feature a minimal physical gate length of less than 100 nm and up to eight (copper) metallization levels (see Fig. 1.1, [1]). Such advanced CMOS processes are required for the fabrication of today's and tomorrow's microprocessors comprising tens of millions of transistors on a single chip. An example is Apple Computer's 64-bit PowerPC-G5 processor with more than 58 million transistors [2], manufactured using IBM's 90 nm CMOS technology.

Researchers at IBM's T. J. Watson Research Center have recently used the copper-based interconnect technology of such modern CMOS processes to fabricate microelectromechanical devices, namely r.f. switches and resonators [3, 4]. Up to now, however, most commercially available microsystems combining (micromachined) transducer elements and integrated electronics on a single chip rely on CMOS or BiCMOS processes with minimum feature sizes typically between 0.5 and 3 μm and 4 or 6 in wafer sizes. While the underlying CMOS technologies are between 10 and 15 years old, their capabilities are sufficient for most microsystem applications. An example is the pressure sensor KP100 by Infineon Technologies, a surface micromachined pressure sensor array with on-chip circuitry for signal conditioning, A/D conversion, calibration and system diagnostic, which is based on a 0.8 μm BiCMOS technology on 6 in wafers [5].

A typical cross-section of a sub-μm (0.5–1.0 μm) CMOS technology used for CMOS-based microelectromechanical systems (MEMS) is shown in Fig. 1.2 [6].

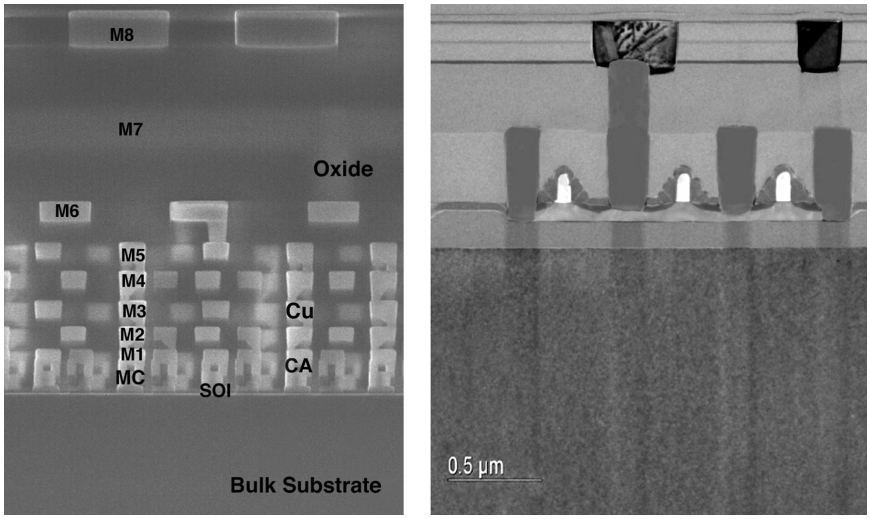


**Fig. 1.1** Cross-section of IBM's 90 nm CMOS technology 9S2 with 8-level copper metallization (labeled M1–M8) with close-up of three metal–oxide–semiconductor field effect transistors (MOSFETs). Images courtesy of International Business Machines Corporation; unauthorized use not permitted

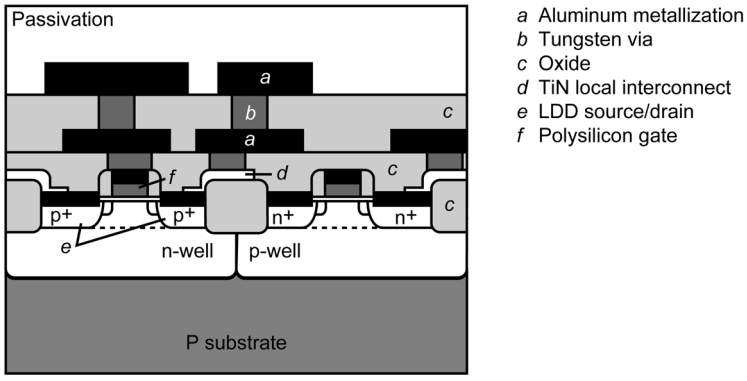


**Fig. 1.2** Schematic cross-section of typical sub-µm (0.5–1.0 µm) CMOS technology with two-level aluminum metallization and TiN local interconnects. Adapted from [6]

The twin-well technology is based on 6 in p-type wafers and uses a polysilicon/silicide gate, low-doped drain (LDD) technology for source and drain formation, silicide source/drain contacts and a two-level metallization based on tungsten plugs and aluminum interconnects. A thermal oxide separates adjacent transistors, chemical vapor deposition (CVD) silicon dioxide layers are used as dielectric layers between the metallization levels and a PECVD (plasma enhanced CVD) silicon nitride layer or a silicon dioxide, silicon nitride sandwich are employed as pas-

sivation layer. The CMOS fabrication sequence is briefly highlighted in Section 1.1.2. More detailed process descriptions can be found in a number of microelectronics textbooks, e.g. [6–8].

When designing CMOS-based MEMS or microsystems, the designer must adhere, to a great extent, to the chosen CMOS process sequence in order not to sacrifice the functionality of the on-chip electronics. This limits the available 'design space' for the integrated microsystems, as e.g. materials, material properties and layer thicknesses are determined by the CMOS process. In the following, a brief introduction into integrated circuit fabrication will be given: the basic fabrication steps are highlighted (Section 1.1.1) and a CMOS process sequence is summarized (Section 1.1.2). Section 1.1.3 discusses how the different CMOS materials and layers can be used in micro- and nanosystems and Section 1.1.4 depicts a few microsystems that can be completely formed within a regular CMOS sequence.

### 1.1.1 Basic Microfabrication Steps

The fabrication of integrated circuits (ICs) using CMOS or BiCMOS technology is based on four basic microfabrication techniques: deposition, patterning, doping and etching. Fig. 1.3 illustrates how these techniques are combined to build up an IC layer by layer: a thin film, such as an insulating silicon dioxide film, is deposited on the substrate, a silicon wafer. A light-sensitive photoresist layer is then deposited on top and patterned using photolithography. Finally, the pattern is transferred from the photoresist layer to the silicon dioxide layer by an etching process. After removing the remaining photoresist, the next layer is deposited and struc-

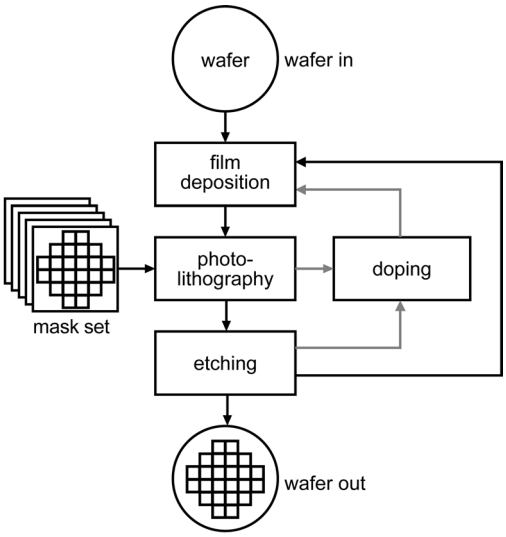


**Fig. 1.3** Flow diagram of IC fabrication process using the four basic microfabrication techniques: deposition, photolithography, etching and doping. Adapted from [8]

tured, and so on. Doping of a semiconductor material by ion implantation, the key step for the fabrication of diodes and transistors, can be performed directly after photolithography, i.e. using a photoresist layer as mask, or after patterning an implantation mask (e.g. a silicon dioxide layer).

*Silicon* is the standard substrate material for IC fabrication and, hence, the most common substrate material in microfabrication in general. It is supplied as single-crystal wafers with diameters between 100 and 300 mm. In addition to its favorable electrical properties, single-crystal silicon also has excellent mechanical properties [9], which enable the design of micromechanical structures. CMOS processes for digital electronics typically use low-doped (doping concentration in the $10^{16}\,cm^{-3}$ range) silicon wafers, whereas processes for mixed-signal or analog electronics are often based on high-doped (doping concentration in the $10^{19}\,cm^{-3}$ range) wafers with a low-doped epitaxial layer to minimize latch-up. The choice of the substrate material might already require a compromise between the requirements for the MEMS part and the on-chip electronics: the fabrication of membrane structures for, e.g., pressure sensors is typically based on anisotropic silicon etching in a potassium hydroxide (KOH) solution (see Section 1.2). High p-type doping ($N_A \geq 10^{19}\,cm^{-3}$) substantially reduces the silicon etch rates in KOH solutions, thus preventing the use of highly p-doped CMOS substrates in combination with KOH etching.

In the following, a brief overview on the four basic microfabrication steps will be given. More details can be found in textbooks and reference books on semiconductor processing [6–8, 10, 11].

#### 1.1.1.1 **Thin-film Deposition**

The two most common thin-film deposition methods in microfabrication are *chemical vapor deposition* (CVD), performed at low pressure (LPCVD), atmospheric pressure (APCVD) or plasma-enhanced (PECVD), and *physical vapor deposition* (PVD), such as sputtering and evaporating. Typical CVD and PVD film thicknesses are in the range of tenths of nanometers up to a few micrometers. Other film deposition techniques include electroplating of metal films (e.g. the copper metallization in state-of-the-art CMOS processes) and spin- or spray-coating of polymeric films such as photoresist. Both processes can yield film thicknesses from less than 1 μm up to several hundreds of micrometers.

*Dielectric* layers, predominantly silicon dioxide, $SiO_2$, and silicon nitride, $SiN_x$, are used as insulating material, as mask material and for device passivation. Silicon dioxide is either thermally grown on top of a silicon surface (thermal oxide) at high temperatures (900–1200 °C) in an oxidation furnace or it is deposited in a CVD system (CVD oxide). CVD oxides can be deposited at temperatures between 300 and 900 °C, with the high-temperature depositions usually yielding better film properties. Low-temperature CVD oxide films are typically deposited in PECVD systems and high-temperature CVD oxide films in LPCVD equipment. Silicon nitride layers deposited in LPCVD furnaces are commonly used as masking

material during local oxidation of silicon (LOCOS process), while PECVD silicon nitride films are used for e.g. device passivation.

Highly doped *polycrystalline silicon* (polysilicon) is used as gate material for metal oxide semiconductor field effect transistors (MOSFETs), as electrode and resistor materials, for piezoresistive sensing structures, as thermoelectric material, and for thermistors. Polysilicon microstructures released by sacrificial layer etching are also widely used in sensor applications (see Section 1.4). Polysilicon is usually deposited in an LPCVD furnace using silane ($SiH_4$) as gaseous precursor.

*Metal* layers are used, e.g., for electrical interconnects, as electrode material, for resistive temperature sensors (thermistors) or as mirror surfaces. Metals, which are widely used in the microelectronics industry, such as aluminum, titanium and tungsten, are routinely deposited by sputtering. Depending on the application, a large number of other metals, including gold, palladium, platinum, silver or alloys, can be deposited with PVD methods. A number of metals and metal compounds, such as Cu, $WSi_2$, $TiSi_2$, TiN and W, can be deposited by CVD. Metal CVD processes are less common, but can provide improved step coverage or local deposition of metals. Whereas aluminum has been the standard metallization in IC fabrication for many years, the state-of-the-art sub-0.25 μm CMOS technologies often feature copper as interconnect material, owing to its lower resistivity and higher electromigration resistance as compared with aluminum. An example is IBM's interconnect metallizations based on the so-called damascene process [12], which employ copper films electroplated in a dielectric mold. After each metallization step, planarization is achieved with a chemical–mechanical polishing (CMP) step.

*Polymers* such as photoresist are commonly deposited by spin- or spray-coating. Polymers can be used as dielectric materials, passivation layers, and as chemically sensitive layers for chemical and biosensors ([13]; see also Chapter 7).

#### 1.1.1.2 **Patterning**

Photolithography is the standard process to transfer a pattern, which has been designed with computer-aided-engineering (CAE) software packages, on to a certain material. The process sequence is illustrated in Fig. 1.4. A mask with the desired pattern is created. The mask is a glass plate with a patterned opaque layer (typically chromium) on the surface. Electron-beam lithography is used to write the mask pattern from the CAE data. In the photolithographic process, a photoresist layer (photostructurable polymer) is spin-coated on to the material to be patterned. Next, the photoresist layer is exposed to ultraviolet (UV) light through the mask. This step is done in a mask aligner, in which mask and wafer are aligned with each other before the subsequent exposure step is performed. Depending on the mask aligner generation, mask and substrate are brought in contact or close proximity (contact and proximity printing) or the image of the mask is projected (projection printing) on to the photoresist-coated substrate. Depending on whether positive or negative photoresist was used, the exposed or the unexposed photoresist areas, respectively, are removed during the resist development process.

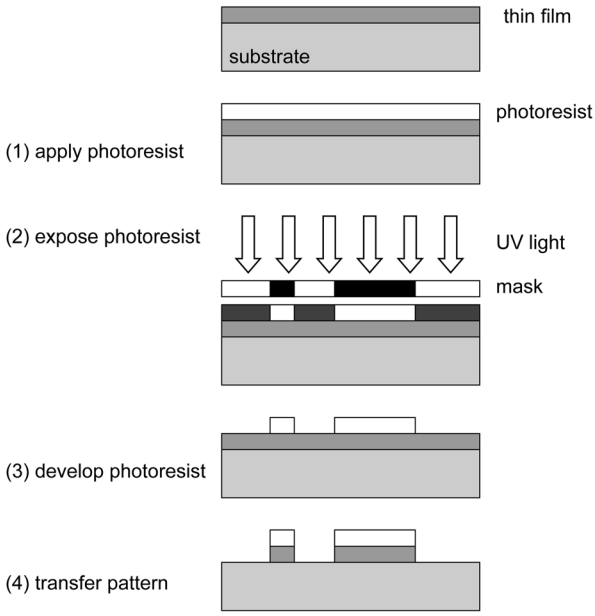


**Fig. 1.4** Schematic of a photolithographic process sequence to structure a thin-film layer

The remaining photoresist acts as a protective mask during the subsequent etching process, which transfers the pattern onto the underlying material. Alternatively, the patterned photoresist can be used as a mask for a subsequent ion implantation. After the etching or ion implantation step, the remaining photoresist is removed, and the next layer can be deposited and patterned.

The so-called *lift-off technique* is used to structure a thin-film material, which would be difficult to etch. Here, the thin-film material is deposited on top of the patterned photoresist layer. In order to avoid a continuous film, the thickness of the deposited film must be less than the resist thickness. By removing the underneath photoresist, the thin-film material on top is also removed by 'lifting it off', leaving a structured thin film on the substrate.

Thick photostructurable polymer layers, such as SU-8 [14], can be used as a mold for electroplating metal structures. A thick polymer layer is deposited on top of a metallic seed layer and photostructured. During the subsequent electroplating process, the metal is only deposited in the areas where the seed layer is exposed to the plating solution, i.e. the polymer layer acts as a plating mold.

Recently, microcontact printing or soft lithography [15] has been introduced as an additional method for pattern transfer. A soft polymeric stamp is used to reproduce a desired pattern directly on a substrate. Routinely, feature sizes on the order of 1 μm can be achieved with this technique. The polymer stamp, often made from poly(dimethylsiloxane) (PDMS), is formed by a molding process using a master fabricated with conventional microfabrication techniques. After 'inking' the stamp with the material to be printed, the stamp is brought in contact with the substrate material, and the pattern of the stamp is reproduced. Surface proper-

ties of the substrate can therefore be modified to, e.g., locally promote or prevent molecule adhesion. Soft lithography has been specifically developed for biological applications such as patterning cells or proteins with the help of, e.g., self-assembled monolayers (SAMs) [15].

#### 1.1.1.3 **Etching**

The two different categories of etching processes include wet etching using liquid chemicals and dry etching using gas-phase chemistry. Both methods can be either isotropic, i.e. provide the same etch rate in all directions, or anisotropic, i.e. provide different etch rates in different directions (see Fig. 1.5). The important criteria for selecting a particular etching process encompass the material etch rate, the selectivity for the material to be etched, and the isotropy/anisotropy of the etching process. An overview on various etching chemistries used in microfabrication can be found in [16].

Wet etching is usually isotropic with the important exception of anisotropic silicon wet etching in, e.g., alkaline solutions, such as potassium hydroxide (see Section 1.2). Moreover, wet etching typically provides a better etch selectivity for the material to be etched in comparison with neighboring other materials. An example includes wet etching of silicon dioxide using hydrofluoric acid-based chemistries. $SiO_2$ is isotropically etched in dilute hydrofluoric acid ($HF–H_2O$) or buffered oxide etch, BOE ($HF–NH_4F$). Typical etch rates for high-quality (thermally grown) silicon dioxide films are 0.1 μm/min in BOE.

Dry etching, on the other hand, is often anisotropic, resulting in a better pattern transfer, as mask underetching is avoided (see Fig. 1.5). Therefore, anisotropic dry etching processes, such as *reactive ion etching* (RIE), of thin-film materials are very common in the microelectronics industry. In an RIE system, reactive ions are generated in a plasma and are accelerated towards the surface to be etched, thus providing directional etching characteristics. Higher ion energies typically result in more anisotropic etching characteristics, but also in reduced etching selectivity.

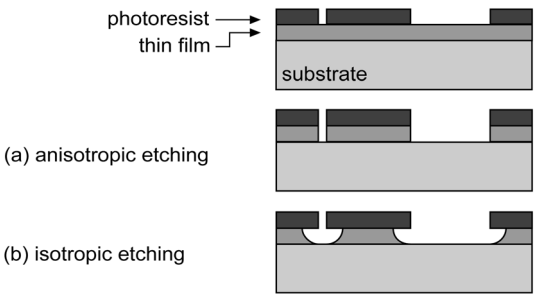


**Fig. 1.5** Schematic of isotropic and anisotropic thin-film etching

#### 1.1.1.4 **Doping**

Doping is used to modify the electrical conductivity of semiconducting materials such as silicon or gallium arsenide. It is hence the key process step for fabricating semiconductor devices such as diodes and transistors. In the case of silicon, doping with phosphorus or arsenic yields n-type silicon, whereas p-type silicon results from boron doping. By varying the dopant concentration of n-type silicon from $10^{14}$ to $10^{20}\,\mathrm{cm}^{-3}$, the resistivity at room temperature can be tuned from approximately 40 to $7\times10^{-4}\,\Omega\,\mathrm{cm}$.

Dopant atoms are introduced by either ion implantation or diffusion from a gaseous, liquid or solid source. Ion implantation has become the key process to introduce precisely defined quantities of dopants in the microelectronics industry. The substrate material, i.e. a silicon wafer, is bombarded with accelerated ionized dopant atoms in an ion implanter. The result is approximately a Gaussian distribution of the dopant atoms in the substrate wafer with a mean penetration depth controlled by the acceleration voltage. A high-temperature diffusion process can then be used to additionally 'drive-in' the dopant until a desired doping profile has been achieved.

### 1.1.2
### CMOS Process Sequence

To be able to integrate microelectromechanical devices with CMOS circuitry, the designer must have an excellent understanding of the underlying CMOS process sequence. The particular process flow is, of course, strongly dependent on the chosen CMOS technology and a detailed description of a CMOS technology goes way beyond the scope of this chapter. Nevertheless, we briefly summarize a typical CMOS process sequence in the following, highlighting the main process steps and their importance for co-integration of CMOS and MEMS. We thereby follow the CMOS process sequence described in detail in [6] (see schematic cross-section in Fig. 1.2), which is typical for a sub-μm technology with minimal feature sizes between 0.5 and 1 μm.

The starting wafer material is a lightly p-doped (100) wafer with a typical doping concentration of $N_A \approx 10^{15}\,\mathrm{cm}^{-3}$. The first step is the definition of the active areas by local oxidation of silicon (LOCOS), thus growing a thick ($\sim 0.5$ μm) field oxide in the areas between the individual transistors. Next, the p-wells for the n-channel MOSFETs and the n-wells for the p-channel MOSFETs are implanted. A joint drive-in for both wells establishes the desired junction depth of 2–3 μm. Typical drive-in times are 4–6 h at 1000–1100 °C. We will see later (Section 1.2) that the n-well diffused in the p-substrate can be used to define accurately the thickness of a silicon membrane. Such membranes are commonly released by anisotropic wet etching from the back of the wafer using an electrochemical etch-stop technique at the p–n junction between n-well and p-substrate [17, 18].

After n- and p-well formation, the MOSFET gate and channel regions are engineered. First, channel implants for the n- and the p-channel transistors are implanted to adjust their threshold voltages to the desired values. After removing the

implantation oxides in the active area, the gate oxide with a thickness ≤10 nm in modern CMOS processes is thermally grown in the active areas. Next, a 0.3–0.5 μm thick polysilicon layer for the gate electrodes is deposited across the wafer in an LPCVD furnace operating at about 600 °C and doped by ion implantation. Finally, the polysilicon layer is patterned to define the actual gate regions. In MEMS, the gate polysilicon can also be used for resistors, piezoresistors, thermopiles, electrodes and as structural materials. The last application often requires a high-temperature anneal of the polysilicon to reduce its residual stress to values acceptable for the microstructures. Such a high-temperature step can be critical at this stage in the CMOS process, as it might effect previous doping distributions and, hence, the CMOS device characteristics.

After gate formation, the source/drain regions are implanted. In typical sub-μm CMOS technologies, this is done using a LDD (lightly doped drain) process. It provides a gradient in the doping of the source/drain regions towards the channel region, reducing the peak value of the electric field close to a channel and, hence, increasing device reliability. First, phosphorus (or arsenic as alternative n-type dopant) is implanted in the source/drain of the NMOS transistors to form $n^-$ regions, followed by a boron implantation of the source/drain of the PMOS transistors to form $p^-$ regions. Next, a conformal spacer dielectric layer is deposited on the wafer and anisotropically etched back, leaving sidewall spacers along the edges of the polysilicon gates. After growing a thin screen oxide for the following implantation, the source/drain regions of the NMOS and PMOS transistors not protected by the sidewall spacer are successively implanted to form $n^+$ and $p^+$ regions, respectively. The final step of the source/drain engineering is a furnace anneal, typically at ∼ 900 °C for 30 min, to activate the implants, anneal implant damage and drive the junctions to their final depth. Alternatively to the furnace anneal, a much shorter rapid thermal anneal at higher temperatures can be performed (e.g. 1 min at 1000–1050 °C). The fabrication of the active devices is now completed. Any subsequent high-temperature step (above 700–800 °C) necessary for the MEMS fabrication must be carefully qualified, as it might affect the doping distributions in the active devices, thus potentially changing the device characteristics.

In the back end of the process, the individual active devices are interconnected on the wafer to form circuits and pads for input/output connections off the chip are created. Although a large number of back-end metallization process flows with up to eight metallization levels exist, the exemplary CMOS process described in [6] uses three metallization levels with a local interconnect level based on titanium nitride and two wiring levels based on aluminum. The contacts to the source/drain regions and to the gate polysilicon are based on titanium silicide ($TiSi_2$). To this end, a thin titanium layer (50–100 nm) is sputtered on the wafer after removal of the implantation oxide. During an annealing step at about 600 °C in $N_2$, the titanium reacts with Si where they are in contact (e.g. source, drain and gate polysilicon) to form $TiSi_2$ and with $N_2$ to form TiN elsewhere. The resulting TiN layer is patterned to create a local interconnect. Subsequently, the wafer surface is typically planarized using a PSG (phosphosilicate glass) or BPSG (borophosphosilicate glass) layer reflown at 800–900 °C. Modern CMOS processes often

use chemical mechanical polishing (CMP) for interconnect and interconnect dielectric planarization. In the process described in [6], each of the following wiring levels uses CVD tungsten vias with a TiN adhesion/barrier layer and an aluminum (with a small percentage of Si and Cu) interconnect layer. Finally, the passivation layer is deposited (typically by PECVD) and patterned to form the pad openings necessary to contact the device from the outside. The composition of the passivation layer and especially its residual stress can be adapted according to the needs of the microstructures (see Section 1.3.1). After passivation, the wafers are annealed at low temperatures (400–450 °C) for about 30 min in forming gas (10% $H_2$ in $N_2$) to alloy the metal contacts.

The CMOS process presented in [6] and briefly described here requires 16 masks. A schematic device cross-section is shown in Fig. 1.2.

### 1.1.3 CMOS Materials for Micro- and Nanosystems

The particular CMOS technology chosen for the implementation of a micro- or nanoelectromechanical system (MEMS or NEMS) dictates the overall process sequence, the doping profiles and junction depths of doped silicon regions, and the material properties and thicknesses of the different thin-film layers. In general, only minimal adaptations can be made in order not to compromise the performance of the CMOS circuits (see Section 1.3). However, the different layers of the CMOS process can be used for the fabrication of the microstructures themselves. Tab. 1.1 summarizes the different doping regions and layers of a typical CMOS process and their use in MEMS and NEMS.

Two examples, namely a CMOS-based mass-sensitive chemical sensor [19–21] and a CMOS-based thermal imager [22, 23], will be discussed in the following. The mass-sensitive chemical sensor (see Fig. 1.6) is based on a 150 µm long and 140 µm wide cantilever beam consisting of the n-well of the CMOS process covered by the CMOS dielectrics [21]. Thus, the n-well and the CMOS dielectrics are used as structural materials. The cantilever is released after completion of the CMOS process by three post-CMOS micromachining steps: first, a silicon membrane is formed by anisotropic wet etching from the back of the wafer in combination with an electrochemical etch-stop technique at the p–n junction between p-substrate and n-well; thereafter, the cantilever is released by two reactive ion etching (RIE) steps. The two aluminum metallization layers are used to form a planar coil on top of the cantilever, enabling the generation of transverse vibrations in the presence of an external DC magnetic field parallel to the cantilever length. The transverse vibration are detected with stress-sensitive diode-connected PMOS transistors, arranged in a Wheatstone bridge configuration at the cantilever's clamped edge. Alternatively, piezoresistors can be formed using either the $p^+$-source/drain implantation of a PMOS transistor or the $n^+$-doped gate polysilicon. The cantilever beam is coated with a chemically sensitive polymer layer. Upon absorption of analyte in the polymer layer, the cantilever's mass increases and, hence, its resonance frequency decreases. The change of resonance frequency is

**Tab. 1.1** Common CMOS materials and their use in micro- and nanoelectromechanical systems (MEMS and NEMS)

| *CMOS layer/structure* | *Use in MEMS and NEMS* |
|---|---|
| n-well/p-well | Structural material<br>Thermal conductor/mass |
| Source/drain implantation | Resistor<br>Piezoresistor<br>Thermopile<br>Electrode |
| Field oxide | Structural material<br>Thermal insulator<br>Sacrificial material |
| Gate polysilicon<br>(and optional 2nd polysilicon) | Resistor<br>Piezoresistor<br>Thermopile<br>Electrode<br>Structural material<br>Sacrificial material |
| Contact and intermetal oxides | Structural material<br>Thermal insulator<br>Sacrificial material |
| Metallization<br>(and optional multi-level metallizations) | Conductor<br>Mirror<br>Thermal conductor<br>Electrode<br>Structural material<br>Sacrificial material |
| Passivation | Structural material<br>Thermal insulator<br>Stress compensation<br>Infrared radiation absorber |

sensed by incorporating the resonant cantilever into an amplifying feedback loop [20, 21].

The thermal imager shown in Fig. 1.7 is based on a $\sim 3\times3\,\mathrm{mm}^2$ membrane consisting of the dielectric layers of the CMOS process [22, 23]. The membrane is released by wet anisotropic silicon etching from the back of the wafer after completion of the regular CMOS process sequence. The thick field oxide is used as an intrinsic etch-stop layer. The CMOS dielectrics, i.e. the field oxide, the contact oxide, the intermetal oxide and the passivation, are used as structural materials. A grid of electroplated gold lines provides additional structural support to the membrane and divides it into 100 pixels. The gold lines are electroplated after the CMOS process in a standard process step normally preparing the wafers for TAB (tape automated bonding). Sandwiched in between the CMOS dielectrics on each pixel is a polysilicon/aluminum thermopile and a polysilicon heating resistor. The

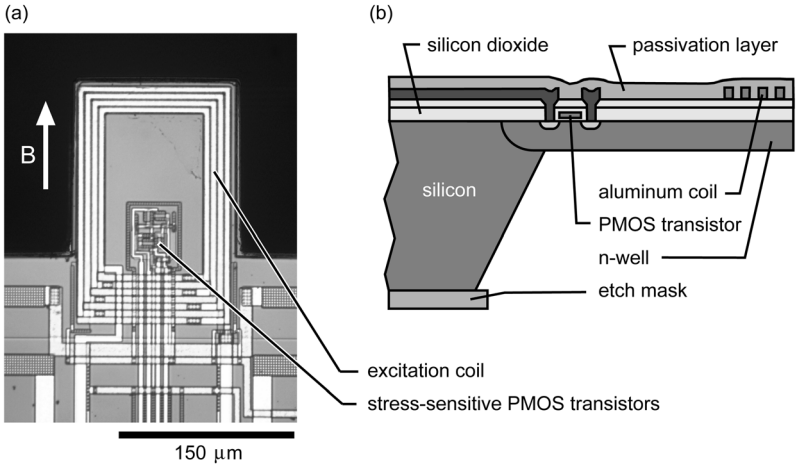


**Fig. 1.6** (a) Photograph and (b) schematic cross-section of a cantilever-based mass-sensitive gas sensor. The cantilever structure features an integrated planar coil for electromagnetic excitation of transverse vibrations in the presence of a DC magnetic field and PMOS transistors in a Wheatstone bridge arrangement for deflection detection [21]. Photograph courtesy of C. Vancura, ETH Zurich, Switzerland

incoming infrared (IR) radiation is absorbed in the CMOS thin-film sandwich

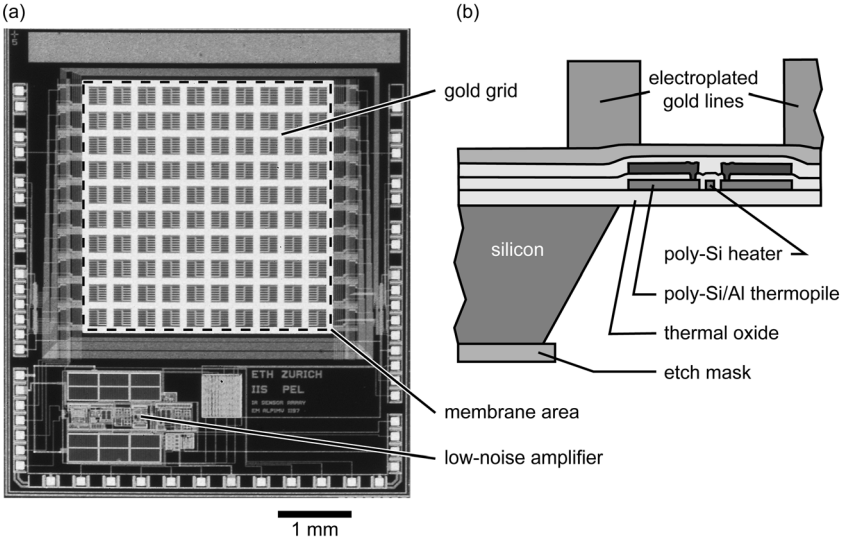


**Fig. 1.7** (a) Photograph and (b) schematic cross-section of a CMOS-based infrared radiation sensor array. The sensor array is located on a micromachined membrane consisting of the dielectric layers of the CMOS process. An electroplated gold grid divides the membrane in a 10×10 array of pixels, each incorporating a thermopile with 16 polysilicon/aluminum thermocouples for temperature sensing. On-chip circuitry includes a multiplexer and a low-noise chopper amplifier [22, 23]. Photograph courtesy of Prof. H. Baltes, ETH Zurich, Switzerland

(including the passivation), resulting in a measurable temperature elevation of the individual pixels. All structures necessary for IR radiation sensing are completely formed within the regular CMOS process sequence [22, 23].

### 1.1.4 CMOS Microsystems

A number of microsensors can be completely formed within the regular CMOS process sequence, typically not requiring any additional process steps. Well-known examples include temperature sensors [24, 25], magnetic field sensors (especially Hall sensors) [26] and CMOS imagers [27, 28]. An additional subset of CMOS-based microsystems only requires either the modification of a CMOS layer or the deposition and patterning of additional layers, but no micromachining steps. A few selected examples will be given in the following.

Chemical sensors and biosensors relying on an electrochemical sensing principle require an electrode in contact with the sample to be sensed. Examples include amperometric sensors, palladium-gate FET and ISFET (ion-sensitive field effect transistor) structures, and also chemoresistors and chemocapacitors. A number of these electrochemical sensors have been co-integrated with CMOS circuitry (see Chapter 7), typically requiring deposition and patterning of special metal electrodes and/or passivation layers in addition to the regular CMOS process sequence.

Examples are the CMOS-based biosensor arrays developed recently for DNA analysis [29, 30] and recording of neural activity [31]. The sensor arrays are based on a standard 0.5 μm CMOS process optimized for analog applications [30]. After deposition and patterning of the second aluminum layer, a silicon dioxide layer is deposited, followed by a planarization step using CMP and the deposition of a silicon nitride passivation. The actual sensor electrodes are fabricated on top of the nitride passivation. First, vias are etched to enable contacts to the aluminum metallization and are filled with a Ti/TiN barrier layer and CVD tungsten [30]. In the case of the DNA arrays, the final interdigitated gold electrodes are deposited by evaporation of a Ti/Pt/Au electrode stack, which is patterned using a lift-off technique ([30]; see Fig. 1.8). In the case of the sensor arrays for neural activity recording, the sensor electrodes and the contact pads are defined by depositing and lift-off patterning of a Ti/Pt layer. Subsequently, a dielectric layer sandwich consisting of different $TiO_2$ and $ZrO_2$ layers is deposited and opened at the location of the bond pads. Neural activity is recorded capacitively with the sensor electrodes covered by the protective dielectric layer sandwich. Finally, a gold layer is deposited on the Pt pads and structured using a lift-off process [31].

Researchers at ETH Zurich have recently reported a CMOS-integrated microelectrode array for stimulation and recording of natural neural networks [32]. The microsystem is fabricated using a 0.6 μm CMOS process in combination with a two-mask post-CMOS process sequence to deposit and pattern biocompatible platinum electrodes. The post-CMOS process sequence starts with the deposition and patterning of 50 nm TiW and 270 nm Pt. The metal layer sandwich is structured

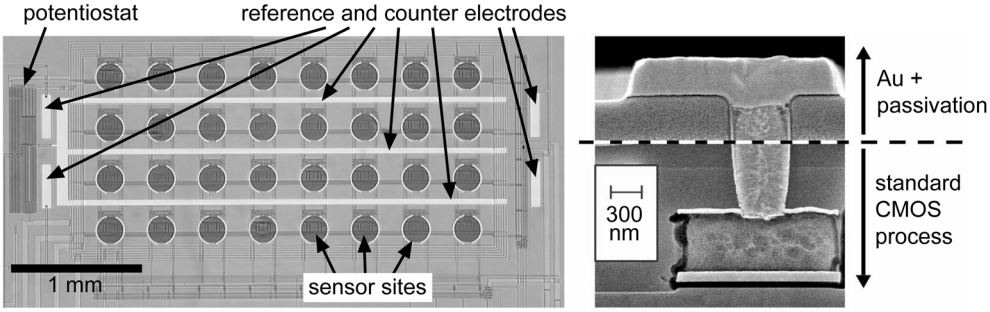


**Fig. 1.8** (a) Photograph of an 8×4 element DNA sensor array with a single sensor diameter of 200 µm and a sensor pitch of 400 µm; (b) SEM photograph of sensor cross-section showing the standard CMOS metallization, the tungsten vias and the gold sensor electrodes. Adapted from [30]

using a lift-off technique. Finally, a 1 µm silicon nitride sealing layer is deposited by PECVD and patterned with RIE.

A CMOS-based biochemical multisensor microsystem requiring no micromachining has been developed by IMEC, K.U. Leuven and Siemens [33]. The microsystem combines, on a single CMOS chip, an array of ISFETs, an amperometric oxygen sensor and a conductometric cell. The biochemical analysis system is based on double-metal, 1.2 µm CMOS technology. A special ISFET module has been integrated into the regular CMOS process sequence to form a protective LPCVD nitride layer on top of the ISFET gates. In addition, Ti/Pt electrodes for the amperometric sensor are deposited and patterned and Ag/AgCl reference electrodes are formed by electroplating and electrochloridation [33, 34]. ISFET structures requiring no modifications to the CMOS process sequence have been presented in [35].

Capacitive chemical microsensors based on interdigitated metal electrodes can be fabricated completely within the regular CMOS process sequence. Examples include microsensors for detection of humidity [36, 37] and volatile organic compounds in air [38, 39]. Typically, the interdigitated electrode structure is formed by the metallization layers of the CMOS process. The capacitive sensor structure detects changes in the dielectric constant of a sensing layer deposited on top of it upon absorption of analyte molecules. CMOS-integrated capacitive humidity sensors are produced by Sensirion, Switzerland [40, 177].

Hall plates can be formed completely within a regular (Bi)CMOS process sequence and Hall sensor systems with on-chip circuitry are commercially available, e.g. from Micronas [41], Infineon Technologies [42], Allegro Microsystems [43] and Melexis [44]. Regular Hall plates are arranged parallel to the chip surface and are sensitive to magnetic fields perpendicular to the chip surface. Using spinning-current methods for offset reduction, commercially available CMOS integrated Hall sensors have offsets as low as 0.5 mT [45]. To improve sensor performance, i.e. sensitivity and offset, the Hall sensors have been combined with integrated magnetic flux concentrators by bonding and patterning thin high-permeability,

low-coercivity ferromagnetic layers to the chip surface [46]. In addition to concentrating the magnetic flux at the location of the Hall sensors, the flux concentrators allow the measurement of magnetic fields in the chip plane with standard lateral Hall sensors [46]. Alternatively, magnetic fields parallel to the chip surface can be sensed by vertical Hall sensors, rotated 90° to the chip surface [47, 238]. Recently, CMOS-based vertical Hall sensors have been fabricated by developing a pre-CMOS trench etching technology to define the geometry of the Hall plates ([47]; see Section 1.4.1).

Ferromagnetic films not only are used in combination with Hall sensors, but are also essential for highly sensitive fluxgate sensors. The operation of a fluxgate sensor requires a ferromagnetic core which needs to be saturated periodically by the control circuitry. CMOS-based fluxgate sensors with minimal detectable magnetic fields in the nanotesla range (typical noise levels in the range 5–100 nT/$\sqrt{\text{Hz}}$) have been demonstrated at the Fraunhofer Institute IMS [48, 49], ETH Zurich [50, 51] and EPF Lausanne [52]. In [49], a ferromagnetic $Ni_{81}Fe_{19}$ core is embedded in the intermetal dielectrics between the two metallization layers of a CMOS process. In this way, the required excitation and pick-up coils consisting of metal-1 and metal-2 lines can be wound around the core. The electron beam-evaporated nickel–iron cores are sandwiched between tantalum layers, serving as adhesion layers and diffusion barriers. The metal sandwich is patterned using lift-off techniques. In [50, 51], two 1 μm thick ferromagnetic NiFeMo cores are electroplated on top of the CMOS chip. Finally, the approach presented in [52] uses a soft-magnetic amorphous alloy (Metglas 2714A, Honeywell), which is mounted on top of the CMOS die and structured using a photolithographic process.

The final two examples both require a direct contact with the surface of a CMOS chip during sensing. Fingerprint sensors are used for access control and authentication and are covered in detail in Chapter 8. In the case of a capacitive sensor, a two-dimensional electrode array measures the capacitance between the chip surface and the finger's surface touching the chip with a resolution of typically 500 dpi. The fingerprint sensor developed by Siemens is based on a double-metal, 0.8 μm CMOS process and features, on a single chip, a 256×256 pixel sensor array with a pitch of 50 μm, the necessary data acquisition circuitry, A/D conversion and a parallel interface [53]. The sensor is protected against electrostatic air discharge, caused by touching the sensor with a charged finger, using a grounded refractory metal grid (see Chapter 8).

Wire bonding remains the predominant method for providing electrical interconnections between chip and substrate. Increasing bonding speed paired with decreasing pad-pitch requires careful optimization of the wire bonding process and a profound understanding of the physical processes occurring during the actual bonding process. Recently, CMOS-based force sensors have been developed for in situ investigation of the forces acting on the bond pad during thermosonic ball-wedge wire bonding [54, 55]. The test chips comprise an array of *xyz*-force sensors connected to a multiplexer (see Fig. 1.9). Each *xyz*-sensor features three Wheatstone bridges with piezoresistors to measure the *x*, *y* and *z*-components of the force acting on the bond pad during the wire bonding process. The $p^+$ and $n^+$

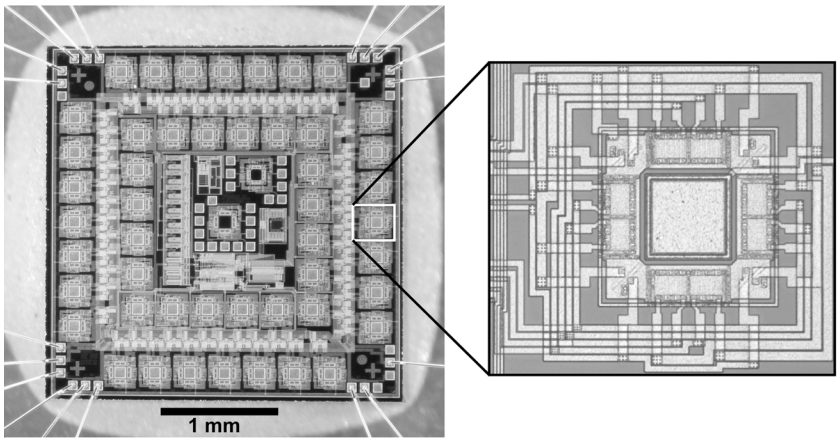


**Fig. 1.9** Test chip with 48 *xyz*-force sensors connected to a multiplexed bus; the close-up of one *xyz*-force sensor shows the test pad with a size of 65 µm and the surrounding piezoresistors for *x*, *y* and *z*-force sensing [54]

source/drain implantations of a double-metal, 0.8 µm CMOS process are used to form the piezoresistors surrounding the bond pad. Hence, the force sensors can be completely formed within the regular CMOS process sequence, potentially allowing the implementation of bonding test structures into regular CMOS designs.

In all of the above cases, no micromachining steps are involved. The focus of the remainder of this chapter (and the main focus of this book) is on CMOS-based micro- and nanosystems requiring either bulk or surface micromachining to release micromechanical structures.

## 1.2 CMOS-compatible Micromachining Process Modules

The basic microfabrication processes described earlier are often combined with special micromachining steps to produce (three-dimensional) microstructures, such as cantilevers, bridges and membranes. In the following, the fundamental micromachining techniques are reviewed. More details on micromachining techniques can be found in dedicated books on microsystem technology [56–59].

The micromachining techniques are categorized into bulk micromachining [60] and surface micromachining processes [61] (see Fig. 1.10). In the case of bulk micromachining, the microstructure is formed by machining the relatively thick bulk substrate material, whereas in the case of surface micromachining, the microstructure comprises thin-film layers, which are deposited on top of the substrate and selectively removed in a defined sequence to release the MEMS structure.

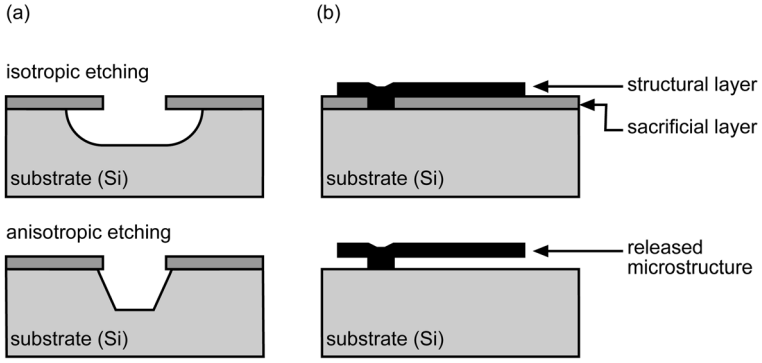


**Fig. 1.10** Schematic of (a) bulk and (b) surface micromachining

### 1.2.1 Bulk Micromachining

Bulk micromachining techniques [60], i.e. etching techniques to machine the (silicon) substrate, can be classified into isotropic and anisotropic, and into wet and dry etching techniques, as can be seen in Tab. 1.2.

The most common *isotropic wet* silicon etchant is HNA, a mixture of hydrofluoric acid (HF), nitric acid ($HNO_3$), and acetic acid ($CH_3COOH$). In this etching system, nitric acid oxidizes the silicon surface and hydrofluoric acid etches the grown silicon dioxide layer. The acetic acid controls the dissociation of $HNO_3$, which provides the oxidation of the silicon. The etch rates and the resulting surface quality strongly depend on the chemical composition [58].

*Anisotropic wet etching* of silicon is the most common micromachining technique and is used to release, e.g. membrane and beam structures. Anisotropic wet etchants etch single-crystalline silicon with different etch rates along different crystal directions. The resulting etch grooves are bound by crystal planes, along which etching proceeds at slowest speed, i.e. the (111) planes of silicon. In case of the commonly used (100) silicon wafers, the (111) planes are intersecting the wa-

**Tab. 1.2** Examples of etching techniques for machining the silicon substrate

| *Type* | *Wet etching* | *Dry etching* |
|---|---|---|
| Isotropic | HNA system<br>$HF–HNO_3–CH_3COOH$ | Vapor-phase etching<br>$XeF_2$ |
| Anisotropic | Alkali metal hydroxide solutions<br>KOH, NaOH<br>Ammonium hydroxide solutions<br>$(CH_3)_4NOH$ (TMAH), $NH_4OH$<br>EDP solutions<br>Other solutions, e.g. hydrazine | Plasma etching<br>RIE, deep-RIE |

fer surface at an angle of 54.7°, yielding the typical pyramid-shaped etch grooves shown in Fig. 1.11. Masking materials for anisotropic silicon etchants are silicon dioxide and silicon nitride. It is important to note that 'convex' corners of the etch mask (as shown in Fig. 1.11) are underetched in the case of (100) silicon substrates, leading to, e.g., completely underetched cantilever structures. The etch rates in preferentially etched crystal directions such as the ⟨100⟩ and the ⟨110⟩ directions, and the ratio of the etching rates in different crystal directions depend strongly on the exact chemical composition of the etching solution and the process temperature [57, 58, 60, 62].

The most common anisotropic silicon etching solution is potassium hydroxide, KOH. As an example, a 6-M KOH solution at 95 °C provides a ⟨100⟩ etch rate of 150 μm/h and an anisotropy, i.e. etch rate ratio, between the ⟨100⟩ and ⟨111⟩ directions of 30–100 : 1 [63]. Since the etch rate of silicon dioxide in KOH solutions is fairly high (for thermal oxide ∼1 μm/h in 6 M KOH solution [58]), silicon nitride films are often used as etching mask. KOH solutions are very stable, yield reproducible etching results and are relatively inexpensive. KOH is, therefore, the most common anisotropic wet etching chemical in industrial manufacturing. The disadvantages of KOH include the relatively high $SiO_2$ and Al etch rates, which require protection of IC structures during etching. Etching with KOH is typically performed from the back of the wafer, with the front side protected by a mechanical cover and/or a protective film [63]. Another issue is the detrimental impact of

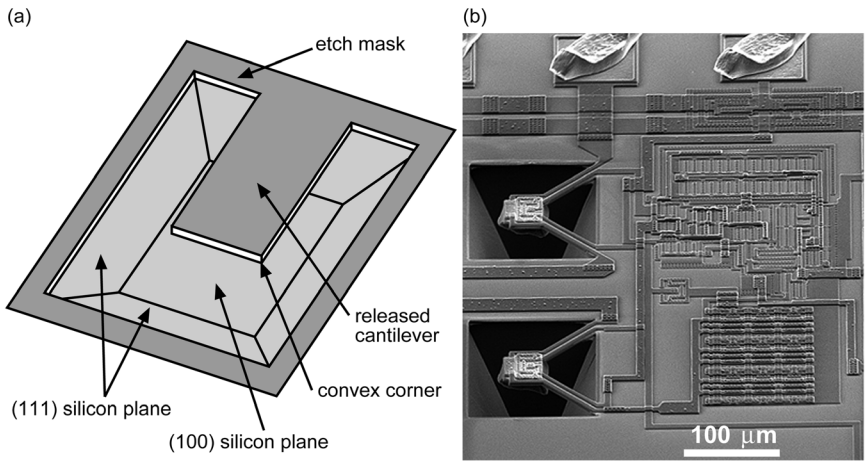


**Fig. 1.11** (a) Schematic of a cantilever beam released by anisotropic silicon etching from the front side of the wafer. The etching mask defines the cantilever shape. The underetching of the cantilever structure starts at convex corners. The resulting etch groove is bound by characteristic (111) side walls and a (100) bottom surface. (b) SEM photograph showing two bulk-micromachined thermal converters cointegrated with CMOS circuitry. The devices are released from the front side of a CMOS wafer by combining anisotropic silicon etching using TMAH with an electrochemical etch-stop technique. SEM photograph courtesy of Prof. G.T.A. Kovacs, Stanford University, USA

alkali metal ions on the characteristics of MOSFET structures. Investigation of MOSFET characteristics after KOH etching from the back of CMOS wafers, however, did not reveal any etching-related damage [63].

Alternative silicon etchants are ammonium hydroxide compounds, such as tetramethyl ammoniumhydroxide (TMAH), and ethylenediamine–pyrocatechol (EDP) solutions. Certain EDP formulations, such as EDP type S, exhibit relatively low Al and $SiO_2$ etch rates, which make them suitable for releasing microstructures from the front side of CMOS wafers [232]. However, EDP solutions age rapidly, are potentially carcinogenic and are very difficult to dispose of. TMAH solutions exhibit similar etching characteristics to EDP, but are easier to handle. By controlling the pH by, e.g., dissolving silicon in the etching solution, the etch rate for aluminum metallizations can be reduced [60, 64], making TMAH also a candidate etchant for releasing microstructures from the front side of CMOS wafers. More detailed discussions of wet etching of silicon can be found, e.g., in [57, 58].

Reliable etch stop techniques are very important for achieving reproducible etching results. As already mentioned, wet anisotropic silicon etchants 'stop' etching, i.e. the etch rate is reduced by at least 1–2 orders of magnitude, as soon as a (111) silicon plane or a silicon dioxide (or silicon nitride) layer is reached. In addition, the etch rate is greatly reduced in highly boron doped regions (doping concentration $\geq 10^{19}$ cm$^{-3}$). The etching can also be stopped at a p–n junction using a so-called electrochemical etch stop technique (ECE) [56, 65]. This method has been extensively used to release silicon membranes and n-well structures (see Fig. 1.12). ECE relies on the passivation of silicon surfaces when an anodic potential is applied that is sufficiently high with respect to the potential of the etching solution.

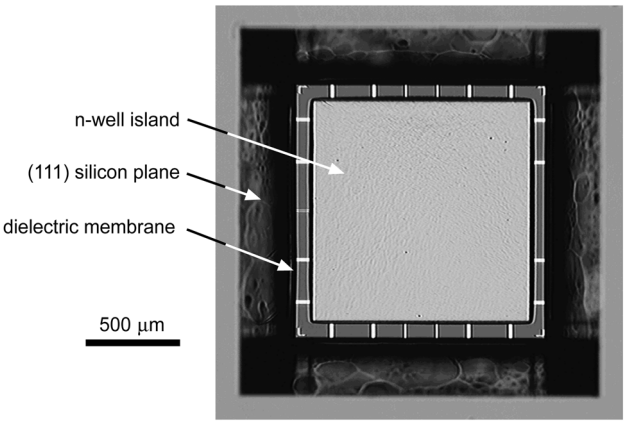


**Fig. 1.12** Micrograph of an anisotropically etched cavity of a capacitive chemical microsystem (see Chapter 7, Fig. 7.32). At the bottom of the cavity, an n-well island structure carrying a thermally stabilized capacitive sensor [67] is visible. The n-well is suspended by a membrane consisting of the CMOS dielectric layers (the embedded metal interconnects connecting the sensor are clearly visible)

*Isotropic dry etching* of silicon can be done using xenon difluoride, $XeF_2$. This vapor-phase etching method exhibits excellent etch selectivity with respect to aluminum, silicon dioxide, silicon nitride and photoresist, all of which can be used as etch masks. However, the resulting etched silicon surfaces are fairly rough. The $XeF_2$ silicon etch rates depend on the loading (size of the overall silicon surface exposed to the etchant) with typical values of $\sim 1\ \mu m/min$. $XeF_2$ etching systems are commercially available from XACTIX [66]. (Alternatively, reactive ion etching (RIE) can be used for isotropic dry etching see also *anisotropic dry etching* below).

*Anisotropic dry etching* of silicon is usually performed by reactive ion etching (RIE) in plasma-assisted etching systems. By controlling the process parameters, such as process gases and process pressure, the etching can be rendered either isotropic or anisotropic. The dry-etching anisotropy mainly originates from the direction of ion bombardment, and is, therefore, independent of the crystal orientation of the substrate material. Most bulk etching of silicon is accomplished using fluorine free radicals with $SF_6$ as a typical process gas. Adding chlorofluorocarbons results in polymer deposition in parallel with etching, which leads to enhanced anisotropy.

Very high aspect ratio microstructures can be achieved with deep (D)RIE, a method which has gained importance during recent years. DRIE systems rely on high-density plasma sources and an alternation of etching and polymer-assisted sidewall protection steps. In a process known as the Bosch process [68], a mixture of trifluoromethane and argon is used for polymer deposition. Owing to the ion

**Tab. 1.3** Comparison of characteristics of common bulk silicon etchants; the etch rates given are typical numbers, the actual etch rates depend on the process parameters (sources for etching rates and selectivities: HNA [9, 58], KOH [58], TMAH [57, 72], $XeF_2$ [66], DRIE [57])

| | ***HNA*** | ***KOH 6 M*** | ***TMAH 22%*** | ***$XeF_2$*** | ***DRIE*** |
|---|---|---|---|---|---|
| Etch type | Wet | Wet | Wet | Dry | Dry |
| Anisotropic? | No | Yes | Yes | No | Yes |
| Si (100) etch Rate [a] (μm/min) | typically > 3 at 25 °C | 2.5 at 95 °C | 0.6 at 80 °C | typically 1 | 2–3 |
| $SiO_2$ etch rate (nm/min) | 30–70 at 25 °C | 15 at 95 °C | 0.1 at 80 °C | 1 : 10000 [c] | 1 : 120–200 [c] |
| $SiN_x$ etch rate (nm/min) | No data available [b] | ≤0.01 at 95 °C | 1 : 3600 [c] at 95 °C | 1 : 100 [c] | No data available |
| ECE etch stop? | Yes | Yes | Yes | No | No |
| Cost | Low | Low | Low | High | High |

**a)** For isotropic etchants, the etch rate is independent of the crystal orientation; for anisotropic dry etching, the etch rate given is in direction of the ion bombardment.

**b)** $SiN_x$ etch rate in HNA is smaller than $SiO_2$ etch rate.

**c)** Selectivities between etch rates $SiO_2$ : Si and $SiN_x$ : Si are given rather than etch rate itself

bombardment, the polymer deposition on the horizontal surfaces can almost be prevented, while the sidewalls are passivated with a Teflon-like polymer. In the second process step, $SF_6$-based etching chemistry provides silicon etching in the non-passivated regions, i.e. the horizontal surfaces. Both process steps are alternated, resulting in typical silicon etch rates of 1–3 μm/min with an anisotropy of the order of 30 : 1 [60]. Silicon dioxide and photoresist layers can be used as etch masks. The DRIE system achieves exceptional anisotropy, which is independent of the crystal orientation, but is far more expensive than e.g. a simple wet-etching setup, and can process only one wafer at a time. Commercial etchers of this type are available from, e.g., Surface Technology Systems (STS) [69], Unaxis Semiconductor [70] and Alcatel [71].

The characteristics of the most common bulk silicon etchants are summarized in Tab. 1.3. In addition to the described 'basic' micromachining processes, a large number of specific silicon-based micromachining processes have been developed. The ones relevant for the fabrication of CMOS-based microsystems will be discussed in Section 1.4.

### 1.2.2 Surface Micromachining

The most commonly used surface micromachining process is sacrificial-layer etching [61]. In this process, a microstructure, such as a cantilever beam or a suspended plate, is released by removing a sacrificial thin-film material, which was previously deposited underneath the microstructure. The release of polysilicon microstructures by removing a sacrificial silicon dioxide film is the most popular surface micromachining technique [61]. Sacrificial aluminum etching (SALE) has been developed to release dielectric microstructures with embedded metal layers [73]. Metallic microstructures deposited by low-temperature PVD processes can use polymer films as sacrificial layers, which are removed using, e.g., an oxygen plasma [74, 75].

A prominent example of a device based on surface micromachined microstructures is the digital micromirror device (DMD) developed by Texas Instruments ([74], see Section 1.4.3). The DMD consists of an array of micromirrors (see Fig. 1.13 a), fabricated on top of a CMOS substrate by deposition and patterning of four metal and two polymer layers. The micromirror array with a pitch of 17 μm is released by removing the polymer sacrificial layers. Fig. 1.13 b shows a surface-micromachined bolometer structure made from polycrystalline $Si_{57}Ge_{43}$ at IMEC (Leuven, Belgium) and Fig. 1.13 c gives details of a 4 μm thick, released polysilicon microstructure fabricated at Analog Devices (Norwood, MA, USA).

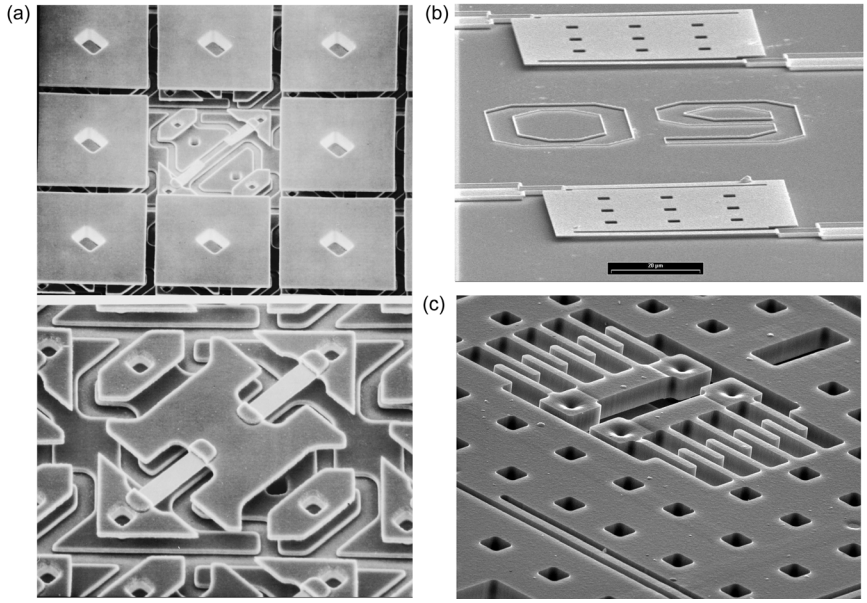


**Fig. 1.13** (a) Top: SEM photograph of 3×3 array of pixels of Digital Micromirror Device (DMD$^{TM}$) by Texas Instruments; the mirror of the center pixel has been removed to show the underlying metal structures. Bottom: SEM photograph shows details of the micromirror yoke and hinges (images from Texas Instruments DLP image library: *http://www.dlp.com*). (b) SEM image of surface-micromachined poly-Si57Ge43 bolometer structures. Courtesy of IMEC, Leuven, Belgium. (c) Detail of surface-micromachined 4 µm thick polysilicon microstructure. Courtesy of Steve Lewis, Analog Devices, Norwood, MA, USA

## 1.3 CMOS-compatible Design of MEMS and NEMS

Can I modify the CMOS process sequence to co-integrate microelectromechanical systems with CMOS circuitry? Can I modify the CMOS process design rules to implement my microstructure? Maybe the questions should be less 'Can I?' but rather 'Where and how much can I?'. In the following section, we would like to give the reader an idea of possible process and design modifications. First and foremost, any modification on the CMOS process sequence and the established design rules for a particular process must not compromise the characteristics and yield of the circuitry components. Therefore, every process modification has to be properly qualified. Even if a process modification is not affecting the circuit characteristics, it might be difficult to implement it in a process run done at a commercial CMOS foundry: it can be very challenging to persuade a CMOS foundry to use pre-processed wafers as starting material or to interrupt the regular process sequence and have additional process steps performed (probably even outside the CMOS foundry) before resuming the 'standard' process sequence. We will see in Section 1.4 that

'substantial' process modifications, as required for pre-CMOS and intra-CMOS approaches, most often require in-house CMOS capabilities. In the following, we will concentrate on 'small' process modifications that might be tolerated by a majority of independent CMOS foundries. Since the author's background is especially in the area of post-CMOS microsystem approaches, most of the discussed process modifications will enable different post-CMOS micromachining modules.

### 1.3.1 Tolerable Process Modifications

If the microstructures are to be released by wet anisotropic silicon etching (especially from the back of the wafer), the wafer starting material for the CMOS process must be considered carefully. Modern CMOS processes often use epitaxial wafers with a weakly p-doped epitaxial layer on top of heavily p-doped substrate as starting material in order to improve latch-up stability. If the substrate p-type doping is above $10^{19}\,cm^{-3}$, the silicon etch rates in common anisotropic etchants, such as KOH and TMAH, are drastically reduced. In addition, the starting material has typically a rather broad specification range for the substrate doping, which, in case of highly p-doped substrates, can result in substantial etch rate variations from wafer to wafer. To ensure compatibility with anisotropic silicon etching, either epi-wafers with reduced substrate doping ($\leq 5\times10^{18}\,cm^{-3}$) or low p-doped non-epi wafers can be used as a starting material [18].

A second challenge for the bulk-micromachining using anisotropic wet etchants is the relatively high interstitial oxygen concentration in the wafer starting material, as required for internal gettering in the CMOS process. With an interstitial oxygen concentration larger than its solid solubility, the oxygen precipitates during annealing steps in the form of oxide particles. Defects caused by oxygen precipitation are commonly used for internal gettering of transition metal impurities during CMOS processing. The oxygen precipitates and the associated crystal defects in CMOS-processed wafers deteriorate the quality of etched cavities, resulting in uneven (111) sidewalls (with crater-like depressions) and large, locally varying underetching of the silicon nitride etch mask, yielding membranes with poor geometric definition [18, 76]. It should be noted that membranes with well-defined lateral dimensions can always be achieved by appropriate design, e.g. using either a $p^{++}$-doped 'etch-stop' ring surrounding the membrane [77] or an electroplated metal ring [22, 63], defining the mechanical edge of the membrane. A reduction of the interstitial oxygen concentration in the starting material from $\sim 8\times10^{17}$ to $(6.0–6.9)\times10^{17}\,cm^{-3}$ resulted in a strongly improved quality of the released microstructures (see Fig. 1.14; [18, 76]). However, the wafer material with reduced defect density also has reduced internal gettering capability and external gettering using, e.g., hard mechanical damage on the wafer back, must be employed. The introduced crystal defects on the wafer back have to be removed at the end of the CMOS process, prior to the deposition of the etch mask.

Any additional (high-temperature) process step performed during or after the regular CMOS process sequence must be considered carefully in terms of the

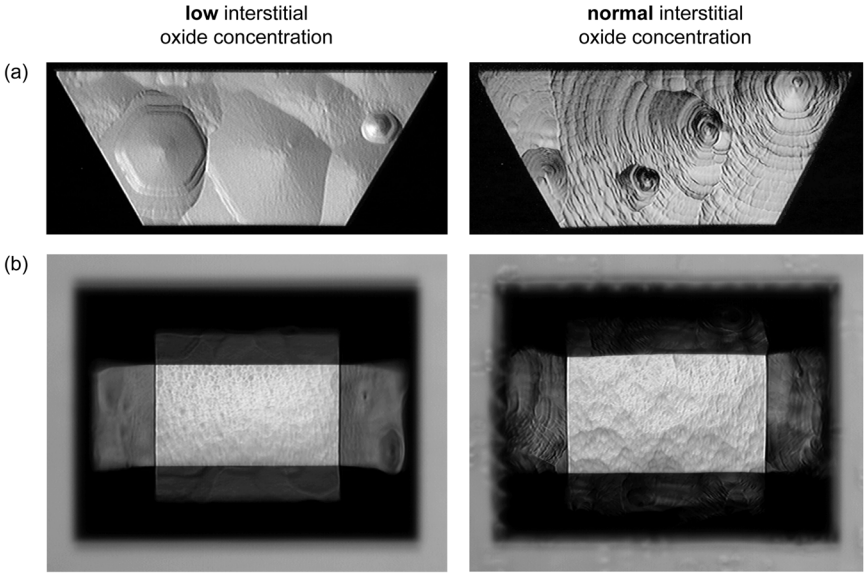


**Fig. 1.14** Quality of etch cavities released by wet anisotropic etching using a 27 wt% (6 M) KOH solution at 90 °C; photographs of (a) (111) sidewalls and (b) (100) etch fronts are shown for test wafers with a normal interstitial oxygen concentration of $\sim 8\times10^{17}$ cm$^{-3}$ and a low interstitial oxygen concentration of $(6.0–6.9)\times10^{17}$ cm$^{-3}$; prior to KOH etching, the wafers were exposed to a thermal simulation of a CMOS process. Adapted from [18]

overall thermal budget of the process. The overall thermal budget critically influences the various doping profiles and thus the resulting device characteristics. Prolonged additional high-temperature process steps with peak temperatures ≥800 °C are likely only possible prior to the channel and source/drain implantations. Medium-temperature processes, such as LPCVD deposition of polysilicon at about 600 °C, have been performed after the source/drain implantations [78], but prior to the back-end aluminum metallization. High-temperature annealing steps required, e.g., for stress relief in the deposited polysilicon layers have to be carefully evaluated, as their thermal budget might influence shallow junction profiles. Of course, the initial doping profiles can be adapted so that additional thermal process steps are taken into account, but this generally requires substantial re-qualification of the CMOS process. The standard aluminum metallization employed in most CMOS processes with minimal feature sizes above 0.25 μm is known to withstand maximum process temperatures of about 450 °C (recent work indicates compatibility with temperatures up to 525 °C [79]), strongly limiting the range of process steps that can be performed after completion of the CMOS process sequence (see Section 1.4.3).

Deposition and patterning of the passivation layer are typically the last process steps of the regular CMOS process sequence. Hence, the passivation composition can often be adjusted to the customer's needs. If the passivation is part of the re-

leased microstructure, its residual stress can be used to tune the stress of the overall microstructure. An example is the thermal imager shown in Fig. 1.7. The membrane with embedded infrared sensor array has a layered structure comprising the different dielectric layers of the CMOS process with polysilicon and metal structures sandwiched in between them. The overall stress of the layer sandwich without the CMOS passivation is compressive in this example, which could result in membrane buckling. To reduce the overall compressive stress in the membrane, a passivation layer with tensile stress is deposited. The stress of a PECVD silicon oxynitride passivation could be controlled in the range from –300 to +300 MPa by choosing an appropriate low frequency (400 kHz) to high frequency (13.56 MHz) power ratio and chamber pressure in the used PECVD system [63]. It should be noted that the stress in the passivation can influence the characteristics of the previous layers, e.g. the electromigration behavior of the underlying metal lines.

### 1.3.2 Design Rule Modifications

Typically, CMOS foundries provide rule-files for their CMOS processes for a number of supported design environments in order to perform design rule checks (DRCs) and extraction of the layout for layout-versus-schematic (LVS) check. The enforced design rules ensure a high yield of the fabricated circuit components within the given process specifications, but might be problematic for the MEMS part. Two examples are given in the following: in order to release microstructures, such as the thermal converters shown in Fig. 1.11, from the front of the wafer, the silicon substrate must be exposed to the etchant in certain areas on the wafer. This can be achieved in a CMOS process by superimposing an active area (i.e. no field oxide), a contact (i.e. no contact oxide), a via (i.e. no intermetal oxide) and a pad opening (i.e. no passivation), thus locally removing all dielectric layers of the CMOS process and exposing the silicon substrate to the environment [80]. The standard design rules of the used CMOS process will, e.g., not allow a via without metal below and on top of it, because a via in a CMOS circuit only makes sense as an interconnect between two metallization levels. Thus, the automated design-rule checker (DRC) will give error messages. In another area one might want to use a non-connected aluminum area as a mirror surface. The DRC will again give an error message because of a non-connected conducting area. Both design examples make no sense in a circuitry environment, but are useful for the MEMS part and, very important, do not compromise the integrity of most CMOS processes (for completeness, it should be mentioned, that sub-0.5 µm CMOS technologies with plated vias might not allow a contact layer without metal overlap in order not to compromise via plug plating and CMP). So, how can one allow such design rule violations and still use the extremely helpful DRC? The ideal case is to write a complete set of design rules for the MEMS areas, having the circuitry checked by the foundry-supplied 'standard' design rule set and the MEMS by an extended design rule set. This approach might be initially more time consuming, but will, in the long run, prevent design errors in the complex MEMS designs.

Modern sub-µm CMOS processes use lithography based on wafer steppers, providing an array of step fields on the wafer with no mutual connection. Post-CMOS micromachining based on anisotropic wet etching in combination with an electrochemical etch-stop technique (see Section 1.4.3) requires the application of etching potentials to (structural) n-well and substrate contacts across the wafer [17, 18]. To supply these etching potentials, a contact network implemented in the metal-1 and metal-2 level of the CMOS process routes the etching potentials from large contact pads to the individual etch contacts. To achieve this, each metal mask step field is surrounded by a predefined frame (see Fig. 1.26 b), routing one etching potential on metal-1 level and the second etching potential on metal-2 level to reduce the risk of short-cuts between the etch networks [18]. The frames are connected to each other at the corners of the step field by metal structures placed in the scribe channel, i.e. the individual metal-level step fields actually overlap during the stepper-based lithography. The construction of these metal bridges must not affect the regular test structures in the scribe channel. Within the reticle, the individual etch contacts are connected to the metal frame. In order to have large contact pads for applying the etch potentials with spring-loaded contacts, a dedicated 'contact' step field (see Fig. 1.26 a, top of the wafer) is printed which has the same size as the other step fields. This is done on the second metal mask level using a special 'contact' reticle. In addition, a 'blank' reticle is used to remove the metal around the edges of the wafer in order to avoid short circuits in the etch network at the wafer edge. The described method requires three additional masks ('blank' reticle, 'contact' reticle and 'contact opening' reticle), which can, however, be reused if the reticle size from design to design is not changing. Besides exposing the wafer on the metal mask level with different reticles, no modification in the process flow is required.

### 1.3.3 Simulation of Circuitry and MEMS

Traditionally, MEMS and IC designers have used very different design tools. While IC designers rely on schematic-driven circuit simulators offered by the major electronic design automation (EDA) companies, such as Cadence [81], Mentor Graphics [82] and Synopsys [83], the MEMS designer typically relies on finite-element modeling (FEM) software, such as ANSYS [84], FEMLAB [85], CoventorWare [86], or IntelliSuite [87], for multi-domain analysis of their microstructures. In order to simulate and design integrated circuits based on a particular CMOS process, the CMOS foundries supply process-specific design kits, including design rules, process specifications, transistor-level models and analog and digital cell libraries, to support the major EDA tools. In order to simulate CMOS-based microsystems including micromechanical transducers and analog and digital circuitry, behavioral models for the transducer elements are required. To be compatible with the standard mixed-signal simulators delivered with common EDA packages (e.g. SPECTRE [81], ADVance MS [82], SABER [83]), these behavioral models must be expressed in an analog hardware description language (HDL), such as

Verilog-A or VHDL-A. The generation of such models for the transducers involving multiple signal domains from either the layout or the results of the FEM simulation is not straightforward. Simple lumped-element circuit models of the transducers might be developed manually on a case-by-case basis. For certain categories of microstructures (e.g. comb-drive resonators), the generation of macromodels is supported by academic [88, 89] and commercial tools [86, 90]. INTEGRATOR, developed by Coventor [86], is able to generate reduced-order macromodels of dynamic mechanical systems, consisting of spring, mass and damping elements, from detailed 3-D finite element (FEM) or boundary element (BEM) simulations for export in standard circuit simulators. NODAS, developed at Carnegie Mellon [88, 91, 92] is a library of parameterized components, including beams, plate masses, anchors, electrostatic comb drives and gaps, to simulate surface-micromachined MEMS structures using the SABER and SPECTRE simulators. Complex microstructures are build by interconnecting individual library elements. NODAS also has the ability to generate automatically the layout from the developed schematic.

Once the top-level layout of the integrated microsystem is completed, a design rule check (DRC) and a layout-versus-schematic (LVS) check are performed. In order to account for different design rules in the circuitry and the MEMS part, the standard design rule files supplied by the CMOS foundry might need to be extended (see Section 1.3.2). In addition, the standard extraction rules can be adapted in order to recognize and extract at least the electrical features of the transducer elements [93]. This allows the verification of the top-level design by comparison with the simulated top-level schematic and avoids, e.g., wiring errors. Some of the available tools also permit extraction of non-electric features [94].

More details on MEMS modeling in general and the extension of circuit simulation to include micromachined devices can be found in several books and overview articles [94–98].

## 1.4 CMOS and Micromachining

The integration of micromachining processes with CMOS technology can be accomplished in different ways. The additional process steps (or process modules) can either precede the standard CMOS process sequence (pre-CMOS) or they can be performed in between the regular CMOS steps (intra-CMOS) or after the completion of the CMOS process (post-CMOS) [99, 100]. In the case of post-CMOS micromachining, the microstructures are built from either the CMOS layers themselves or from additional layers deposited on top of the CMOS wafer. Tab. 1.4 summarizes various CMOS-based microsystem approaches found in the literature. Some of these approaches require several additional process modules, e.g. a pre-CMOS and a post-CMOS module; in these cases, we have categorized them by their first non-standard process sequence. The cited publications are exemplaric and the list provided is by no means considered to be all-inclusive.

**Tab. 1.4** CMOS-based microsystems using pre-, intra- or post-CMOS process modules to implement the microstructures

| | ***Surface micromachining*** | ***Bulk micromachining*** |
|---|---|---|
| **Pre-CMOS** process modules | **Sandia National Laboratories (*M³EMS*)** [101]<br>– Inertial sensors [102]<br>**UC Berkeley, Analog Devices, Raytheon and Sandia National Laboratories**<br>– Accelerometer [103]<br>**University Michigan**<br>– Accelerometer [104]<br>**Analog Devices, Palo Alto Research Center and UC Berkeley (*ModMEMS*)** [105]<br>– Inertial sensors [106]<br>**Analog Devices and UC Berkeley (*SOI-MEMS*)**<br>– Accelerometer [107, 108]<br>**Analog Devices and Clare (Optical iMEMS)**<br>– Optical switches [109]<br>**VTT Information Technologies and Micro Analog Systems** [110] | **MIT**<br>– Pressure sensor [111, 112]<br>**Univ. Michigan**<br>– Pressure sensor [113]<br>**Tohoku Univ.**<br>– Accelerometer [114]<br>– Pressure sensor [115]<br>**Fraunhofer Institute**<br>– Infrared radiation sensor [116]<br>**ETH Zurich**<br>– Vertical Hall sensor [47] |
| **Intra-CMOS** process modules | **Analog Devices (*iMEMS*)** [78, 117]<br>– Accelerometer [107, 118]<br>– Gyroscope [107, 119]<br>**Infineon Technologies (Siemens)**<br>– Pressure sensor [5, 120, 121]<br>– Accelerometer [122]<br>– Ultrasound transducers [123]<br>**Motorola** (now Freescale)<br>– Pressure sensor [124, 125]<br>**Fraunhofer Institute IMS**<br>– Pressure sensor [126–128]<br>**RWTH Aachen and Fraunhofer Institute IMS**<br>– Pressure sensor [129, 130]<br>**Univ. Duisburg, EPOS and Fraunhofer Institute IMS**<br>– Tactile sensor [131]<br>**Bosch**<br>– Accelerometer [132]<br>**Toyota**<br>– Pressure sensor [133, 134] | **Univ. Michigan**<br>– Pressure sensor [77, 136]<br>– Mass flow [77]<br>– Bioprobes [137, 138]<br>– Thermal converter [139]<br>– Infrared imager [140]<br>**LG Electronics Inst. of Technology and Seoul National Univ.**<br>– Accelerometer [141] |

**Tab. 1.4** (cont.)

| | *Surface micromachining* | *Bulk micromachining* |
|---|---|---|
| | **NEC**<br>– Infrared imager [135]<br>**IBM**<br>– Resonators [3]<br>– RF switches [3, 4] | |
| **Post-CMOS** micromachining of add-on layers | **UC Berkeley** [142, 143]<br>– Inertial sensors<br>– Resonators<br>**IMEC**<br>– Si/Ge MEMS [144]<br>**Stanford Univ.**<br>– Variable capacitors [75, 145]<br>**Texas Instruments**<br>– DMD [74, 146]<br>**Univ. Bremen and Infineon**<br>– Acceleration switch [147, 148]<br>**Delphi, General Motors and Univ. Michigan**<br>– Gyroscope [149–151]<br>**Honeywell**<br>– Thermal imager [152] | **austriamicrosystems**<br>– Accelerometer [153]<br>**ETH Zurich and Micronas**<br>– Pressure sensor [154] |
| **Post-CMOS** micromachining of CMOS layers | **ETH Zurich**<br>– Pressure sensor [155, 156]<br>– Fluid density sensor [157]<br>**TU Denmark**<br>– Resonators [158, 159] | **NEC**<br>– Pressure sensor [160]<br>**Bosch**<br>– Pressure sensor [161, 162]<br>**Motorola** (now Freescale)<br>– Pressure sensor [163]<br>**Silicon Microstructures**<br>– Pressure sensor [164]<br>**Toyota, Toyoda and Tohoku Univ.**<br>– Pressure [165]<br>**Toyota and Ritsumeikan Univ.**<br>– Infrared imager [166]<br>**Fraunhofer Institute and European Silicon Structures**<br>– Pressure sensor [167]<br>**Fraunhofer Institute, TU Berlin and Univ. Stuttgart**<br>– Pressure sensor [168] |

**Tab. 1.4** (cont.)

| *Surface micromachining* | *Bulk micromachining* |
|---|---|
| | **ETH Zurich** [17, 80]<br>– Chemical sensors [19, 169, 170]<br>– Thermal imager [22, 23, 171]<br>– Tactile sensor [172]<br>– Thermal converter [173]<br>– Proximity sensors [174]<br>– Flow sensor [175]<br>– Force sensors [176]<br>**Sensirion** [177]<br>– Flow sensor [178]<br>**Stanford Univ.** [179]<br>– Thermal converter [180]<br>– Vacuum sensor [181]<br>– Neural probes [182]<br>– Bandgap reference [183]<br>– Tactile sensor [184]<br>**Middle East TU**<br>– Infrared bolometer [185, 186]<br>– Thermopile [187]<br>**NIST and George Washington Univ.** [188]<br>– Gas sensor [189, 190]<br>– Accelerometer [190]<br>– Power sensor [191]<br>**UC Berkeley, George Washington Univ. and NIST**<br>– Accelerometer [192]<br>**Carnegie Mellon Univ.** [193, 194]<br>– Accelerometer [195]<br>– Gyroscope [196, 197]<br>– Microphone [198]<br>– Loudspeaker [199]<br>– Infrared imager pixel [200]<br>– Variable capacitor [201]<br>**Akustica** [202]<br>– Acoustic devices<br>**George Washington Univ., Naval Research Labs and Carnegie Mellon Univ.**<br>– Chemical sensor [203]<br>**MEMSIC** [204]<br>– Accelerometer [205] |

**Tab. 1.4** (cont.)

| *Surface micromachining* | *Bulk micromachining* |
|---|---|
| | **Univ. Michigan**<br>– Infrared sensor [206]<br>– Accelerometer [207]<br>**TU Berlin**<br>– Inkjet printhead [208]<br>**Toyohashi Univ.**<br>– Accelerometer [209]<br>**Univ. Twente**<br>– Microphone [210]<br>**Warwick Univ. and Univ. Cambridge**<br>– Gas sensor [211, 212]<br>**Seoul National Univ.**<br>– Pressure sensor [213]<br>**Daimler-Benz and Dialog Semiconductor**<br>– Accelerometer [214] |

Depending on the chosen integration path, a number of fabrication constraints are imposed on the micromachining steps in order not to deteriorate the performance of the CMOS electronics. An important example is the thermal budget allowed for the micromachining process steps. Polysilicon microstructures are deposited at temperatures between 575 and 625 °C in an LPCVD furnace and typically require thermal annealing at temperatures ≥900 °C to reduce residual stresses [215, 216]. However, after deposition of the aluminum metallization of a CMOS process, the maximum process temperature is limited to ≤450 °C in order not to degrade the aluminum-silicon contacts. Therefore, polysilicon cannot be deposited after the completion of a CMOS process with standard aluminum metallization. In order to enable the deposition of polysilicon microstructures *after* the completion of the CMOS process sequence, an alternative high-temperature stable metallization, such as tungsten, must be used for the CMOS process [61, 142]. Considering that IC manufacturers have invested enormous resources into the development of reliable, multi-level aluminum interconnect technologies, and further considering the inferior resistivity of tungsten versus aluminum, it seems unlikely that such a process would be adopted in industry. Alternatively, the standard polysilicon gate material of the CMOS process is used as well for the microstructures or an additional structural polysilicon layer is deposited and structured *before* the standard CMOS metallization is applied. In this approach, the regular CMOS process sequence is interrupted before the metal deposition, a dedicated micromachining module is inserted and then the CMOS process sequence resumes with the back-end aluminum interconnect technology. This intra-CMOS approach mini-

mizes performance degradations for both electronic and mechanical components, but requires interruption of the CMOS process sequence and, more critical, the need to return CMOS wafers into a CMOS line after performing non-standard process steps. As a result, this fabrication approach for CMOS-integrated polysilicon microstructures has been commercialized by companies with in-house CMOS or BiCMOS fabrication facilities (e.g. Analog Devices [78, 107, 118] and Infineon [5, 120]).

### 1.4.1 Pre-CMOS Micromachining

Pre-CMOS micromachining or 'MEMS-first' fabrication approaches avoid thermal budget constraints during the MEMS fabrication. In this way, e.g. thick polysilicon microstructures requiring stress relief anneals at temperatures up to 1100 °C can be co-integrated with CMOS circuitry. Typically, the MEMS structures are buried and sealed during the initial process module. After the wafer surface is planarized, the pre-processed wafers with embedded MEMS structures are used as starting material for the subsequent CMOS process. Challenges include the surface planarization required for the subsequent CMOS process and the interconnections between MEMS and circuitry areas.

The $M^3$EMS (Modular, Monolithic MicroElectroMechanical Systems) technology developed at Sandia National Laboratories was one of the first demonstrations of the MEMS-first integration concept [61, 101]. In this approach, the multi-layer polysilicon microstructure is built in a trench, which has been etched into the bulk silicon using an anisotropic wet silicon etchant. After formation of the polysilicon microstructures, the trench is refilled with LPCVD oxide and planarized with a CMP (chemical mechanical polishing) step. Subsequently, the wafers with embedded microstructures are used as starting material in an unmodified CMOS process, fabricating CMOS circuitry in areas adjacent to the MEMS areas. The CMOS metallization is used to interconnect circuitry and MEMS areas. The back-end of the process requires additional masks to open the protective silicon nitride cap over the MEMS areas prior to the release of the polysilicon structures by silicon oxide sacrificial layer etching. A cross-section of the $M^3$EMS technology used for the fabrication of inertial sensors [102] is shown in Fig. 1.15 a. Theoretically, the planarized wafer with embedded MEMS structures can serve as starting material for any microelectronics foundry service, since the technology does not require significant modifications of the CMOS process sequence [102]. Of course, the pre-processed starting material requires stringent qualification by the CMOS foundry in order not to compromise their process yield. A resonant accelerometer fabricated with Sandia's $M^3$EMS technology has been reported in [103]. Researchers at the University of Michigan have developed a similar trench-based MEMS-first technology to co-integrate polysilicon microstructures with a 3 μm CMOS technology [104].

Recently, an alternative pre-CMOS MEMS process called *Mod MEMS* has been demonstrated by Analog Devices, Palo Alto Research Center and UC Berkeley

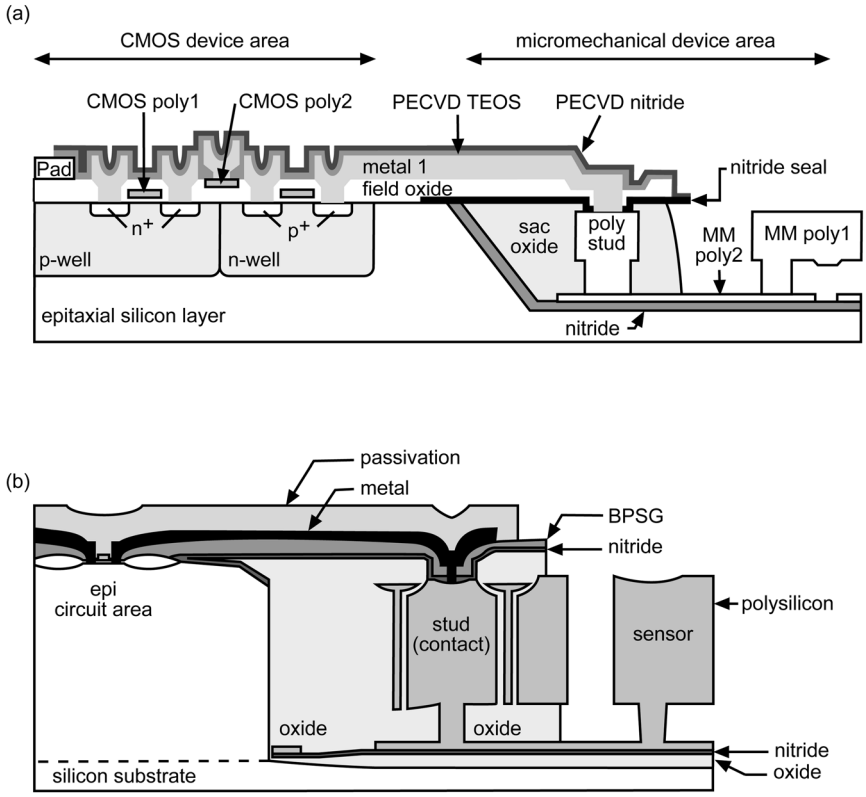


**Fig. 1.15** Schematic cross-section of two pre-CMOS MEMS processes for fabrication of monolithically integrated polysilicon microstructures: (a) $M^3$EMS technology by Sandia National Laboratories. Adapted from [101]. (b) Mod MEMS technology by Analog Devices, Palo Alto Research Center and UC Berkeley. Adapted from [105]

[105]. Mod MEMS enables the integration of 5–10 µm thick polysilicon MEMS devices with sub-µm CMOS circuitry. In contrast to the Sandia approach, the thick polysilicon structures are build on top of the silicon substrate and not in an etched trench (see Fig. 1.15 b). An 1100 °C anneal ensures nearly stress-free polysilicon layers with very small stress gradients [105], which is especially important for thick polysilicon microstructures. The intra-CMOS approach used by Analog Devices for the fabrication of their ADXL and ADXRS series inertial sensors (see Section 1.4.2) does not allow such high annealing temperatures and thus limits the thickness of the structural polysilicon layer. After forming isolation trenches to provide electrical isolation between MEMS regions at different potential, a 2 µm capping oxide/nitride sandwich is deposited on the polysilicon, the MEMS structural regions are defined by a polysilicon etch step and the sidewalls of the MEMS regions are passivated by a thermal oxidation. Next, a selective epitaxial silicon growth process is used to provide planarization around the thick MEMS

structures. With the polysilicon structures encapsulated with a silicon oxide layer, the epitaxial silicon layer only grows in the wafer regions surrounding the MEMS regions. After the selective epi process, the wafer surface is planarized with a CMP process and a seal layer sandwich is deposited and patterned to protect the MEMS areas during the CMOS process. At this point, the wafers are ready for standard CMOS or BiCMOS processing. The CMOS circuitry is formed in the grown epi regions with only a 12 μm exclusion zone between MEMS and active circuitry. Similar to the Sandia $M^3$EMS process, the CMOS metallization connects the polysilicon microstructures with the circuitry. After completion of the IC process, the MEMS areas are opened up, the thick polysilicon layer is structured with an anisotropic dry etching step and the microstructures are released by sacrificial oxide etching. The feasibility of this pre-CMOS MEMS approach has been demonstrated by successfully fabricating integrated accelerometers and gyroscopes [105, 106]. Similar to the $M^3$EMS process, the Mod MEMS process can be used in conjunction with various IC foundry processes as long as the starting material can be qualified for the particular IC process.

Single-crystalline silicon microstructures can be implemented in a pre-CMOS fabrication approach using either SOI (silicon-on-insulator) wafers as substrate material [107–110] or by incorporating sealed cavities using wafer bonding [111, 112].

Originally demonstrated at UC Berkeley [108], the SOIMEMS technology has been further developed by Analog Devices as a next-generation process for the monolithic integration of inertial sensors. Compared with Analog Devices' current high-volume iMEMS technology (see Section 1.4.2), SOIMEMS offers thicker structural layers (10 μm instead of 4 μm), yielding more robust sensor structures, and a more advanced BiCMOS technology (0.6 μm instead of 3.0 μm minimal feature sizes) enabling more on-chip functionality. A cross-section of the SOIMEMS technology is depicted in Fig. 1.16a [107, 108]. The fabrication process comprises both a pre-CMOS (trench isolation) and a post-CMOS (microstructure definition and release) fabrication module, but has the advantage that all of the circuit processing is done in one process module [107]. The fabrication process starts with etching trenches in the SOI wafers (having a 10 μm device layer) to establish isolated areas on the wafer [108, 217]. The DRIE trench etching stops on the buried oxide layer of the SOI substrates. After trench refill and surface planarization, the regular 0.6 μm BiCMOS process sequence is executed. Interconnects between circuitry and microstructures are established with the standard IC metallization. After completion of the BiCMOS process sequence, the structural regions are cleared from all dielectrics and the microstructures are defined using a DRIE trench etching step. Finally, the microstructures are released by etching the buried oxide layer underneath them using a hydrofluoric acid based etch. Temporary photoresist pedestals prevent the structures from collapsing during drying [107]. First commercial acceleration sensors (ADXL40) based on Analog Devices' SOIMEMS technology are expected to be launched in 2004 [107].

The basic SOIMEMS technology developed by Analog Devices has been extended to co-integrate electrostatic optical switches with on-chip electronics [109]. The re-

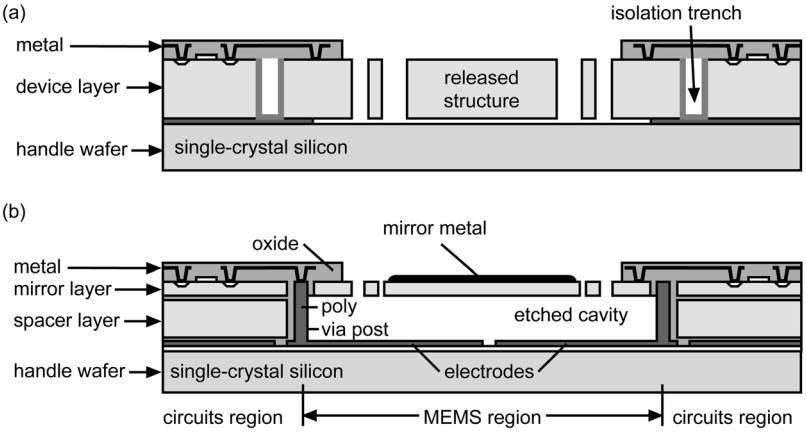


**Fig. 1.16** Cross-sections of SOI-based integrated MEMS technologies by Analog Devices: (a) SOIMEMS with 10 μm device layer for fabrication of single-crystalline silicon inertial sensors. Adapted from [107]. (b) Optical iMEMS based on triple-stack substrate for fabrication of integrated optical switches. Adapted from [109]

sulting 'Optical iMEMS' technology uses a three-layer silicon stack as substrate material (see Fig. 1.16 b). The custom-made triple-stack substrate consists of a 10 μm thick mirror layer on top of a sacrificial spacer layer (10–80 μm thick), which is connected to the handle wafer. A patterned polysilicon layer embedded between two dielectric layers forms the electrode structures for mirror actuation between the silicon spacer layer and handle wafer. Trenches are etched using DRIE to contact the buried polysilicon layer and to achieve device isolation. After surface planarization, the preprocessed wafers enter a 3 μm high-voltage CMOS process provided by Clare for on-chip circuit fabrication. The circuitry provides 200 V high-voltage transistors for mirror actuation and 10 V CMOS for the position sense electronics [109]. After completion of the circuit process, the MEMS area is cleared from all circuit dielectrics and the mirror structures are defined in the mirror layer by DRIE. The mirrors are finally released by etching the spacer silicon layer underneath the mirror with xenon difluoride, $XeF_2$. During this etch, the mirrors themselves are protected using photoresist and silicon oxide layers. Process details can be found in [109].

An alternative SOI-based technology for the monolithic integration of CMOS electronics with MEMS has been demonstrated by VTT Information Technology and Micro Analog Systems [110]. In a pre-CMOS fabrication module, vacuum cavities are formed in defined regions of the buried oxide. The so-called 'plug-up' process sequence consists of (i) DRIE trench etching of micron-sized access holes into the device layer, (ii) deposition of a semipermeable polysilicon layer, (iii) local removal of the buried oxide through the pinholes of the polysilicon layer, thus releasing the microstructures, (iv) plugging of the access holes by conformal LPCVD polysilicon deposition at reduced pressure and finally (v) surface planarization to prepare the wafers for IC processing [110]. The pre-CMOS process se-

quence can be complemented by isolation trenches and substrate contacts and is followed by a 1 μm CMOS process based on molybdenum gates.

A pre-CMOS approach using wafer bonding to incorporate sealed cavities has been developed at MIT [111, 112]. The cavities are etched into a handle wafer and sealed by silicon fusion bonding the device wafer on to the handle wafer. The device wafer is subsequently thinned to the desired thickness. In [111], the device wafer is an epi-wafer and a combination of grinding, polishing and anisotropic wet etching with electrochemical etch-stop is used to thin the wafer down to the epitaxial layer. In this way, sealed cavities bound by membranes with uniform thickness are formed. Subsequently, the pre-processed wafers are run through a 1.75 μm twin-well CMOS process. After completion of the CMOS process sequence, post-CMOS micromachining steps can be used to access the sealed cavities by dry etching from the wafer front or anisotropic wet etching from the wafer back [111]. The technology has been successfully demonstrated by fabricating piezoresistive pressure sensors with circular membranes [111]. The fabrication of complex microstructures by combining silicon fusion bonding and DRIE has been described in [218].

A number of CMOS-based MEMS processes fabricate the on-chip circuitry in recessed cavities anisotropically etched into the silicon wafers prior to the CMOS process sequence [113–115]. In this way, the front side of the sensor wafers with integrated transducer elements and circuitry can be (anodically) bonded to constraint (glass) wafers. The approach facilitates the fabrication of capacitive sensor structures having counter electrodes on the glass wafer and provides a zero-level packaging for the integrated microsystems.

Silicon trench etching and polysilicon refill have become a standard isolation technology in CMOS processes. A similar trench technology has been used to define the active area of a vertical Hall plate [47]. After sidewall implantation of the vertical Hall plate, the trenches are isolated with a silicon oxide layer and refilled with polysilicon. After surface planarization, the silicon wafers with embedded Hall plates are processed using an unmodified CMOS process, providing sensor contacts, interconnects and read-out circuitry. The resulting vertical Hall sensors are sensitive to magnetic fields in the chip surface. The Hall plates are geometrically well defined by the pre-CMOS trench technology and decoupled from the substrate by a reverse biased p–n junction at the bottom of the trenches. The combination of the trench technology with either SOI substrates or silicon wet etching removes the p–n junction at the bottom of the trenches, yielding dielectrically isolated vertical Hall devices [219].

### 1.4.2 Intra-CMOS Micromachining

Intermediate micromachining is most commonly used to integrate polysilicon microstructures in CMOS/BiCMOS process technologies. Inserting the micromachining process steps before the back-end interconnect metallization ensures process compatibility with the polysilicon deposition and anneal. The polysilicon annealing

temperature is typically limited to about 900 °C in order not to affect the doping profiles of the CMOS process. Alternative post-CMOS approaches [142] require modified interconnect metallizations based on, e.g., tungsten to achieve the necessary high-temperature stability for the subsequent polysilicon deposition and anneal.

Commercially available examples of polysilicon microstructures, fabricated with CMOS/BiCMOS processes with intermediate micromachining, include Analog Devices ADXL series accelerometers and ADXRS series gyroscopes [220], Infineon Technologies' KP100 series pressure sensors [42] and Freescale's (Motorola) MPXY8000 series pressure sensors [221]. Not surprisingly, all three companies have in-house IC processing capabilities, facilitating the chosen interleaved process sequences and allowing fine-tuning of the overall process sequence to minimize degradation in both electronic and mechanical components. Business models based on complete outsourcing of the microsystem fabrication will be very unlikely able to use CMOS processes with intermediate micromachining, because a CMOS foundry will probably not accept wafers back into their line after a number of micromachining steps have been performed elsewhere.

In the following, we will briefly highlight the process technologies developed by Analog Devices and Infineon Technologies to fabricate integrated polysilicon microstructures.

Analog Devices employs a 24 V capable 3 μm BiCMOS process with trimable thin-film resistors for the fabrication of their integrated accelerometers and gyroscopes ([119], see also Chapter 3). Surface-micromachined polysilicon structures with a thickness of 2–4 μm are formed within a micromachining module inserted into the process sequence before the BiCMOS back-end interconnect metallization. An early version of the process [78, 96] for integrated acceleration sensors used 24 masks, including 13 for the electronics and 11 for the mechanical structure and the interconnects to the electronics. A cross-section illustration of Analog Devices' integrated MEMS technology is shown in Fig. 1.17. The fabrication starts with the front end of the BiCMOS technology, creating n-wells, sources, drains and polysilicon gates for the MOS transistors and bases and emitters for the bipolar transistors. In the course of the front-end circuit process, diffused $n^+$-runners to connect the capacitive microstructures to the on-chip electronics and $n^+$ ground plane regions are formed. After transistor fabrication, the circuit areas are covered with an LPCVD nitride layer and a BPSG (borophosphosilicate glass) layer and the sensor regions are cleared from all dielectrics down to the gate oxide. Subsequently another LPCVD nitride layer is deposited and patterned, which will later serve as an etch-stop layer during the sensor release etch. Next, the 1.6 μm sacrificial oxide layer and the 2 μm structural polysilicon are successively deposited and patterned. The polysilicon layer is doped by a phosphorus implantation and annealed, targeting a slightly tensile final stress in order to prevent microstructure warping or buckling. After depositing an additional thin oxide over the wafer and removing this oxide and the sacrificial oxide in the circuit areas, the BiCMOS process sequence is resumed with the back-end interconnect formation. Finally, a passivation layer sandwich consisting of a PECVD oxide and nitride film are deposited and patterned and the inertial sensors are released on a wafer level by sa-

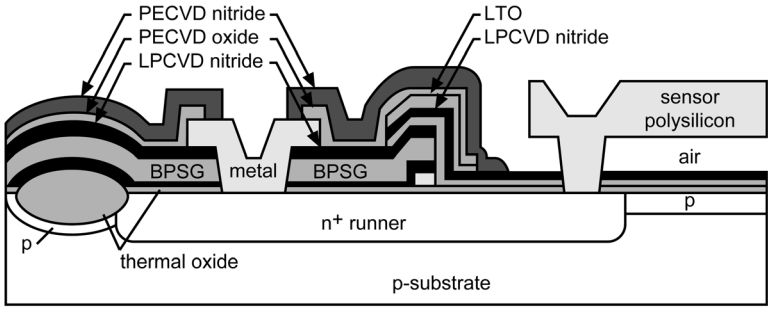


**Fig. 1.17** Schematic cross-section of Analog Devices' integrated MEMS technology with an $n^+$-diffusion interconnect structure between polysilicon microstructure and on-chip electronics. Adapted from [78]

crificial oxide etching. During the release and subsequent drying step, temporary photoresist pedestals prevent the microstructures from collapsing. After sensor release, the sensors are tested and the on-chip SiCr resistors are trimmed, followed by dicing, die and wire bonding and application of an antistiction coating. During wafer sawing from the back of the wafer, the released mechanical elements are protected by two layers of tape (with recessed cavities) on the front side of the wafer. Details on these non-standard packaging process steps can be found in [107, 117]. More recent iMEMS versions use polysilicon ground planes, thicker 2 μm sacrificial oxide layers and thicker 4 μm structural polysilicon layers [107].

In contrast to Analog Devices, Infineon Technologies uses the standard capacitor polysilicon layer of a 0.8 μm BiCMOS process as mechanical layer for their pressure sensors ([5, 120]; see also Chapter 6). Obviously, the rather small pressure sensors with a diameter of 70 μm are less sensitive to residual stress within the polysilicon layer and do not require a dedicated low-stress polysilicon structural layer. A schematic cross-section of the surface-micromachined pressure sensors are shown in Fig. 1.18. The standard process sequence of the 16-mask BiCMOS process is stopped before the back-end interconnect metallization to insert a single-mask micromachining module. The basic pressure sensor structure is formed within the course of the BiCMOS process sequence. The lower electrode is made from the n-well, the 600 nm field oxide serves as sacrificial layer and the 400 nm capacitor polysilicon as structural layer and top electrode [5, 120]. Within the micromachining module, the polysilicon membranes are released by sacrificial layer etching and the cavities are sealed. After perforating the membranes in a dry etching step, the oxide sacrificial layer is etched using vapor HF through these holes. Finally, the resulting cavities are sealed with a process optimized for the vertical etch channels, yielding a typical cavity pressure of 300 mbar [120]. After completion of the micromachining module, the regular BiCMOS back-end process is employed to form the aluminum interconnects and passivate the microsystem. The final pad etch is used to open the contact pads and form the oxide boss structures on the pressure sensors.

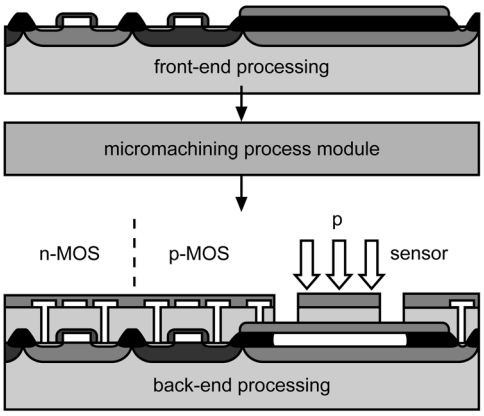


**Fig. 1.18** Schematic cross-section of Infineons' integrated MEMS technology for the fabrication of pressure sensors. Adapted from [120]

In addition to the processes by Analog Devices and Infineon, substantial work has been invested at the Technical University of Aachen and the Fraunhofer Institute IMS in the development of a monolithically integrated capacitive pressure sensor technology [126]. The underlying CMOS process remains unchanged until the source/drain implantation. The $n^+$ implantation is used as one electrode for the capacitive pressure sensors. After drain/source implantation, the pressure sensors are formed by depositing a thin silicon nitride insulation layer, depositing and patterning a sacrificial oxide layer, and finally the polysilicon structural layer. After releasing the polysilicon membranes by a hydrofluoric acid etch, the cavities are sealed with an LPCVD oxide layer, which also serves as the contact oxide for the metallization. Subsequently, the CMOS process is completed with the metallization and passivation. The pressure sensor consists of an array of polysilicon membranes connected in parallel. Different pressure ranges can be covered by adjusting the membrane diameter from 25 to 125 µm [127]. Recently, the capacitive sensor technology has been combined with a CMOS technology on SIMOX (Separation by IMplantation of OXygen) substrates for high-temperature applications up to 250 °C [130]. The pressure sensor is insulated towards the substrate by a thin silicon nitride layer deposited before the sacrificial oxide. The developed capacitive pressure sensor technology has been employed for, e.g., catheter flow sensors [129], intraocular pressure sensor implants [128] and tactile sensors [131].

In order to minimize the influence of the structural polysilicon deposition and anneal on the doping profiles of the CMOS process, the structural polysilicon should be deposited as early as possible in the process sequence (see, e.g., MEMS-first approaches in Section 1.4.1). A unique approach to integrate thick polysilicon layers in a BiCMOS technology has been proposed by Bosch and the Fraunhofer Institute ISiT [132] for the fabrication of a surface-micromachined accelerometer. After the definition of the buried layer, a sacrificial oxide sandwich consisting of an oxide and a LPCVD polysilicon layer is deposited and patterned to define the sensor areas. Subsequently, the BiCMOS process is continued with the deposition of the epitaxial silicon layer in the circuit areas. At the same, a thick polycrystal-

line silicon layer (epi-poly) is grown in the sensor areas with the LPCVD polysilicon layer acting as nucleation layer. The 10 µm thick epi-poly is grown at high temperatures and exhibits almost ideal mechanical properties [132]. In a later process stage, the epi-poly layer is doped together with the gate polysilicon of the BiCMOS process. After completion of the BiCMOS process metallization and passivation, the epi-poly is patterned and the sacrificial oxide layer etched with vapor HF to release the accelerometer structure. The accelerometer structure is electrically contacted through the buried layer.

All processes described so far relied on a polysilicon structural layer and sacrificial oxide etching. A 1K-element pressure sensor array based on a sacrificial polysilicon layer has been developed by Toyota Central R&D Laboratories [133, 134]. The micromachining module for the sensor fabrication is inserted into the CMOS process flow after source/drain implantation. The MEMS module consists of deposition and patterning of a silicon nitride base layer to protect the silicon substrate, a polysilicon sacrificial layer, followed by the membrane sandwich consisting of silicon nitride top and bottom layer with a polysilicon sensing layer in between. The sacrificial layer is etched using a KOH solution through etch holes located at the edges of the 50×50 µm membranes [133, 134]. Finally, the back-end of the CMOS process is performed and the released cavities are sealed using a PECVD silicon nitride film. The pressure sensor array features piezoresistive pressure sensing using the polysilicon piezoresistors embedded in the silicon nitride membrane (see Fig. 1.19). The array has been used for high-resolution tactile imaging [133, 134].

Using a sacrificial polysilicon layer as well, a monolithic infrared focal plane array has been developed at NEC [135]. The sensor array with a pixel pitch of 50 µm is based on titanium bolometer structures embedded in silicon dioxide suspended plates. The devices are fabricated by inserting a micromachining module consist-

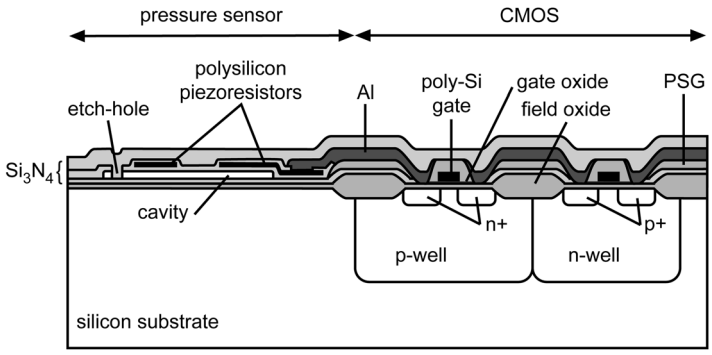


**Fig. 1.19** Schematic cross-section of surface-micromachined pressure sensor element developed at Toyota Central R&D Laboratories for use in tactile imagers. Adapted from [133]. The silicon nitride membrane structure with embedded polysilicon piezoresistors is formed in an intra-CMOS process module and released by etching a sacrificial polysilicon layer

ing of several silicon dioxide and metal deposition and patterning steps after the source/drain implantation of the CMOS process [135].

Researchers at IBM's T. J. Watson Research Center have recently incorporated r.f. switches and resonators into the copper-based interconnect technology of state-of-the-art CMOS processes [3, 4]. Certain adaptations had to be made to the standard copper (dual)-damascene process sequence [222] used by IBM for interconnect formation in order to (i) encapsulate the copper and, thus, prevent its oxidation, (ii) introduce suitable contact materials for the switches and (iii) provide a sacrificial layer for copper microstructure release. The microstructures are released by removing an organic sacrificial layer in an oxygen plasma. All required dielectric films are produced using PECVD at temperatures of 400 °C or less and all metal films are deposited by sputtering or a combination of sputtering and electroplating [3].

Bulk micromachining using wet anisotropic silicon etchants in combination with $p^{++}$ etch-stop techniques have been used by Wise and co-workers at the University of Michigan for the fabrication of CMOS-based mass-flow sensors [77], pressure sensors [77, 136], microelectrode recording arrays [137, 138], thermal converters [139] and infrared sensors [140]. The microsystems are fabricated using a modified p-well CMOS process. The highly p-doped regions are diffused into the silicon substrate wafer after the CMOS p-well implantation. The p-well implant dose had to be modified from the baseline CMOS process to account for the additional p-well oxidation and boron segregation into the masking oxide in the merged process [77, 137]. The p- well drive-in is accomplished simultaneously with the $p^{++}$ diffusion. Using a 16 h

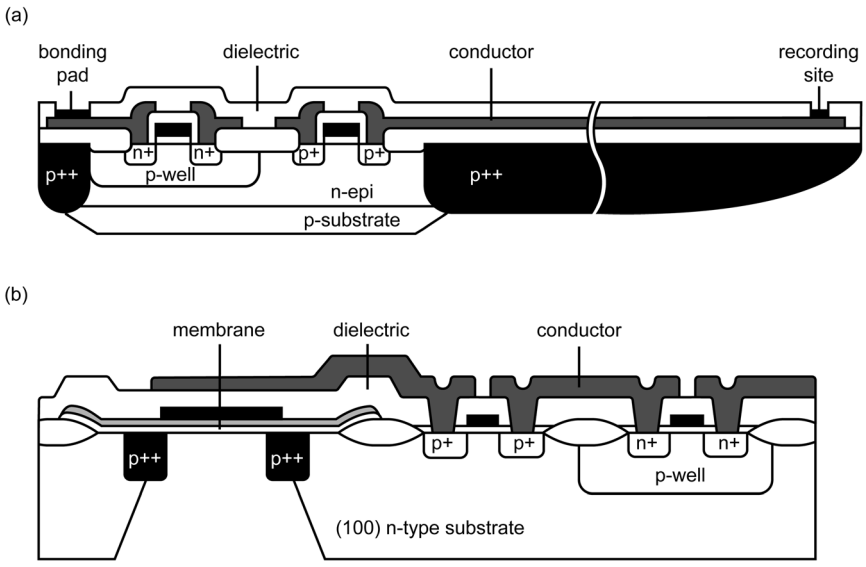


**Fig. 1.20** Schematic cross-section of (a) needle probe (adapted from [137]) and (b) mass flow sensor (adapted from [77]) developed at the University of Michigan; diffused $p^{++}$-regions are used as etch-stop layers during the microstructure release by anisotropic wet etching

diffusion at 1175 °C, rim and p-well depths of 15 and 5 μm are obtained, respectively. If required, an additional shallow $p^{++}$ diffusion is implemented. The $p^{++}$ regions define (a) the lateral dimensions of dielectric membranes by providing a non-etched $p^{++}$ rim around them and (b) the thickness of silicon microstructures, e.g. membranes for pressure sensors or shafts for needle probes, by the depth of the diffusion (see Fig. 1.20). Depending on the actual microsystem, additional process modifications to the CMOS baseline, such as special dielectric layers [77] or metallizations [137], have been incorporated. The microstructures are released after completion of the CMOS process sequence with the $p^{++}$ regions providing an intrinsic etch-stop. In the early 1990s, a number of impressive CMOS-based microsystems were realized based on this process, including a multi-sensor chip comprising six different sensor types and their electronics [77].

### 1.4.3 Post-CMOS Micromachining

Probably the greatest advantage of post-CMOS micromachining approaches is that the fabrication can be completely outsourced. After completion of the regular CMOS process sequence, which can, in principle, be performed at any CMOS foundry, the post-CMOS micromachining steps can be done at a dedicated MEMS foundry. The price to pay for this fabrication flexibility is the stringent thermal budget for all process steps following standard CMOS technologies with aluminum metallizations. A maximum process temperature of $\sim 450$ °C excludes high-temperature deposition and annealing steps, such as polysilicon deposition in an LPCVD furnace. PECVD processes, sputtering, electroplating and most wet and dry bulk and surface micromachining processes are, however, well suited for the post-CMOS approach. During the micromachining etching/release step the CMOS electronics might require special protection.

Basically, one can distinguish two general post-CMOS micromachining approaches: the microstructures either are formed by machining the CMOS layers themselves or by building the complete microstructures on top of the CMOS substrate. In the first approach, most of the microstructure is already formed within the regular process sequence. In this case, the post-CMOS process module typically requires very few process steps, such as an etching step to release the microstructure or an additional deposition step. Building the complete MEMS on top of the CMOS substrate might require more process steps but can save valuable real estate, because the MEMS part can be build directly on top of the CMOS circuitry. In the following, we will provide examples for both fabrication approaches.

#### 1.4.3.1 Post-CMOS Micromachining of Add-on Layers

Building the MEMS on top of a CMOS substrate, most processes in this category use surface micromachining techniques and in particular sacrificial layer etching to release the microstructures. Based on the required process temperatures, one can distinguish two basic categories of post-CMOS add-on micromachining mod-

ules: (i) low-temperature modules with process temperatures up to ~ 100–150 °C, which are typically based on PVD (physical vapor deposition) or electroplating of metal layers and use polymers or metals as sacrificial layers, and (ii) medium-temperature modules requiring process temperatures over 300 °C, which are often based on CVD (chemical vapor deposition) processes for the structural and the sacrificial layers.

Crucial for all add-on surface micromachining modules is a good planarity of the underlying CMOS substrate and both good electrical and mechanical contact between the microstructures and the CMOS circuit. The on-chip circuitry can either surround the MEMS or be located underneath the microstructures, saving valuable CMOS real estate.

Because of its desirable mechanical properties, the integration of polysilicon microstructures after the completion of a CMOS process was studied carefully in the early 1990s [142]. The LPCVD deposition and stress-relief anneal of thin polysilicon films require process temperatures of ~600 and ≥900 °C, respectively, which are not compatible with the standard aluminum (or copper) metallization used in most of today's CMOS processes. To accommodate the required high-temperature post-processing module, modifications to a baseline CMOS process were made at the metallization and passivation level only [142]. Metal–silicon contacts use a high-temperature stable titanium silicide and titanium nitride barrier metallurgy and a tungsten metallization for circuit interconnect. The passivation layer should planarize the wafer surface and protect the underlying circuitry not only from the environment but also from the hydrofluoric acid used to release the microstructures. To this end, a passivation layer consisting of a sandwich of LPCVD phosphosilicate glass (PSG, for surface planarization) and low-stress LPCVD silicon nitride (for HF protection) has been chosen. The subsequent micromachining module consisting of a ground-plane polysilicon (SP1) and two structural polysilicon layers (SP2 and SP3, see Fig. 1.21 a) requires nine additional lithography steps. Polysilicon–polysilicon interconnects are used between circuitry and microstructure. The process sequence is described in detail in [142]. To minimize the effect of the high-temperature steps on the circuit characteristics, both the PSG densification and the polysilicon stress-relief anneal are done by RTA (rapid thermal anneal) steps at 900 °C. Additional high-temperature steps include the LPCVD nitride (835 °C) and the polysilicon (610 °C) depositions. A slight shift of the transistor characteristics could be observed, indicating a doping redistribution during the high-temperature post-processing steps.

To avoid doping redistribution and the need for high-temperature stable interconnect metallizations, the post-processing temperature must be reduced to below ~ 500 °C [79]. To achieve this, polycrystalline silicon–germanium films have been investigated recently [143, 144, 223] as an alternative to polysilicon films. Depending on the germanium concentration and the deposition pressure, polycrystalline Si–Ge films can be deposited at temperatures of 450 °C or even lower, making the process compatible with a standard CMOS aluminum metallization. The poly-SiGe films are deposited in either an LPCVD furnace [143, 223] or a PECVD system [144], with the latter method showing increased deposition rates. In [143], two post-CMOS micromachining approaches for the co-integration of poly-SiGe microstructures with

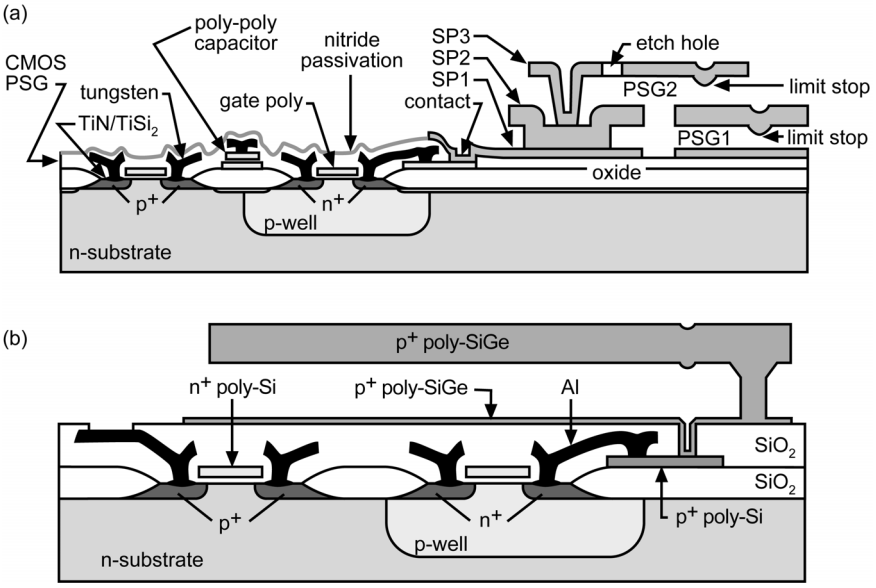


**Fig. 1.21** Schematic cross-sections of (a) polysilicon and (b) polycrystalline silicon germanium (poly-SiGe) microstructures fabricated by post-CMOS surface micromachining techniques on top of a completed CMOS substrate wafer. Both fabrication processes were developed at the University of California at Berkeley. Adapted from [142] and [143]

CMOS circuitry are investigated: the first approach uses n-type poly-Ge deposited at 400 °C as structural layer and $SiO_2$ as sacrificial layer, the second approach p-type poly-$Si_{0.35}Ge_{0.65}$ as structural layer and poly-Ge as sacrificial layer (see schematic in Fig. 1.21 b). Whereas the first approach requires a special CMOS passivation to protect the circuitry during the microstructure release, the second approach uses hydrogen peroxide for sacrificial layer etching and no special layers are needed to protect CMOS metallization and dielectric layers. Similarly to the earlier poly-Si technology [142], a polysilicon–polysilicon contact connects the MEMS to the circuitry. Even though the deposited poly-$Si_{0.35}Ge_{0.65}$ films already exhibit a relatively low as-deposited stress of only –10 MPa, it is expected that the film properties can be improved for MEMS applications with further optimization of deposition and annealing parameters [143, 223], making poly-SiGe a promising candidate for post-CMOS integration of MEMS.

The use of PVD techniques for film deposition can further lower the processing temperatures of post-CMOS micromachining modules. Silicon films sputter-deposited at room temperature using a DC magnetron sputter system have been deposited on both polyimide and silicon dioxide sacrificial layers for MEMS applications [145]. After 3 h anneal in forming gas at 350 °C, films with a thickness of 2 and 5 µm showed residual tensile stress of the order of 70 MPa. A drawback of the sputtered silicon films are very high sheet resistances in the MΩ/sq. range before annealing and in the GΩ/sq. range after the 350 °C anneal. Cladding the

structural silicon layer with two 50 nm thick TiW layers resulted in a decreased electrical resistivity of 25 Ω/sq. To prove the CMOS compatibility of this approach, integrated variable capacitors have been fabricated in a post-CMOS approach using the TiW-clad sputtered silicon process [145]. The microstructures have been released by dry etching the polyimide sacrificial layer in an oxygen plasma.

A commercial example of a metal-based MEMS fabricated on top of a CMOS substrate using low-temperature processes only is the DMD (digital micromirror device) developed by Texas Instruments [74, 146]. The DMD, an array of electrostatically actuated torsional micromirrors (used as light switches), creates the image in DLP-based (digital light processing) projection displays. The mechanical structure of a DMD pixel consists of alternating layers of patterned aluminum and air gaps and is built on top of a CMOS static random-access memory (SRAM) cell using surface-micromachining techniques. After completion of the 0.8 μm double-metal CMOS process, the final dielectric layer is planarized using CMP and vias are generated for interconnecting the mirror with the underlying circuitry [146]. As can be imagined, the surface planarization throughout the MEMS process is crucial, as non-uniformities in the mirror surface would result in non-tolerable contrast changes on the final picture. The formation of the 16×16 μm micromirror superstructure requires six additional photolithographic steps to define four aluminum layers and two sacrificial photoresist layers (see schematic in Fig. 1.22). The four aluminum layers are used to fabricate (1) the yoke address electrodes and the bias/reset bus, (2) the torsional hinges, (3) the

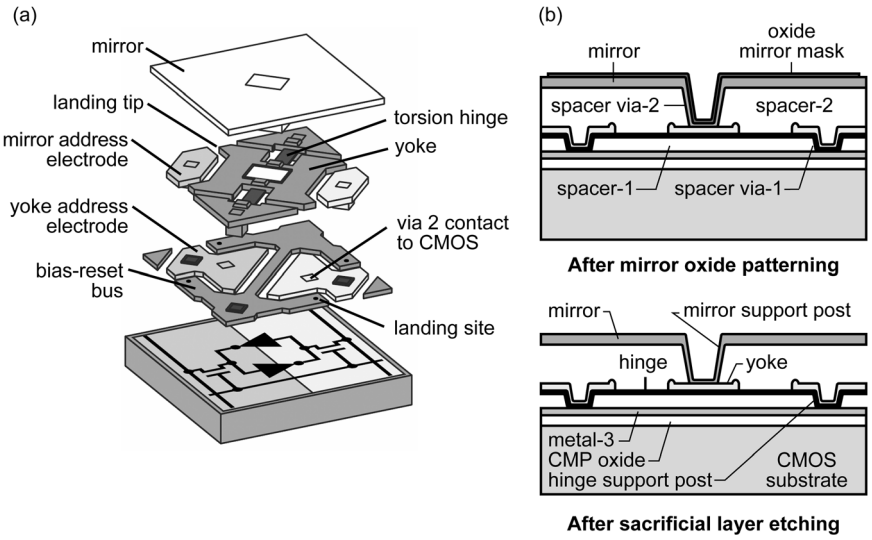


**Fig. 1.22** (a) Schematic of the DMD superstructure consisting of four aluminum layers and two sacrificial polymer layers on top of a CMOS SRAM cell. Adapted from [146]. (b) Cross- section of DMD superstructure before and after release by polymer sacrificial layer etching. Adapted from [74]

mirror address electrodes, yoke and hinge support posts and (4) the actual mirror. The aluminum layers are sputter-deposited and the final mirror superstructures are released by etching the polymer sacrificial layer in a plasma etcher. Finally, an antistiction coating is applied to prevent stiction of the micromirrors to the landing pads during operation. The fabrication and packaging process have been described in detail in [74, 146].

Thicker metal structures can be achieved by electroplating techniques. Examples of electroplated microstructures on top of CMOS substrates include a gold acceleration threshold switch developed by Infineon and the University of Bremen ([147, 148], see Fig. 1.23 a) and a nickel ring gyroscope developed by Delphi-Delco Electronics, General Motors and the University of Michigan at Ann Arbor ([149–151], see Fig. 1.23 b). In the following, the fabrication process of the acceleration switch is briefly highlighted. After completion of the CMOS process, a thin sacrificial photoresist layer is spun-on and patterned for electrical and mechanical contacts between microstructure and circuitry. Subsequently a titanium/gold seed layer is sputtered on the wafer and a thick photoresist plating mold is spun-on and patterned. Finally, gold is electroplated into the photoresist plating mold and the microstructures are released by removing plating mold, seed layer and sacrificial photoresist layer. The post-CMOS fabrication process has been described in detail in [147].

The electroplated ring gyroscope is fabricated using a similar post-CMOS fabrication sequence [149, 150]. An early post-CMOS process sequence [224, 225] is summarized in the following (see cross-section in Fig. 1.24). After completion of the CMOS process, the aluminum metallization is passivated using a LTO (low-temperature oxide)–SOG (spin-on-glass)–LTO sandwich to protect the metallization and CMOS circuitry from the subsequent etching steps in the sensor process. After formation of via holes to connect to the underlying aluminum IC metallization, Ti/W and Au are deposited and patterned. The Ti/W layer serves as an adhesion layer for the gold and as a diffusion barrier to keep the gold from interacting with the aluminum. Next, a conductive sacrificial spacer (Cr/Al/Cr) is deposited and patterned. This layer defines the movable portions of the sensor element and also serves as a plating base layer for electroforming the microstructure. Then, the electroforming mold is defined and the sensor element is formed by selective electroplating in the open mold areas. Finally, the mold and sacrificial layer are removed, completing the sensor process. Fig. 1.23 b shows close-up photographs of the photoresist plating mold and the fabricated metal ring and electrodes.

Both additive electroplating technologies are room temperature processes and do not affect the performance of the underlying CMOS circuits. As with most surface-micromachined structures, control of the thin-film stress and stress gradients is a major challenge.

If the monolithic integration of MEMS and CMOS circuitry is either technologically or economically not feasible, a hybrid integration based on wafer bonding of a MEMS wafer to a CMOS circuit wafer might be a viable alternative. Examples of this approach include an acceleration sensor developed by austriamicrosystems

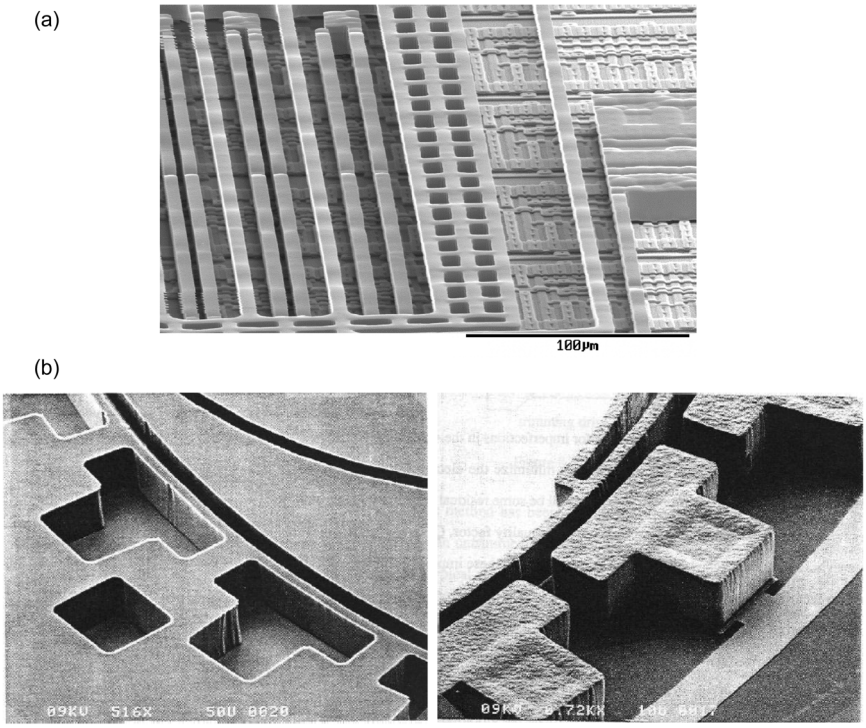


**Fig. 1.23** (a) Detail of acceleration threshold switch by Infineon Technologies and the University of Bremen, fabricated using gold electroplating on top of a CMOS substrate. Reprinted with permission from [148]. (b) Detail of photoresist mold (left) and electroplated nickel structure (right) of vibrating ring gyroscope developed by General Motors, the University of Michigan and Delphi Electronics [148, 149]. SEM photographs courtesy of Prof. K. Najafi, University of Michigan, USA

[153] and a pressure sensor developed at ETH Zurich and Micronas [154]. The acceleration sensor is based on a polysilicon cantilever beam fabricated on the MEMS wafer and released by wet anisotropic silicon etching [153]. The cantilever beam forms the movable electrode of the capacitive microsystem. Static actuation and sensing electrodes and also the readout electronics are implemented on the CMOS wafer. MEMS and CMOS wafer are finally hermetically bonded to each other using an Au–Si eutectic bonding technique, resulting in a controlled spacing between cantilever beam and static electrodes. The capacitive pressure sensor is based on a silicon membrane micromachined on the MEMS wafer using wet anisotropic etching from the back of the wafer [154]. The MEMS wafer is solder bonded on to the substrate wafer with the counter electrode. In both approaches, CMOS and MEMS wafers can be processed independently in a CMOS and MEMS foundry, respectively, and are joined in the final wafer bonding step.

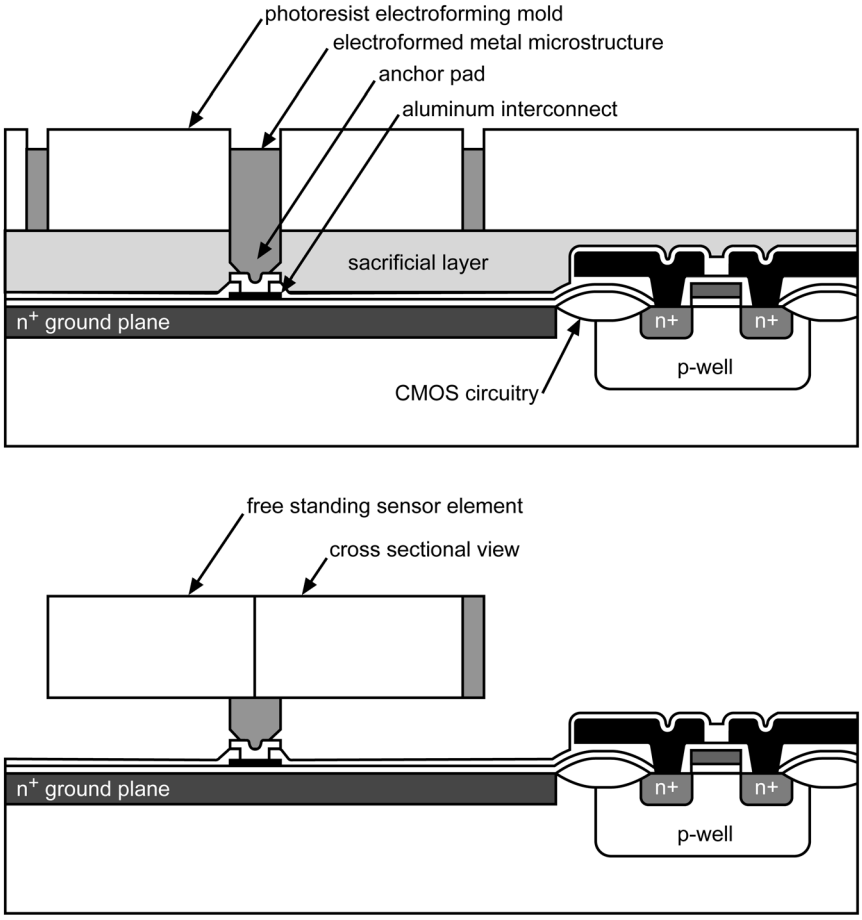


**Fig. 1.24** Schematic cross-section of electroplated ring gyroscope developed by General Motors, Delphi-Delco Electronics and the University of Michigan (a) before and (b) after removal of the photoresist plating mold and the conductive sacrificial layer. Adapted from [149]

#### 1.4.3.2 **Post-CMOS Micromachining of CMOS Layers**

In this approach, microstructures are released by micromachining the CMOS substrate wafer itself after the completion of the regular CMOS process sequence. By far the majority of demonstrated devices rely on bulk micromachining processes, such as wet and dry anisotropic and isotropic silicon etching, but surface-micromachining approaches have also been proposed.

Piezoresistive pressure sensors based on bulk-micromachined silicon membranes were the earliest commercially successful application of silicon micromachining, with the first complete silicon pressure transducer catalog distributed by National Semiconductor in 1974 (an excellent overview of the early MEMS efforts

was published in 1982 by Petersen [9]). It is therefore not surprising that early attempts to co-integrate transducers and electronics also targeted bulk-micromachined pressure sensors. Fully integrated and temperature-compensated pressure sensors using bipolar technology were demonstrated in 1979 [226, 227]. Shortly thereafter, the first integrated capacitive pressure sensor with bipolar circuitry was demonstrated [228]. The first CMOS-integrated piezoresistive silicon pressure sensor was developed by NEC in the mid-1980s [160]: the sensor consists of a thin, square silicon diaphragm with four piezoresistors in a Wheatstone bridge configuration located along the clamped edges. p-Type wafers with an n-type epitaxial layer were used as starting material for the p-well CMOS process. While an additional implantation step for the piezoresistors was implemented in the CMOS process sequence, the actual silicon micromachining steps were performed after the completion of the CMOS process sequence. The membranes were released by anisotropic etching from the back of the wafer using a hydrazine–water etchant [160]. An electrochemical etch-stop technique was applied to stop the etching automatically at the p–n junction between p-substrate and n-epitaxial layer. Finally, the sensor wafer was anodically bonded to a glass constraint wafer. The early NEC pressure sensor featured on-chip circuitry for a stable Wheatstone bridge biasing, temperature compensation and signal amplification.

Today, CMOS-integrated piezoresistive pressure sensors are commercially available from several companies, including Bosch [229], Freescale (Motorola) [221] and Silicon Microstructures [230]. Although the basic transducer structure of these microsystems is still a bulk-micromachined silicon membrane with implanted piezoresistors, far more circuitry components are implemented in these modern systems. The Freescale (Motorola) design features an on-chip digital signal processor (DSP) and non-volatile memory for calibration, temperature compensation and the ability to implement customer-specific features [163]. The CMOS process is only slightly modified to provide the optimal doping profile for the piezoresistors and to deposit the etch mask for the membrane release on the back of the wafer. The membrane is released using a timed wet etching step, yielding membranes with a $\pm 2\,\mu m$ thickness tolerance across the wafer [163]. Finally, the sensor wafer is anodically bonded to a glass wafer in vacuum.

Bulk micromachining from the back of the wafer using silicon anisotropic etching has become one of the standard post-CMOS micromachining modules, releasing not only membranes but also cantilevers and suspended microstructures. Substantial work in this area has been done e.g. at ETH Zurich [19, 22, 169–171, 174–176, 231], the University of Michigan [77, 104, 137, 138, 206], Tohoku University [114, 115], and the Fraunhofer Institutes [167, 168]. A typical device cross-section after post-CMOS bulk micromachining is shown in Fig. 1.25. In addition to the pressure sensors mentioned earlier, e.g. accelerometers, flow sensors, ultrasound proximity sensors, thermal converters, infrared radiation sensors, and chemical sensors have been fabricated using this approach (see Tab. 1.4).

While potassium hydroxide (KOH) solutions have become the most common wet etchant used in bulk micromachining from the back of the wafer, various etch-stop techniques are employed to control the etch result. In addition to a

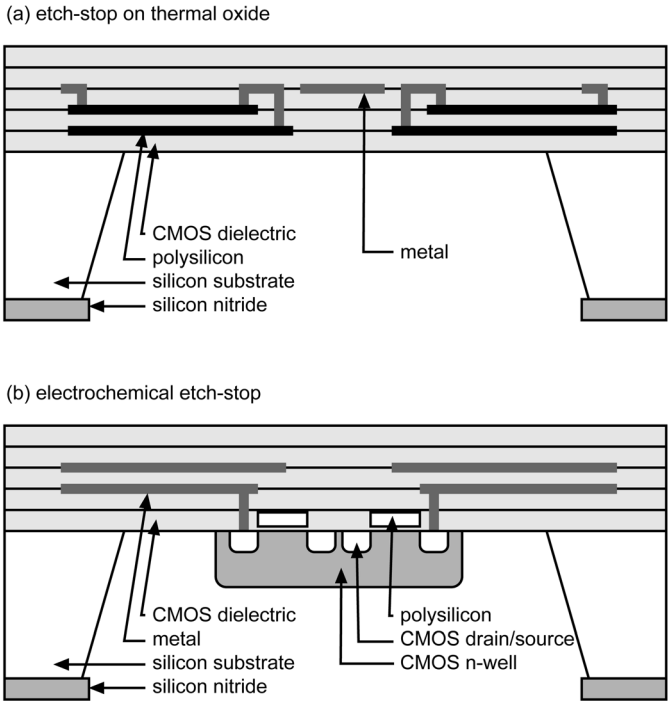


**Fig. 1.25** Post-CMOS bulk micromachining from the back of the wafer

timed etch (e.g. [163]), silicon dioxide layers, highly $p^{++}$-doped silicon regions and p–n junctions are commonly used as etch-stop layers. Membranes consisting of the dielectric layers of the CMOS process are released by using the field oxide on top of the silicon substrate as an intrinsic etch-stop layer [232]. The use of SOI-based CMOS processes offers the possibility of employing the buried oxide layer of the SOI substrates as an etch-stop layer in order to release single-crystalline silicon structures. Alternatively, a buried etch-stop oxide can be locally fabricated before the CMOS process sequence (i.e. as a pre-CMOS sequence) by high-dose oxygen implantation with subsequent high-temperature annealing [116].

Early CMOS-based pressure sensor designs [160, 161] relied on electrochemical etch-stop (ECE) techniques [65] to cease the silicon etching at the p–n junction between a p-type substrate and an n-type epitaxial layer. In this implementation, a special wafer starting material had to be introduced, as commercial CMOS processes are typically not based on p-doped substrates with n-type epitaxial layers. Fortunately, the ECE technique can be also applied at the p–n junction between the n-well of a CMOS process and the p-doped substrate [17, 179, 214]. In this case, however, the electrochemical potential provided by a potentiostat has to be connected to each individual 'mechanical' n-well on the wafer. A scheme to modify commercial CMOS device technologies for application of ECE in a four-electrode configuration has been presented in [17] (see also Section 1.3.2): to supply

the ECE potentials to the sensor structures, a contact field and a wafer-wide contact network are generated (see Fig. 1.26). The contact network routes the n-well and p-substrate potential to the respective contacts on the sensor structures. The chosen process sequence comprises additional standard photolithography steps at the metallization and passivation mask levels performed exclusively on wafer steppers. Hence, there are no restrictions on the minimum feature size of the process or the wafer diameter.

The $p^{++}$ etch-stop techniques have been used extensively by Wise and co-workers for the fabrication of CMOS-based mass-flow sensors [77], microelectrode recording arrays [137] and IR sensors [205]. Even though the microstructure release is done after the completion of the CMOS process sequence, the $p^{++}$ etch-stop requires a preparatory intra-CMOS process module to diffuse highly p-doped regions into the silicon substrate wafer after the p-well implantation (see Section 1.4.2).

Bulk micromachining from the back of the wafer requires the deposition and patterning of a hard mask on the back of the wafers. Prior to the deposition of the hard mask, any processing residues and damage caused by the CMOS process have to be removed from the back side of the wafer. Damage in the wafer surface can lead to an intolerable large mask underetching during the MEMS release. The preparation of the wafer back can be achieved, e.g., using a spin etcher [18]. The hard mask typically consists of a PECVD silicon nitride layer, if necessary with a pad of oxide underneath. Care must be taken to minimize the pinhole density for the subsequent anisotropic wet etching step. The etch mask is patterned using a double-side mask aligner, aligning the patterns on the wafer back to front-side structures. Subsequently, the CMOS wafer is typically mounted in a wafer holder to protect the wafer front with the CMOS circuits from the wet etchant. In the case of wet anisotropic etching with an electrochemical etch-stop technique, the

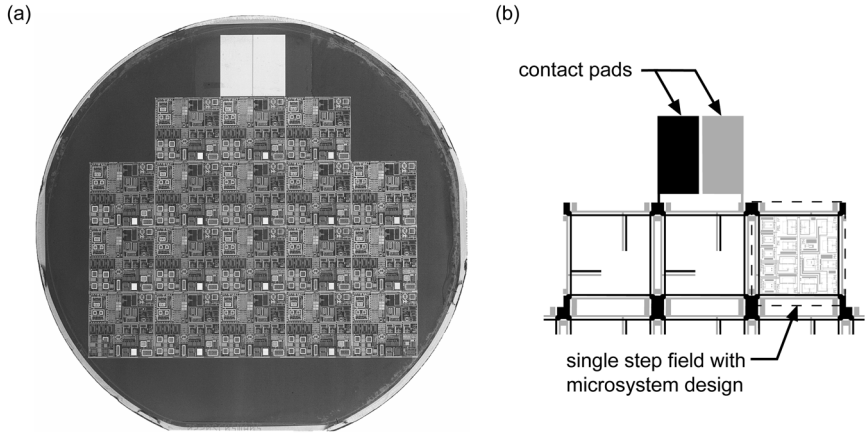


**Fig. 1.26** (a) CMOS wafer with large contact pads to enable anisotropic wet etching from the back of the wafer with an electrochemical etch-stop technique. (b) Schematic of etch network routing the etching potentials for the structural n-well and substrate contacts from the contact pads to the individual microstructures. Adapted from [17, 18]

wafer holder supplies the etching potentials to the wafer (see, e.g., [233]). The need for mounting every wafer in a mechanical holder might be cumbersome, but is currently still the most reliable method to protect the front-side structures and the wafer edges. Recently, alternative protection schemes based on metal films [234] or polymer layers [18] have been proposed.

Alternative to wet etching, bulk micromachining from the back of the wafer can be performed with DRIE systems, resulting in almost vertical sidewalls independent of the silicon crystal orientation. DRIE techniques have gained significant momentum over the past few years, but the equipment required is expensive, only single wafers can be processed at a time and no ECE or $p^{++}$ etch-stop can be used. On the other hand, DRIE can achieve structures, e.g. narrow support bars, that cannot be achieved by KOH etching of (100) wafers.

The post-CMOS release of microstructures from the front of the wafer using anisotropic silicon etchants was pioneered by Baltes and co-workers [80, 235]. By superimposing active area, contact, via and pad opening in the design of the integrated microstructures, silicon areas on the wafer surface are exposed to the ambient at the end of the regular CMOS process sequence. Anisotropic wet etchants, such as EDP and TMAH, will etch the silicon substrate in these areas (see Section 1.2.1). Alternatively, isotropic dry etching techniques based on, e.g., $XeF_2$ can be used for microstructure release [188]. In the case of anisotropic wet etchants, the etch mask consisting of the dielectric layers of the CMOS process will be underetched at convex corners, allowing the release of dielectric microstructures, such as cantilever beams and bridges [80, 232]. Polysilicon and metal layers can be embedded in these microstructures, enabling the fabrication of a variety of microsensors, including flow sensors [236], power sensors [173] and IR sensors [185, 186]. Care must be taken to protect the aluminum contact pads of the CMOS process during the etching step. Certain EDP and TMAH formulations have relatively small aluminum etch rates, allowing a maskless wet release of the microstructures if the etching step is not too long. KOH etching solutions cannot be used for front-side release because of the relatively large silicon dioxide etch rate. In order to permit active electronics on the microstructures, the bulk micromachining from the front of the CMOS wafer has been successfully combined with an electrochemical etch-stop technique on CMOS n-wells [179] (see Fig. 1.11 b). For example, CMOS-based thermal converters [180] and focal plane arrays [185, 186] have been fabricated in this way.

An alternative bulk micromachining technology from the front side of CMOS wafers using dry etching steps has been developed at Carnegie Mellon University [193]. The post-CMOS micromachining module uses the top metal interconnect layer as etch mask for the microstructure definition. In this way, the minimum feature sizes, such as minimum beam widths and gaps, are defined by the CMOS design rules and can be scaled with the CMOS technology. The actual laminated microstructures consisting of the CMOS dielectrics with polysilicon and metal layers sandwiched in between are released using two dry etching steps (see schematic in Fig. 1.27 a): in the first anisotropic etching step using $CHF_3$–$O_2$ etch chemistry, the oxide areas not protected by the metal mask are etched to the sili-

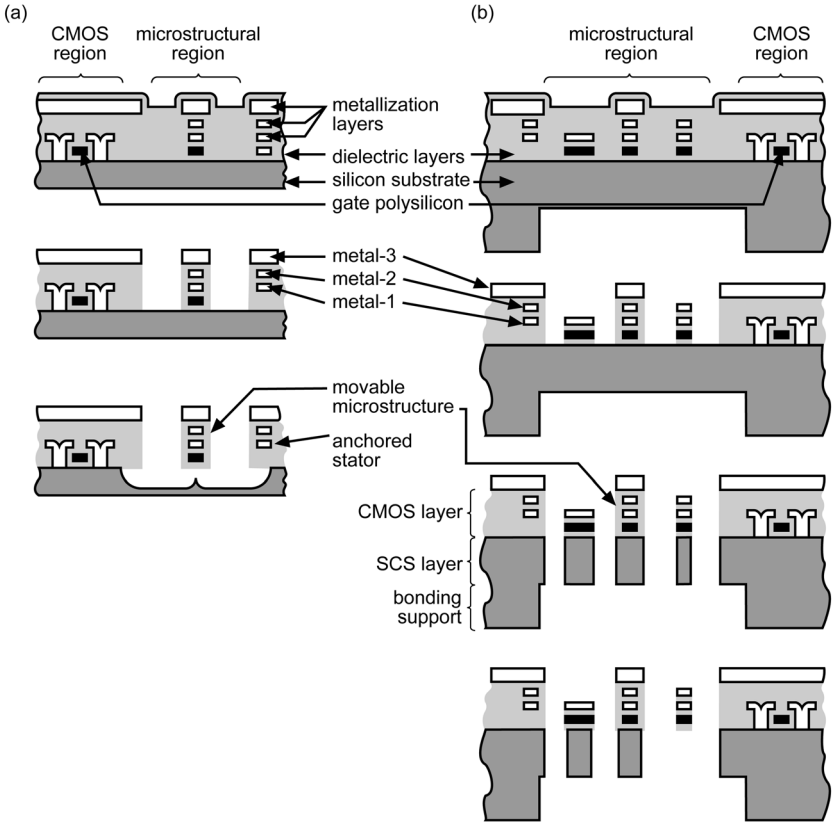


**Fig. 1.27** Cross-section of post-CMOS process sequences developed at Carnegie Mellon University to release (a) dielectric (adapted from [193]) and (b) crystalline silicon microstructures (adapted from [194]). Both processes are based on a series of anisotropic and isotropic dry etching steps

con substrate; in the second isotropic etching step using $SF_6$–$O_2$ chemistry, the oxide beams are underetched, releasing the microstructures. The isotropic release etch has a vertical to lateral etch rate of about 2:1, safely undercutting 16 µm wide structures for a typical etch depth of 25 µm. The process technology has been used to fabricate integrated accelerometers [195], gyroscopes [197], IR sensors [200] and acoustic devices [198, 199]. To construct a speaker or microphone, a mesh-type membrane is released with the described post-CMOS dry etching sequence. The released mesh is conformally coated with polymer in a CVD process, yielding a continuous, airtight membrane [199] (for more detail, see Chapter 4).

Depending on the CMOS process, the released dielectric layer sandwich with embedded polysilicon and metallization lines can be subject to large residual stress and stress gradients, causing large microstructures to curl. To be able to release single-crystalline silicon microstructures, the maskless post-CMOS micromachining process developed at Carnegie Mellon University has been combined with

DRIE and an anisotropic etch step from the back of the wafer ([194]; see schematic in Fig. 1.27 b). The new post-CMOS process sequence starts with a deep anisotropic backside etch, leaving a 10–100 μm thick single-crystal silicon membrane. The membrane thickness ultimately controls the thickness of the microstructure. Next, an anisotropic dry etching step is performed from the front of the wafer, removing silicon dioxide where it is not protected by the top metal layer. Then, in contrast to the earlier technology [193], an anisotropic instead of isotropic silicon etching step is used to release the microstructures, which now consist of a thick silicon layer in addition to the dielectric layer sandwich. With an optional lateral underetch, the silicon under small beams can be removed to achieve, e.g., electrical isolation of certain silicon areas. The process has been used, e.g., for the fabrication of a *z*-axis accelerometer [194] and a gyroscope [196].

A unique post-CMOS bulk-micromachining process based on silicon-on-glass (SOG) bonding has been demonstrated recently at the University of Michigan [207]. A schematic of the SOG monolithic integration process is shown in Fig. 1.28. First, conventional IC fabrication is performed on a silicon wafer. A glass substrate with recessed cavities and a shielding metal is also prepared. The metal is deposited and patterned on the glass substrate not only to avoid the micro-loading effect from the following DRIE, but also to protect the IC from the large electric field during the bonding process. Next, the fabricated silicon wafer is anodically bonded to the glass substrate and is thinned to the desired thickness using CMP. Finally, metal contacts are formed, and DRIE is used to define the MEMS structure, silicon islands and dielectric bridges.

So far, post-CMOS bulk-micromachining modules have been discussed to release microstructures consisting of the layers of the CMOS process. In addition, surface-micromachining techniques can be used to remove thin-film layers of the CMOS process selectively, thus releasing different types of microstructures. An example is the sacrificial aluminum etching (SALE) technique developed at ETH Zurich [237]. In this post-CMOS micromachining module, the first metal layer of the CMOS process is selectively removed to release microstructures comprised of the intermetal dielectric, the upper metallization layer and the passivation. During the sacrificial aluminum etching using standard wet etchants [237], the electrical

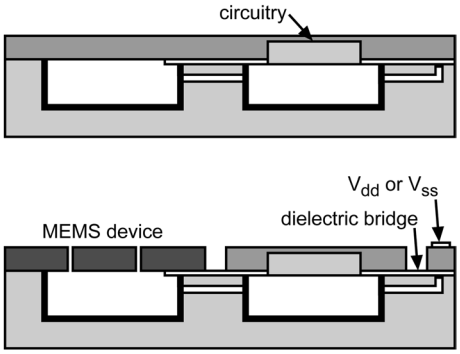


**Fig. 1.28** Schematic cross-section of monolithic silicon-on-glass microsystems developed at the University of Michigan using a post-CMOS micromachining module [207]. Courtesy of Dr. J. Chae, University of Michigan

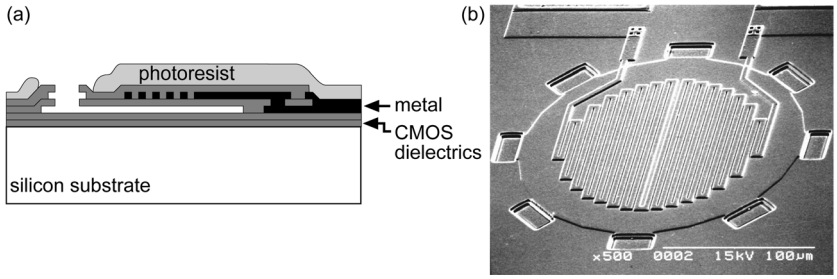


**Fig. 1.29** (a) Schematic cross-section and (b) SEM photograph of a Pirani-type pressure sensor released in a post-CMOS module by sacrificial aluminum etching (SALE). Adapted from [155]

contact pads have to be protected either using a photoresist layer or electroplated, etch-resistant contact bumps. Fig. 1.29 shows a cross-section and an SEM photograph of a thermal pressure sensor realized with the SALE process [155]. The circular pressure sensing membrane is released by etching the sacrificial aluminum layer through a number of etch holes around its perimeter. The second aluminum layer is used to form a resistor inside the membrane, acting as both heating element and temperature sensor. A complete thermal pressure-sensing system based on the surface-micromachined sensor cells has been presented [156].

A second example is a mass-sensitive nanocantilever fabricated recently using a post-CMOS surface-micromachining technique [158]. The approach uses an innovative laser beam direct lithography process to structure an aluminum etch mask. The aluminum mask is used to transfer the cantilever structure to the gate polysilicon layer of the CMOS process. Finally, the polysilicon cantilever having submicron width and height is released by locally removing the field oxide layer underneath the cantilever using BOE (buffered oxide etch). All these process steps are performed after the completion of the regular CMOS process sequence. To do this, the passivation and upper polysilicon layer are removed in the sensor area. A thin aluminum layer acting as etch mask is deposited on top of the thin oxide separating the two polysilicon layers [158].

## 1.5 Conclusion

A large number of process technologies for the co-integration of MEMS with CMOS circuitry has been demonstrated over the past 20 years. Even though the material and process choices are limited to ensure compatibility with the underlying CMOS process, this fabrication constraint is, for many applications, outweighted by the possibility of on-chip electronics and the proven reliability of well-established CMOS technologies. High-volume applications (e.g., inertial and pressure sensors) and applications requiring sensor arrays (e.g., DMD and infrared imagers) are predestined for CMOS integration. As examples, Analog Devices

is producing about 1 million inertial sensors per week [107] and Texas Instruments' DMD chips consist of up to 1.3 million, individually addressable, CMOS-integrated micromirrors [74]. While physical sensors currently clearly dominate the CMOS-based sensor market, chemical and biological microsensors are likely to benefit from the CMOS-integration as well, enabling small-size sensing arrays for, e.g., hand-held, battery-operated (bio)chemical sensing systems.

While many of today's CMOS-based microsystems still require the insertion of dedicated (micromachining) modules in between the regular CMOS process steps, a clear trend towards not interrupting the CMOS sequence can be observed. This can be achieved by adding the required process modules either before (pre-CMOS) or after (post-CMOS) the CMOS process steps. From a manufacturing point of view, especially the post-CMOS approach is appealing: the CMOS process can be completed in a dedicated CMOS foundry, followed by a micromachining module processed in a dedicated MEMS foundry. This approach allows especially small and medium size MEMS companies without in-house CMOS capability to design and produce CMOS-based MEMS.

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