I
Introduction

1
Organic Transistors

Gilles Horowitz

1.1
Introduction

Although the beginning of the electronics age was marked by Karl Braun's cathode ray tube (1897) and Ambrose Fleming's vacuum rectifier (1904), it was actually launched by Lee de Forest's vacuum-tube ''triode'' (1906); by including a ''grid'' between the anode and the cathode, the triode transformed the rectifier into an amplifier, thus making radio communications and long-distance telephone a reality. The vacuum triode had its limitations, however – it was fragile, rather slow, difficult to miniaturize, consumed too much energy and produced too much heat. The idea of replacing the triode with a solid-state device offering an alternative to the thermionic principle can be traced back to the mid-1920s. In October 1926, Julius Edgar Lilienfeld filled a patent describing an ''apparatus for controlling the flow of an electric current between two terminals of an electronically conducting solid by establishing a third potential between said terminals'' [1]. He probably never got his device to work, and his patent went into obscurity. It was not until thirty years later that this early concept could be successfully demonstrated. This was *not* with the celebrated Bardeen and Brattain's ''point-contact'' transistor (1947), nor with Shockley's bipolar transistor (1948) – both devices were based on different principles. Actually, nearly fifteen more years of material technology research were needed to finalize the silicon–silicon dioxide metal-oxide-semiconductor field-effect transistor (MOSFET) [2]. Today, MOSFETs dominate our environment; there are millions of them in the processors used in personal computers, cellular phones, and many other microelectronic devices. The success of MOSFETs actually rests on a continuous improvement in the handling of one semi-conducting material, silicon.

Besides their numerous technological applications, FETs have also been used as tools for studying charge transport in solid materials; this is because the device gives direct access to charge-carrier mobility. A celebrated example of such a concept is with hydrogenated amorphous silicon (a-Si:H). For this, an alternative architecture was employed, the thin-film transistor (TFT) [3], which differs from the MOSFET in that the conducting channel is induced in the accumulation regime

rather than through the formation of an inversion layer. The first a-Si:H TFTs were actually designed to measure the mobility of the material, which was at that time difficult to access by other techniques [4, 5]. It was only later that the technological importance of the device was recognized in applications in which large area is required and where single crystalline silicon can no longer be used. Today, a-Si:H TFTs play a crucial role in active-matrix liquid-crystal displays (AM-LCD).

Organic semiconductors have been identified as early as the late 1940 [6]. Because they are low mobility materials, the TFT structure is well suited to these solids. Apart from a handful of isolated preliminary reports [7–9], however, work on organic thin-film transistors only emerged in the late 1980s on both polymers [10, 11] and small molecules [12, 13]. Because of the poor performance of these initial devices, interest in organic thin film transistors (OTFTs) remained limited to a small number of academic groups for nearly ten more years. During that period, much research effort was devoted to improving the charge-carrier mobility; several review papers can be consulted to learn of this quest for better materials and device structure [14–18]. It is only when the mobility of organic semiconductors approached, and even surpassed, that of amorphous silicon [19] that several industrial groups decided to embark into research programs on OTFTs.

The availability of organic semiconductor devices may open the way to completely new set-ups, fabrication processes, and applications. Thus, one can envisage processing of organic materials by printing, which enables high-volume, low-cost production. New products include radio-frequency identification (RFID) tags [20], that might replace the optical bar code found on nearly all consumer goods today, single-use electronics, low-cost sensors, and flexible displays.

The purpose of this introductory chapter is to give a general overview of the topic. Emphasis will be made on recent leading advances in terms of materials and device fabrication, together with the development of models that help understanding of what controls the operating mode of the device, thus opening ways at improving its performance. It is worth pointing out that although organic semiconductors have been identified for more than half a century, the field of organic electronics is still in its infancy. Accordingly, a general consensus has not yet been achieved on several basic points. The reader should therefore keep in mind that on many points, the opinion reported here is that of the author, and may differ from what is found elsewhere in this book.

1.2
Overview of the Organic Thin-film Transistor

1.2.1
Are Organic "Semiconductors" Real Semiconductors?

Asking this question may sound provocative in a book devoted to "organic electronics". Actually, one would first ask the question "what is a semiconductor?" In most current dictionaries, a semiconductor is still defined as "a nonmetallic solid

that has electrical conductivity between that of a conductor and an insulator''. According to several sources, the first occurrence of the word (''Halbleiter'' in German) dates back to 1911 [21], at a time when electrical conduction in solids was not fully understood. Classical physics served well at accounting for electrical conduction in metals, but was contradicted by the ''anomalous'' behavior of various non-metals, among which were silicon and a variety of binary compounds, for example oxides and sulfides. The ''anomalous'' phenomena associated with these materials, for which the word ''semiconductor'' was invented, included the positive variation of conductivity with temperature, photoconductivity, rectification, and photovoltaic effect. The puzzle was only resolved with the advent of quantum mechanics and the subsequent development of the band theory of solids [22]. The following definition, more in accordance with our current state of knowledge, can be found in a ''modern'' encyclopedia [23]: ''A semiconductor is a material that is an insulator at very low temperature, but which has a sizable electrical conductivity at room temperature. The distinction between a semiconductor and an insulator is not very well-defined, but roughly, a semiconductor is an insulator with a band gap small enough that its conduction band is appreciably thermally populated at room temperature.'' ''Semi-insulators'' would certainly be a more appropriate designation of these materials, but it is too late for such a correction.

The above definition is actually that for *intrinsic* semiconductors. What make semiconductors so useful in electronics, however, is that their electronic properties can be altered in a controllable manner by adding tiny amounts of an advisedly chosen impurity. This is the well-known process of doping, which is related to the notion of *extrinsic* semiconductors.

The difference between intrinsic and extrinsic semiconductors is illustrated in Fig. 1.1, which represents the energy diagram of metals, insulators, and semi-
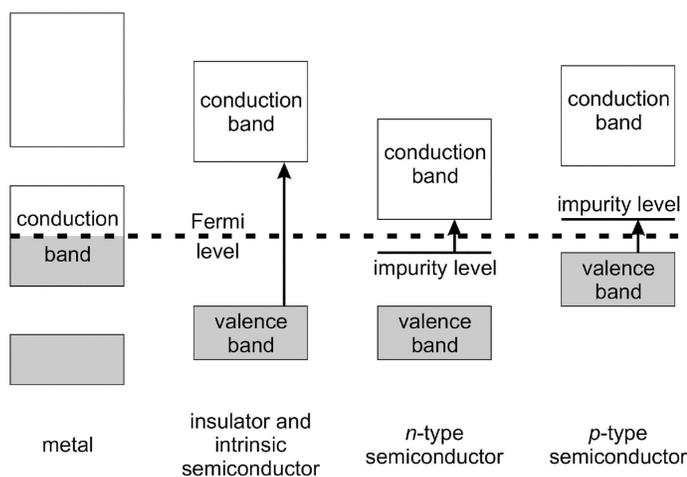

Fig. 1.1. Energy diagram of a metal, an insulator, and an extrinsic semiconductor.

conductors, as pictured in the framework of the now well-accepted band theory of solids. The theory delineates a clear distinction between a metal, which has a partially-filled conduction band, and an insulator characterized by a filled valence band and an empty conduction band. An insulator is, however, only perfectly insulating at $T = 0$ K. As soon as its temperature is elevated, electrons can be thermally excited from the valence band to the conduction band. Because electrical conduction can occur in partially filled bands, both bands contribute to conduction. Because thermal energy is low ($kT = 25$ meV at room temperature), this thermally activated conduction can only be observed in a low energy-gap insulator, also termed intrinsic semiconductors.

Doping a semiconductor results in induction of localized energy levels close to the conduction (n-type doping) or valence (p-type doping) band edge. Accordingly, the energy required to promote an electron (a hole) in the conduction (valence) band is substantially lowered, to a level comparable with thermal energy. The temperature dependence of the conductivity of a typical doped (extrinsic) semiconductor is shown in Fig. 1.2. The curve contains three separated domains. At high temperatures the intrinsic domain is characterized by thermally activated behavior. The intermediate domain is the so-called saturation (or exhaustion) regime in which the conductivity is practically temperature-independent. Finally, at low temperature the carriers are frozen. In terms of electronic devices, the only domain of interest is the exhaustion regime, where the density of charge-carriers practically equals that of the dopant.

At this stage, it is essential to note that doping requires high purity. Actually, with the notable exception of electronic grade silicon and a few other inorganic compounds used in microelectronics, most semiconductors contain approximately equal amounts of n and p-type doping impurities; such materials are termed *compensated* and behave much like intrinsic semiconductors. Almost all organic semiconductors belong to that category. In particular, the effect of intentional doping in organic semiconductors only appears for large densities of dopant (a few percent,
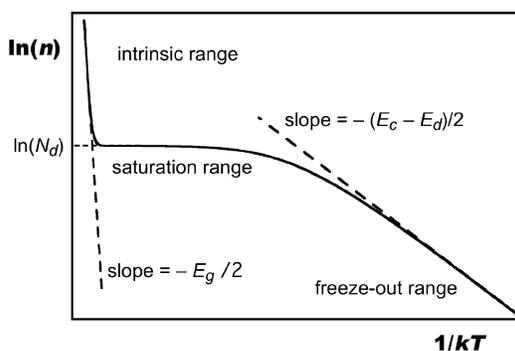

Fig. 1.2. Arrhenius plot of the temperature-dependent conductivity of an extrinsic semiconductor.

compared with ppm, or even less, in silicon). At this level, ''doped'' organic semiconductors are conductors rather than semiconductors, and are useless for making electronic devices.

In conclusion, we can state that organic semiconductors are closer to insulators than to semiconductors. Despite several claims, no definitive evidence has been obtained for the possibility of ''microelectronic grade'' doping of organic semiconductors, mainly because the purity of these materials is still too low. Their potential in constituting the basis of electronic devices is, however, now well established. This was made possible by using an alternative means of inducing charge-carriers, namely injection from electrodes. As we shall see in the following discussion, this new concept implies that the very notion of n and p-type must be redefined.

1.2.2
Thin-film Transistor Architecture

The structures of OTFTs have several variants. Roughly speaking, a TFT is made of three parts – an insulator, a thin semiconducting layer, and three electrodes. Two of the electrodes, the source and the drain, are in direct contact with the semiconductor; the third, the gate, is isolated from the semiconductor by the insulator. The structure of the device is dictated not only by its operating mode, but also by issues arising from its fabrication. The basic fabrication scheme consists of piling up thin films of the different elements. Because most organic semiconductors are fragile materials, the deposition of organic semiconductors on the insulator is much easier than the converse. So the large majority of current OTFTs are built according to the bottom-gate architecture, which in turn declines in two alternatives depicted in Fig. 1.3, top contact (TC) and bottom contact (BC). Each of these structures has its advantages and drawbacks. In the BC structure, contacts are deposited on the insulator; if the latter is an inorganic oxide for example silicon oxide, the electrodes can be patterned by means of microlithographic techniques. This is not possible with TC architecture; with this architecture contacts are deposited through shadow masks, with substantial loss of resolution. On the other hand, contact resistance has been reported to be lower in TC than BC.

(a)   (b)
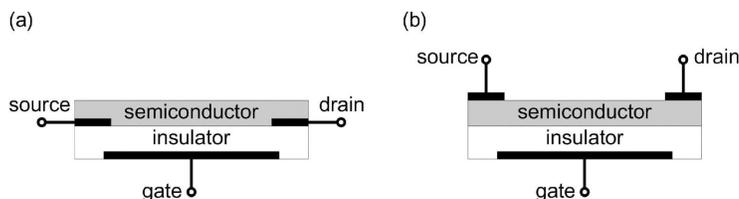
Fig. 1.3. Schematic view of the structure of organic thin film transistors. Both structures are top-gated. (a): Bottom contact (BC); (b): Top contact (TC).

(a)

(b)
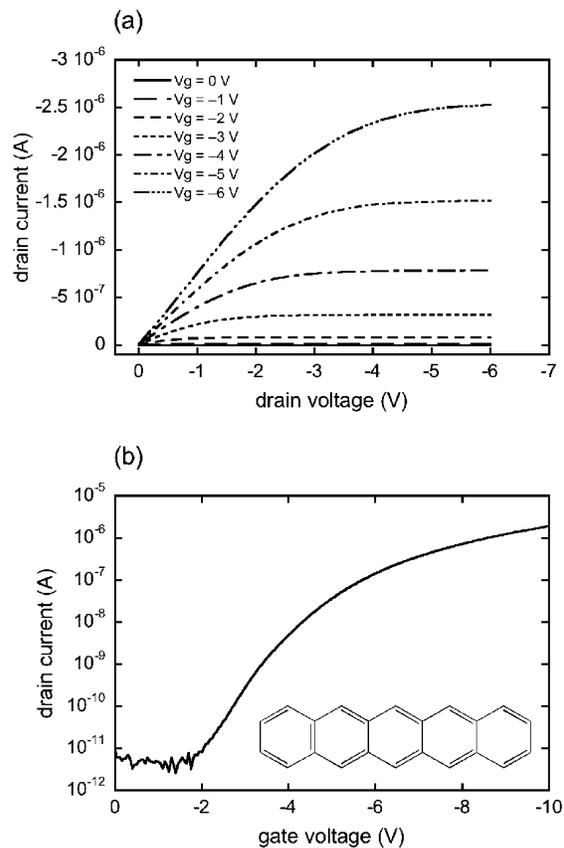
Fig. 1.4. Output (a) and transfer (b) characteristics of a typical OTFT. The inset shows the molecular structure of pentacene, which serves as semiconductor in the device.

1.2.3
Operating Mode

To demonstrate the operating mode of the OTFT, a typical set of current–voltage characteristics are shown in Fig. 1.4. These curves were measured on a device made of pentacene, the chemical structure of which appears in the inset, with gold source and drain electrodes. The energy scheme in Fig. 1.5 indicates the respective positions of the Fermi level of gold and the frontier orbitals (highest occupied molecular orbital, HOMO, and lowest unoccupied molecular orbital, LUMO) of pentacene. Data for pentacene were taken from Ref. [24]. Throughout the following discussion the source serves as the reference (grounded) electrode.

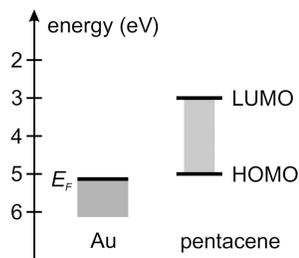When a positive voltage is applied to the gate, negative charges are induced at

Fig. 1.5. Energy scheme of the gold-pentacene interface [24].

the source. As can be seen in Fig. 1.5, the LUMO level of pentacene is quite far away from the Fermi level of gold, so there is a substantial energy barrier for electrons and electron injection is very unlikely. Accordingly, no current passes through the pentacene layer and the small current observed in Fig. 1.4(a) essentially comes from leaks through the insulator. In contrast, when the gate voltage is reversed to negative, holes are easily injected because the Fermi level is close to the HOMO level and the barrier height is low. A conducting channel forms at the insulator–semiconductor interface and charge-carriers can be driven from source to drain by applying a second, independent, bias to the drain. Because holes are more easily injected than electrons, pentacene is said to be p-type. Note that this concept differs from that of doping in conventional semiconductors. Symmetrically, an organic semiconductor is said to be n-type when electron injection is easier than hole injection, which occurs when the LUMO is closer to the Fermi level than the HOMO. Note that in the terminology of organic light-emitting diodes, these two classes of materials are often designated ''hole transport'' (or hole-injecting) and ''electron transport'' (or electron-injecting) materials.

Basically, the thin-film transistor operates like a capacitor; when a voltage is applied to the gate an equal (but of opposite sign) charge is induced at both sides of the insulator. On the semiconductor side this charge forms a conducting channel, if the charge-carriers can be injected into the semiconducting material; because the conductance of the channel is proportional to the charge, it is also proportional to the gate voltage. At low drain voltage, the current follows Ohm's law; it is therefore proportional to both the gate and drain voltages. As the drain voltage increases, the voltage drop at drain decreases to a point at which it falls to zero. At this point, which occurs when the drain voltage approaches the gate voltage, there is a pinch off of the channel, and the channel current becomes independent of the drain bias. This regime is called the saturation regime. The gradual transition from the linear to the saturation regime is clearly shown in Fig. 1.4(a). The curve in Fig. 1.4(b) is the transfer characteristic; it shows than the device has a high on–off ratio, which makes it very useful in logic circuits.

The linear and saturation current can be quantified by use of Eqs. (1) and (2), which are derived on the basis of two assumptions:

1. the electric field along the channel is much lower than that across it. This is the so-called gradual channel approximation, which is valid when the distance between source and drain is much larger than the thickness of the insulator; and
2. the mobility, μ, is constant.

$$I_{\text{Dlin}} = \frac{W}{L} \mu C_i (V_G - V_T) V_D \tag{1}$$

$$I_{\text{Dsat}} = \frac{W}{2L} \mu C_i (V_G - V_T)^2 \tag{2}$$

where W and L are the channel width and length, C_i is the insulator capacitance per unit area, V_G and V_D are the gate and drain voltages, and V_T the threshold voltage that takes into account various potential drops through the gate–insulator–semiconductor structure. The limitations of using these over-simplified equations to estimate the mobility will be detailed below.

1.2.4
Thickness of the Channel

From the very beginning, two classes of material have been used in organic field-effect transistors – conjugated polymers and small molecules. The best performance has been obtained with materials belonging to the latter category. Conjugation means that the carbon backbone has alternating single and double bonds, which confers stiffness to the molecules, so they can be regarded as rigid rods. In the solid state, these rods tend to pack parallel to each other, thus forming layers, the width of which roughly equals the length of the molecule. The crystal structure of pentacene [25, 26], shown in Fig. 1.6, perfectly illustrates this arrangement. Typical values for the thickness of a monolayer range between 1.5 and 3 nm.
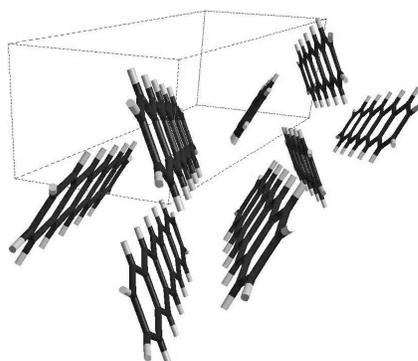

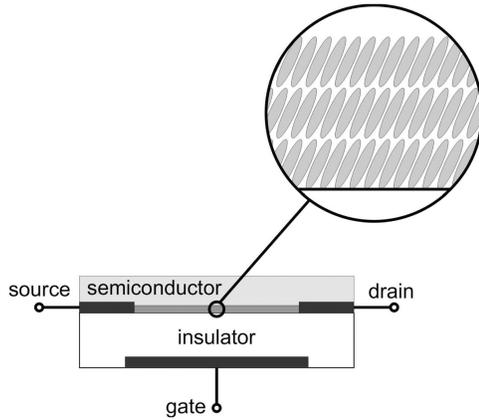**Fig. 1.6.** Crystal structure of pentacene.

Fig. 1.7. Arrangement of the molecules in the conducting channel of an OTFT made of short conjugated molecules.

Because molecules located in the same layer are much closer to each other than those situated in different layers, charge transport is expected to be much more efficient in the direction along the layers than across them. This has largely been confirmed by X-ray diffraction measurements on sexithiophene-based devices [27, 28], which indicated that the highest performance is attained when molecules are standing upright on the insulator. Similar behavior was found for pentacene [29, 30]. This is illustrated in Fig. 1.7, in which the molecules are depicted as short rods.

Let us now turn to the thickness of the conducting channel. The concept of thickness is not that obvious, because the actual distribution of charge-carriers decreases continuously from the insulator–semiconductor interface to the semiconductor bulk, so one can more sensibly speak of an effective thickness. The distribution can be estimated by resolving Poisson's equation (Eq. 3):

$$\frac{\mathrm{d}^2 V}{\mathrm{d}x^2} = -\frac{\rho(x)}{\varepsilon_{\mathrm{s}}} \tag{3}$$

where V is the potential, x the direction perpendicular to the channel, ρ the density of charge, and ε_{s} the permittivity of the semiconductor. There is no analytical solution of Poisson's equation for the metal–insulator–semiconductor structure. An example of numerical solution can be found in Ref. [31]. A satisfactory approximate solution in the accumulation regime is given by Eq. (4):

$$n(x) = \frac{\rho(x)}{q} = \frac{(C_i V_{\mathrm{G}})^2}{2kT\varepsilon_{\mathrm{s}}}\left(1 + \frac{x}{\sqrt{2}L_{\mathrm{D}}}\right)^{-2} \tag{4}$$

where $n(x)$ is the charge-carrier density and q the charge on the carriers. The Debye length, L_D, is given by:

$$L_D = \frac{\sqrt{2}kT\varepsilon_s}{qC_iV_G} \tag{5}$$

where k is Boltzmann's constant and T the temperature. The charge distribution was first derived by Mott and Gurney [32]. The Debye length can be viewed as a rough estimate of the thickness of the channel. Typical values of this "effective" thickness range between 0.1 and 1 nm, which is substantially lower than the thickness of a monolayer. For this reason, it is often stated that practically all the charge of the channel resides in the first monolayer next to the insulator–semiconductor interface [34].

At least two facts may temper this simple description, however. First, Eq. (4) indicates that the density of charge-carriers decreases with distance according to an inverse square law; this is a long-range law, which might imply that the density of charge remains non-negligible even far from the insulator–semiconductor interface. The second argument stems from the layer structure of the semiconducting film. Because the charge-carrier density in the conducting channel is less than one charge out of ten molecules, it is most likely that each charged molecule only bears one elemental charge (electron or hole). Quantum mechanical calculations have shown that in short conjugated molecules the additional charge almost uniformly spreads over the whole entity [33], which leads us to the conclusion that the actual distribution of charge-carriers in the film is not continuous; instead, it presents the staircase shape shown in Fig. 1.8, where the width of each step equals that of one monolayer.
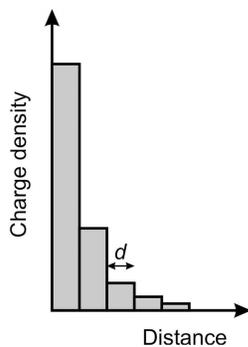
Fig. 1.8. Charge distribution across the conducting channel of an organic TFT. The width of each step corresponds to one monolayer.

Let d be the thickness of a monolayer and n the total number of layers (that is, the thickness of the film divided by d). The layers are numbered starting from the insulator–semiconductor interface. To estimate the density n_i (per unit area) of charge-carriers in the ith layer we apply Gauss's law to a cylinder of unit cross section limited by the boundaries between the ith layer and each of its neighboring layers. For a long channel device, the electric field **F** is perpendicular to the film, and we have:

$$F_{i-1} - F_i = -\frac{qn_i}{\varepsilon_s} \tag{6}$$

where F_i is the module of the electric field at the boundary between the ith and the $(i+1)$th layers. The variation of the electric field F and electrical potential V in the direction perpendicular to the layers is obtained by rewriting Poisson's equation (Eq. 3) as:

$$\frac{\mathrm{d}F}{\mathrm{d}x} = \frac{qn(x)}{\varepsilon_s} \tag{7}$$

where

$$F = -\frac{\mathrm{d}V}{\mathrm{d}x} \tag{8}$$

Because the density of charge is constant in each layer, the electric field varies linearly with distance between two boundaries, which implies, in turn, that the variation of the potential is quadratic within the same limits. Furthermore, we assume that charge transfer between adjacent layers is sufficiently efficient that the distribution of charge-carriers in the whole film is at thermodynamic equilibrium. Assuming Boltzmann's statistics holds, which is true as long as the charge density remains much lower than the density of molecules, this yields:

$$\frac{n_{i+1}}{n_i} = \exp\left[-\frac{q}{kT}(V_i - V_{i+1})\right] \tag{9}$$

After some manipulations, the following series of equations is obtained:

$$n_i = n_{i+1} \exp\left[\frac{dq^2}{kT\varepsilon_s}\left(\frac{n_{i+1}}{2} + \sum_{j=i+2}^{n} n_j\right)\right] \tag{10}$$

Although there is no analytical solution to Eqs. (10), a numerical calculation is easily performed by starting from a given density in the nth layer and cascading down to the first layer. The gate voltage is connected to the n_i values by:
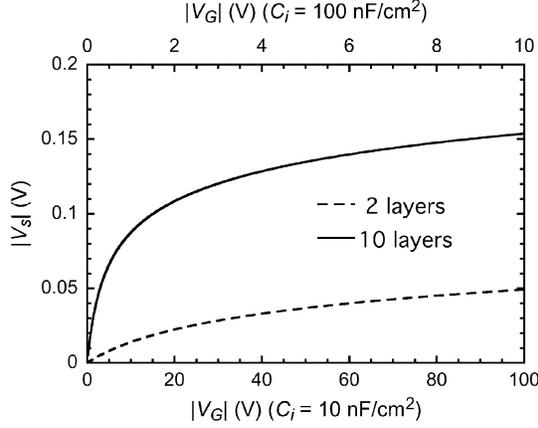
Fig. 1.9. Variation of the potential drop at the insulator–semiconductor interface as a function of gate voltage for two values of the insulator capacitance.

$$C_i(V_G - V_s) = q \sum_1^n n_i \tag{11}$$

where $V_s = V_1$, is the potential at the insulator–semiconductor interface, which is obtained by multiplying Eqs. (9) from $i = 1$ to $i = n$, with the boundary condition $V_{n+1} = 0$:

$$V_s = \frac{kT}{q} \ln \frac{n_1}{n_n} \tag{12}$$

The variation of the interface potential as a function of gate voltage is shown in Fig. 1.9. The value of the gate voltage is calculated for two values of the insulator capacitance, 10 and 100 nF cm^{-2}. In most practical cases the actual value lies between these numbers, so it can be stated that V_s can be neglected in Eq. (11).

Figure 1.10 shows the variation of the ratio of the density of charge-carriers in the first layer to the total density $n_{tot} = \sum n_i$ as a function of the total density of charge-carriers, which is connected to the gate voltage by Eq. (11). We note that the statement "all the induced charge resides in the first layer" is only true at high gate bias. It is worth remarking that at low bias the density of charge-carriers strongly depends on the thickness of the film (i.e. the number of layers). This can be understood by noting that the limit at $V_G \rightarrow 0$ is simply $n_i = n_{tot}/n$ for all values of i. We also note that, even at high gate voltages, a non-negligible part of the induced charge resides outside the first layer. This is worth mentioning because variation of the mobility by a factor of ten from sample to sample is not uncommon.
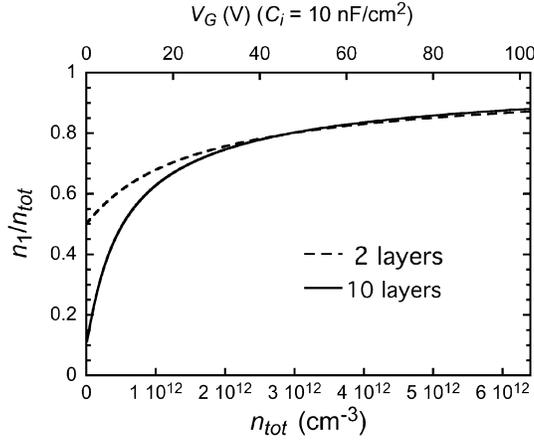
Fig. 1.10. Calculated ratio of the charge in the first layer to the total charge in the conducting channel as a function of gate voltage multiplied by insulator capacitance. The ratio is calculated for two-layer and ten-layer thin films.

1.3
Contact Resistance

Until recently, the issue of contact resistance was hardly mentioned in papers dealing with OTFTs because the performance of the devices was so low that the current flowing between source and drain was only limited by the resistance of the channel. With improvement of the charge-carrier mobility, this is no longer true; limitations by contact resistance are becoming increasingly crucial, and finding ways to reduce these limitations has become a key issue.

1.3.1
Contact Resistance Extraction

Access to contact resistance was first sought by modeling. Figure 1.11 shows equivalent circuits used for that purpose. Note that the bottom circuit includes head-to-toe diodes to account for non-linear contact resistance [35]. The model developed by Necliudov and coworkers also assumed a gate voltage-dependent mobility (this point will be discussed in more detail below).

The dependence is accounted for by a semi-empirical law depicted by Eq. (13):

$$\mu = K(V_G - V_T)^\gamma \tag{13}$$

where K and γ are empirical parameters. The width-normalized contact resistance (i.e. resistance multiplied by channel width) extracted from this model for both top-
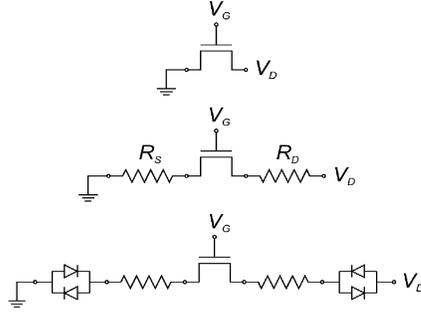
Fig. 1.11. Equivalent circuit of a TFT including contact resistance. The bottom circuit also comprises head-to-toe diodes to account for non-linearity in the contact resistance.

contact and bottom-contact architecture was of the order of 10^3 Ω cm. Data obtained for sexithiophene with TC structure [36] were approximately ten times larger. The extraction method consists of rewriting Eq. (1) by introducing an additional voltage drop $R_c I_D$ where R_c is the contact resistance. This is done by replacing V_D by $V_D - R_c I_D$ in Eq. (1). After some manipulation we obtain:

$$\frac{I_D}{V_D} = \left(\frac{1}{(W/L)C_i \mu (V_G - V_T)} + R_c \right)^{-1} \tag{14}$$

A more general approach was adopted by Street and coworkers [37]. To analyze the effect of contact resistance they add, at both ends of the channel, a small contact region of length d where there is a voltage drop V_c. The channel length is then reduced to $L - d$ and the voltage drop along the whole channel to $V_c - V_D$. In the gradual channel approximation, the drain current is given by Eq. (15) where $V(x)$ is the potential at a distance x from the source:

$$I_D = W C_i \mu [V_G - V_T - V(x)] \frac{dV}{dx} \tag{15}$$

Integrating Eq. (15) along the channel yields:

$$I_D = C_i \mu \frac{W}{L - d} \left\{ (V_G - V_T)V_D - \frac{V_D^2}{2} - \left[(V_G - V_T)V_c - \frac{V_c^2}{2} \right] \right\} \tag{16}$$

For an ohmic contact resistance ($V_c = R_c I_D$) and $d \ll L$, Eq. (16) reduces to Eq. (14). While the two previous analyses [35, 36] assumed constant contact resistance and gate voltage-dependent mobility, Street and coworkers make the assumption that the mobility is constant and find a non-ohmic contact resistance that varies with gate voltage.
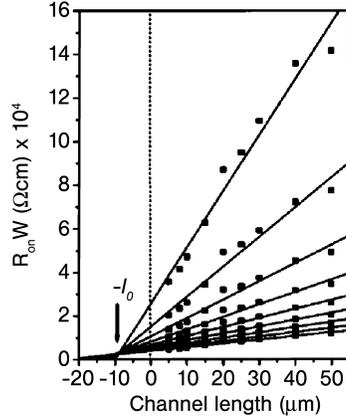
Fig. 1.12. Width-normalized resistance as a function of channel length at gate voltages ranging from −20 to −100 V [39].

At this stage, a technique that would enable independent access to the channel and contact resistances is needed. Such a feature is offered by the transfer line method (TLM) [38–41, 89], a method adapted from a classical technique use to estimate contact resistance, and first developed for the amorphous silicon thin-film transistor [42]. The method consists of measuring the channel resistance for different channel lengths. The measured resistance is actually the sum of the channel and contact resistances. As long as the measurement is performed in the linear regime (small drain voltage) the channel resistance is proportional to L (see Eq. 1) and the width-normalized ($R \times W$) total resistance is given by:

$$R \times W = \frac{L}{C_i \mu (V_G - V_T)} + R_c \times W \tag{17}$$

The contact resistance is extracted by plotting the width normalized resistance as a function of channel length. Extrapolation to zero length readily gives the contact resistance, while the slope of the curve can be used to extract device properties. The method is exemplified in Fig. 1.12 (taken from Ref. [39]). Each line corresponds to a given gate voltage. Figure 1.13 shows that the contact resistance is indeed gate voltage-dependent as assumed by Street [37]. It actually strongly decreases when the gate voltage increases. Extracting the mobility from the slope of the lines is not that easy, because this factor actually contains two parameters, mobility and threshold voltage, so a method of estimating the threshold voltage must first be found. It has, however, also been shown that the mobility is gate voltage-dependent [43, 44], even if the exact dependency cannot be undoubtedly determined from the TLM.
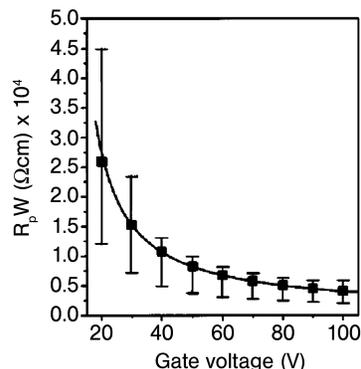
Fig. 1.13. Gate voltage-dependent contact resistance as deduced from the data in Fig. 1.11 [39].

Apart from problems in determining the mobility, the TLM has several other drawbacks. First, it requires measurements on different devices and it cannot be taken for granted that the channel and contact resistances are strictly similar for all of them, even if they are prepared during the same run. This is the reason why scattering occurs when plotting the data, as shown in Fig. 1.12. Next, the validity of Eq. (17) requires contact resistance not to depart from Ohm's law. In other words, the method cannot be used if contact resistance is non-linear. It must also be noted that, as the method requires measurements in the linear regime, that is, at low drain voltages, it is very sensitive to leaks through the insulator. Finally, the method cannot be used to make a distinction between the contact resistance at the source and that at the drain. This last point is important – theoretical modeling has shown that for ideal contacts all the ohmic drop should occur at the source electrode. As we shall see in the following discussion, this is not observed by use of other methods.

An alternative method to TLM is the four-point probe, which consists of introducing into the conducting channel two additional electrodes [45, 46]. The current remains the same all along the channel and the voltage drop between these two additional electrodes is not affected by the contact resistance, thus giving access to the true channel resistance. Moreover, as shown in Fig. 1.14, the contact resistance at each side of the channel can now be estimated independently.

An even more powerful technique makes use of an atomic force microscope (AFM) tip to probe the potential along the channel of the transistor [47, 48]. The technique and its results have been analyzed in detail by Bürgi et al. [49]. A variety of semiconductors and metals have been studied. The main features can be summarized as follows:

1. As expected, the contact resistance strongly depends on the nature of the electrode, e.g. its work function;
2. Contact resistance is gate-bias-dependent; it decreases substantially when gate
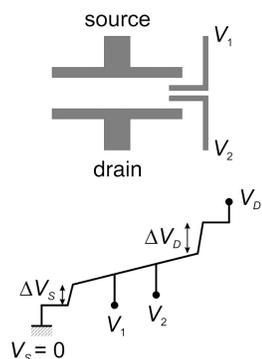
Fig. 1.14. Electrode pattern for a four-probe set up. The corresponding voltage profile along the conducting channel is shown in the bottom part of the figure.

bias is increased. This confirms what has been observed both with the TLM and by use of the four-point technique; and
3. Mobility is gate-bias-dependent.

Experiments were also conducted to study the effect of the nature of the contact on the respective part of the voltage drop at source and drain. This point will be dealt with in the next section.

1.3.2
Origin of Contact Resistance

The image most commonly used to describe source and drain contacts is that of a metal–semiconductor junction. According to the conventional Mott–Schottky (MS) model, contacts are expected to be ohmic when the work function of the metal is close to the HOMO or LUMO level of the semiconductor, depending on whether the semiconductor is p or n-type. If the reverse situation prevails, an energy barrier forms at the metal–semiconductor interface, leading to poor charge injection. From this standpoint, the Au/pentacene interface would be a good candidate as a low-resistance contact. In practice, the actual resistance is rather high. The mechanism of barrier formation at metal–organic semiconductor interfaces has been studied in great detail for organic light-emitting diodes (OLEDs), for which contact resistance is also a crucial issue. UV photoelectron spectroscopy (UPS) and inverse UPS have been used for precise determination of the energy levels at both side of the interface [50]. A typical result for the Au/pentacene interface is shown in Fig. 15, which clearly shows that the actual interface strongly deviates from the MS model. Instead, the interface has an additional ''dipole'' barrier, Δ, which shifts the HOMO level downward by more than 1 eV, hence increasing the barrier height by the same amount. The reason for this rather large interface dipole is that the electron density at a metal surface presents a tail that extends from the metal-free
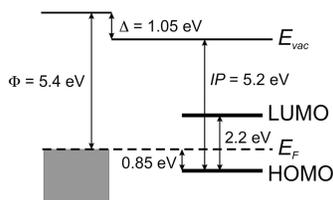
Fig. 1.15. Actual energy level diagram of the Au/pentacene interface. The position of the HOMO and the dipole barrier Δ are estimated from photoelectron spectroscopy [50].

surface into vacuum, thus forming a dipole pointing at the metal bulk. Molecules deposited on the metal tend to push back this tail, thus reducing the surface dipole and reducing the work function of the metal.

The above-described four-probe [45, 46] and scanning probe [47–49] techniques enable separate determination of the source and drain contact resistances. If contacts do behave as Schottky barriers, one would expect the voltage drop at source be substantially higher than that at drain. This is what is indeed observed with "bad" contacts. For "good" contacts, however, comparable drops are observed at both electrodes. A possible origin of this behavior has recently been suggested [51]. The model assumes the region immediately adjacent to the electrodes is made of organic material of quality different from that of the rest of the conducting channel, with very low mobility.

It is worth remarking that the contact resistance of the top contacts is usually lower than that of bottom contacts. The asymmetry of the organic-metal contact, depending on whether the organic film is deposited on the metal or the metal on the organic layer, has been studied both theoretically [52] and experimentally [53]. For example, combined UPS and XPS measurements have revealed signs of metal penetration and the formation of metal clusters after deposition of gold on top of a pentacene layer, leading to a substantial reduction of the interface barrier from 1 to 0.3 eV.

1.4
Charge Transport

Despite impressive progress in organic thin-film transistors during the past two or three decades, charge transport in organic materials remains a highly controversial topic. Basically, one can make a distinction between two families of charge-transport models. The first pertains to disordered materials, for example polymers. Models that belong to this family are based on hopping transport. An archetypal model of this group is that developed by Vissenberg and Matters [54], which assumes variable range hopping in an exponential distribution of traps. The model predicts a thermally activated mobility. It also predicts that mobility depends on

the gate voltage according to a power law, a feature that is, indeed, observed in actual devices (Eq. 13), so this prediction has proved very fruitful in the analysis of current-voltage curves of OTFTs.

Dealing with well-organized molecular crystals seems much more difficult. On the basis of the inverse power law dependence of mobility on temperature (that is, mobility increases when temperature decreases) found in highly pure crystals from time-of-flight measurements [55], it is often stated that charge transport in these materials occurs via charge-carriers in delocalized states, as in conventional semiconductors. The statement does not withstand analysis, however. Except at very low temperatures, the corresponding mean free path does not exceed the intermolecular distance [56], which is not compatible with a diffusion-limited process. Although polarons have been invoked to resolve the discrepancy [56, 57], the theoretical problem is very intricate, because useful approximations used with inorganic materials, for example the one-electron limit, are no longer valid, so one must deal with huge numbers of atoms and molecules. Despite recent efforts [60–63], basic problems, for example the ultimate value of the mobility and its temperature dependence, have not been satisfactorily resolved.

An interesting aspect is the gate voltage-dependent mobility. Such dependence is predicted by the Vissenberg's model [54] and has indeed been observed in most devices made of polymers. Briefly, the dependence stems from the fact that as the gate voltage increases, injected charge-carriers tend to fill the traps, so trapping becomes less efficient and charge transport improves. Interestingly enough, similar gate-voltage dependence was reported for early devices made of small molecules. To account for that, a parent model has been developed that assumes delocalized transport limited by a distribution of traps near the band edge [64]. The model is derived from the multiple trapping and release (MTR) model developed for a-Si:H [65]. The model also predicts thermally activated mobility, which, again, was found in most early devices. It is worth pointing out that as the quality of the devices improves, both of these features (gate bias dependent and thermally activated mobility) tend to be encountered less, which tends to confirm they indeed originate from defects. This is particularly true for single-crystal devices, as will be dealt with below.

1.5
Fabrication Techniques

Organic semiconductors are so different from their inorganic analogs in terms of melting point, solubility, and mechanical properties that it is not conceivable that the fabrication techniques of conventional microelectronics would be appropriate for making organic devices. Nevertheless, these technologies are so powerful and well mastered that in the early days of OTFTs it seemed more convenient to take advantage of techniques such as thermal oxidation and photolithography, so most of the devices were actually derived from standard silicon technology. In most instances, organic transistors consisted of highly doped silicon wafers that served as

the gate with thermally grown oxide as insulator and lithographically patterned source and drain. Deposition of the organic semiconductor was performed at the last step of the process, either by casting from solution or from the vapor phase.

Of course, such fabrication processes are not appropriate for taking advantage of the potential of organic materials, for example low cost, large area, and the possibility of using flexible substrates. In the following discussion we will focus on different printing techniques that have been used for the fabrication of OTFTs.

Earlier work made use of screen-printing. The major elements of the device were deposited from solutions through stainless-steel mechanical masks [58, 59]. Although this simple technique afforded devices whose performance compared well with those fabricated by ''conventional'' techniques, it was of much less interest for production of highly integrated circuits. Typical space resolution for screen-printing falls in the 35–100 μm range – several times larger than the critical length needed for realistic applications. To circumvent this problem, a group at Bell Laboratories developed a strategy using high resolution printing with resolution down to 2 μm [66]. Microcontact printing uses elastomeric stamps to print patterns of self-assembled monolayers (SAMs) that are then used either as resists to prevent removal of a pre-deposited material, or as initiators to promote material deposition [67]. The transistor follows a top-gate geometry, in which fabrication starts with deposition of a gold layer on the appropriately prepared substrate. A specifically designed stamp is used to produce the patterned SAM. Then, etching the gold not protected by the SAM is used to define the source and drain electrodes. The SAM is next removed with heat, ultraviolet light, or an oxygen plasma to expose the bare gold. The semiconductor (regio-regular poly(3-hexylthiophene); P3HT), insulator (poly(methyl methacrylate); PMMA), and gate electrode (carbon ink) are sequentially cast from solution. Interestingly, the technique can be extended to reel-to-reel fabrication by making use of cylindrical stamps.

Inkjet printing is an alternative printing technique that is widely used to fabricate organic light-emitting diodes [68, 69] and full-color displays [70]. The main problem with applying the technique to OTFTs is size resolution limited to 20–50 μm, because of spreading of the droplets on the substrate. A group at Cambridge University (UK) recently succeeded in overcoming the problem by confining the spreading of the water-based ink with a pattern of repelling, hydrophobic regions that define the device dimensions [71]. The pattern was fabricated by photolithography and oxygen plasma etching of a polyimide film. Again, the device was fabricated with a top-gate configuration. The elements, deposited in sequence, are: inkjet-printed source and drain (polyethylenedioxythiophene doped with polystyrene sulfonate; PEDOT–PSS), semiconductor (dioctylfluorene–bithiophene copolymer; F8T2), and insulator (polyvinylphenol; PVP).

Stamping and inkjet printing both require liquid inks, which may be a problem when dealing with conjugated polymers and small molecules. To surmount this drawback, a dry process based on thermal imaging has been developed at DuPont. The technique has been claimed to enable the patterning of organic materials at high speed and with micron size resolution [72]. It involves the transfer of a thin solid layer from a donor film on to a flexible receiver. The two flexible films are

held together by vacuum. The heat is produced by a laser beam focused through the donor base at a thin metal layer. Conversion of light to heat converts the surrounding materials into gaseous products, whose expansion propels the top layer from the donor to the receiver. Not all conducting polymers can withstand the heat generated during the process, however. Good results were obtained with a polyaniline synthesized by emulsion polymerization and doped with dinonyl naphthalene sulfonic acid (DNNSA-PANI) that may constitute the source and drain electrodes. The possibility of transferring organic semiconductors has not yet been established, however. Transistors with a bottom gate configuration have been fabricated on Mylar substrates. The gate was an indium tin oxide (ITO) film on which a spin-coated glass resin served as the insulator. Heat-transferred DNNSA-PANI source and drain electrodes and vapor-deposited pentacene completed the structure. A TFT backplane containing 5000 transistors with 20 µm channel length could thus be realized on a $50 \times 80 \ cm^{-2}$ flexible substrate.

1.6
The Materials

Organic semiconductors are traditionally classified as polymers or small molecules. The former have the advantage of being amenable to specific deposition techniques that have been developed for long for conventional polymers. Their performance is still orders of magnitude lower than that of small molecules, however. Encouraging performance has been reported with the latter, although high performance requires high ordering, particularly in the vicinity of the insulator–semiconductor interface. The importance of high ordering has been recently confirmed by measurements on single crystal devices.

1.6.1
Polymers

Two polymers are used for most work dealing with polymer-based OTFTs – polyfluorene [37, 73] and poly(3-alkylthiophene) (P3AT). We will only deal with the latter, which afford the highest mobility.

After pioneering work by Sirringhaus et al. [74] on spin-coated P3AT, it is now well established that the performance of polymer OTFTs critically depends on the chemical and structural ordering of the chains at the insulator–polymer interface. High order first relies on the regio-regularity of the polymer chains; that is, the percentage of regio-regular head-to-tail attachment of the alkyl side chains to the beta position of the thiophene rings. High regio-regularity is not sufficient, however. Two orientations are observed, one with the thiophene rings flat on the surface and the other with the chain edge-on (Fig. 16). High mobility, up to 0.1 $cm^2 \ V^{-1} \ s^{-1}$ was only found with the latter arrangement.

More recently it has been shown that the mobility can be slightly increased if the film is applied by dip-coating instead of spin-coating. Under these conditions the
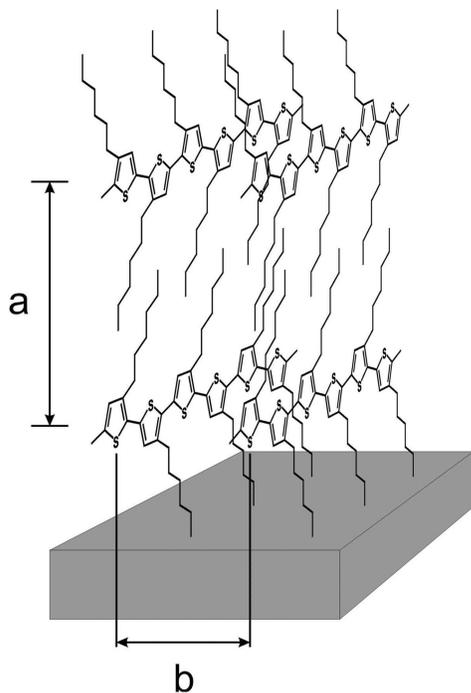
Fig. 1.16. Regio-regular poly-3-hexylthiophene with edge-on orientation of the polymer chains. Redrawn from Ref. [74].

thickness of the film could be reduced to 2–4 nm [75]. It must be remarked that the factors affecting orientation of the polymer chains on the substrate are not fully understood.

1.6.2
Small Molecules

Pentacene is the material most used for preparation of p-type OTFTs based on small molecules, with oligothiophenes and their derivatives being the nest most important. The highest reported mobility is up to 6 cm^2 V^{-1} s^{-1} for the former [76] and 1 cm^2 V^{-1} s^{-1} for the latter [77].

Major improvements have been achieved by modification of the insulator–semiconductor interface. Most devices are grown by vapor deposition on silicon oxide. Because of the different physical and chemical nature of both materials, their association may lead to highly disordered interfaces, thus leading to poor performance. Heating the substrate [27, 78, 79] and depositing at a low rate [30, 78]

leads to better organization. A better alternative, however, consists in covering the surface of the oxide with an organic monomolecular layer before vapor deposition. Thus, octadecyltrichlorosilane (OTS) [80] gave good results with pentacene on SiO_2. Even better results have been claimed after use of an ultrathin film of polystyrene [76]. An alternative route is to use a polymer dielectric, which resulted in high performance with sexithiophene derivatives [77].

1.6.3
n-Type Semiconductors

As stated above, the notions of n and p-type do not have the same meaning as for inorganic semiconductors. At the current state of the art, an organic n-type material is one in which electrons are more easily injected than holes. This is therefore more a matter of HOMO and LUMO energy level rather than possibility of doping. In other words, an n-type organic semiconductor is characterized by high electron affinity.

The compounds with the highest electron mobility are currently fullerene C_{60} [81, 82] and *N*,*N*4-dialkyl-3,4,9,10-perylene tetracarboxylic diimide derivatives [83, 84], with values up to 0.5 cm^2 V^{-1} s^{-1}. A major problem with these compounds is their high sensitivity to ambient conditions, especially oxygen and moisture. A small number of air-stable n-type compounds have been reported [85–88]. All are perfluorinated and their mobility does not exceed a few tenths of 1 cm^2 V^{-1} s^{-1}.

A prominent aspect that promotes the search for air-stable, high-mobility n-type organic semiconductors is the possibility of access to complementary circuitry. It must be recalled that CMOS architecture is a corner stone of microelectronics. Making circuits that combine n-channel and p-channel transistors has many advantages – high robustness, low power consumption, and low noise. A new concept has recently emerged in the field of organic thin-film transistors, that of ambipolar materials, which can be defined as materials that change type depending on the nature of the contact used to inject charges. Ideally, an ambipolar semiconductor would have a low ionization potential and high electron affinity. An elegant way of realizing an ambipolar compound has been discovered by a group at Eindhoven [89]. It consists in making an interpenetrating network of two compounds, one n-type and one p-type. The former was a derivative of C_{60} (6,6-phenyl C_{61}-butyric acid methyl ester, PCBM) and the latter was either regio-regular P3HT or a derivative of poly-*p*-phenylenevinylene (PPV). The group also showed that pristine pentacene could also have ambipolar behavior. It must, however, be stressed that this concept is highly controversial. Some have pointed out that complementary circuitry requires that one transistor be off while the other is on, and vice versa. Accordingly, an ambipolar material that will conduct holes for negative gate voltages and electrons for positive gate voltages will only turn off for a very limited voltage range, or for no voltage at all. This seems detrimental for any practical circuit. Separate use of a purely n-type and purely p-type compound seems a much wiser approach.

1.6.4
Single Crystals

Until recently, reports on single-crystal OTFTs were rather scarce [90, 91]. The difficulties in building a single crystal OTFT are numerous. Single crystals of organic materials useful for making OTFTs are small, fragile, and difficult to handle. The standard fabrication technique for OTFTs, which consists of depositing a semiconductor film on top of the insulator from either the vapor phase or a solution, cannot be extended to single crystals. Furthermore, many conventional fabrication processes may damage the surface of the crystal. For these reasons, the OTFT must be made of already grown crystals. To date, only two techniques have been successfully used.

1. Electrostatic bonding of the crystal on top of a previously prepared gate-insulator-source-drain structure [92–94]. Sometimes the source and drain contacts have been deposited afterwards, on top of the crystal [90].
2. Direct deposition of the contacts and gate insulator on to the crystal [95, 96]. In this technique the gate dielectric is the polymer parylene, which forms conformal coatings with good dielectric and mechanical properties. The polymer is deposited in a three-zone reactor, in which the deposition zone can be kept at room temperature.

These techniques have recently been reviewed [97] and will not be discussed further here. Instead, we will focus on the electrical characteristics of single-crystal OTFTs.

Because the concentration of defects is much lower in single crystals than in vapor-deposited or solution cast films, the main motivation in fabricating single crystal OTFTs was to explore the physical limitations on the performance of the device, with the hope of approaching the ultimate properties of the materials. Pentacene was somewhat disappointing – the highest reported single-crystal mobility was several times lower than for the best polycrystalline films. This is because the crystal structure in thin films (the so-called "thin-film" form) is slightly different from that in single crystals [98]. More encouraging results were obtained with tetracene (also called "naphthacene"), a parent molecule of pentacene made of four fused benzene rings instead of five, and even more with rubrene, the molecule of which consists of a tetracene core with four pendant benzene rings. The molecular formulas of tetracene and rubrene are given in Fig. 1.17.

Comparing single crystal and vapor-grown devices for these two compounds is difficult, because reports on evaporated tetracene OTFTs are rather scarce [99–101], and despite several (unpublished) attempts, fabrication of an operating thin-film device from rubrene has not yet been successfully achieved. For both compounds the problem seems to arise from an improper deposition mechanism, which, in contrast with experience with pentacene and sexithiophene, does not favor two-dimensional growth.

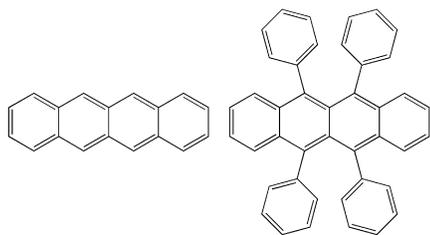Prominent features of these single crystal devices are [102]:

Fig. 1.17. Molecular structures of tetracene (left) and rubrene (right).

1. unexpectedly high mobility (up to 20 cm^2 V^{-1} s^{-1} for rubrene at room temperature);
2. an inversion in the temperature dependence; that is, mobility tends to increase when the temperature is reduced from room temperature to ca. 280 K for tetracene and 200 K for rubrene, at which point the tendency is reversed; and
3. anisotropic mobility depending on the crystal axis.

All these features are reminiscent of results obtained from time-of-flight measurements on highly pure molecular crystals (Section 1.4). This might indicate of that the intrinsic properties of these materials are being approached.

1.6.5
Insulators

It has long been known that in an insulated gate field-effect transistor, the role of the insulator is at least as important as that of the semiconductor. For historical reasons, most of the OTFTs made so far have used inorganic dielectrics, mostly silicon oxide. We have already mentioned (Section 1.6.2) that the quality of the insulator–semiconductor interface, and hence the performance of the device, can be significantly improved by inserting an organic single layer between the insulator and the semiconductor. It seems that the performance of the OTFT is very much dependent on the physical and chemical nature of the surface of the insulator. In this respect organic insulators seem to be more flexible than their inorganic counterparts.

The nature of the insulator may intervene at different levels. First, in the bottom configuration, the insulator is capable of affecting the morphology of the semiconductor layer. For instance, its surface energy strongly affects the nucleation and growth mechanism of vapor-deposited films. According to the standard nucleation and growth models, it is expected that the nucleation rate increases, and thus the size of the grains decreases, with increasing surface energy. An archetypal example of this behavior is vapor deposition of pentacene on hydrogenated silicon (a low-energy surface) compared with silicon oxide (a high-energy surface); the nucleation rate was found to be several orders of magnitude higher on the former than on the latter [103, 104]. Similar studies on organic insulators have not yet been conducted,

but would be of great interest in that respect. At this point, it is worth remarking that the effect of grain size on the performance of OTFTs is currently the subject of much debate. On the basis of conventional theories on charge transport in polycrystalline semiconductors it can be expected that mobility increases with grain size. This can be simply understood by noting that charge transport in polycrystalline media is limited by grain boundaries, so that as the grain size increases the number of grain boundaries decreases, leading to improved transport. Although this seems, indeed, to be observed for oligothiophenes, according to an early report [105], several results prove the opposite is true for pentacene [106, 107].

Besides its morphological effects, the nature of the insulator may also have chemical and electrical consequences. It has recently been claimed that the dipole field present at the surface of high dielectric constant (high-*k*) insulators may enhance the formation of local states that in turn induce carrier localization and reduce charge-carrier mobility. Hence, benefits have resulted from use of low-*k* organic dielectrics [108]. It is worth remarking that such a conclusion is at variance with previous work that established interest in using high-capacitance insulators, which can be obtained by making use of high-*k* dielectrics [109]. Interest in high capacitance comes from the above mentioned gate voltage (actually, charge density) dependence of the mobility. High capacitance means that high charge-carrier concentration can be reached at low gate voltage, hence mobility is expected to be higher. The respective advantages of low-*k* and high-*k* dielectrics thus seem contradictory, and more work will be necessary to clarify this point.

1.7
Concluding Remarks

The organic thin-film transistor is at a pivotal point of its history. The number of research teams that have embarked in the field has blossomed in recent years. Several important features have been uncovered or confirmed, for example the crucial role of the quality of the semiconductor at the insulator–semiconductor interface and of the resistance of the source-drain contacts. The advent of the single-crystal device has enabled charge-carrier mobility to be increased to even higher values than that reported for highly pure molecular crystal, at least at room temperature. Fundamentally, the main issue with organic thin-film transistors is the lack of reliable model for predicting the charge-transfer properties of a given molecular material. It has been largely confirmed that the performance of the device is mostly governed by the structure of the semiconductor film at the insulator–semiconductor interface. In that respect, the role of the insulator is at least as important as that of the semiconductor. This is exemplified by recalling that silicon is the universal element used in microelectronics not so much because of the intrinsic properties of the material but because of the almost perfect interface it forms with its thermally grown oxide. For this reason, the major challenge in the development of OTFTs is now to identify suitable organic insulator–semiconductor combinations rather than semiconductors by themselves.

Acknowledgements

References

1 J. E. Lilienfeld, US Patent 1,745,175, **1930**.

2 D. Kahng, M. M. Atalla, in *IRE Solid-State Devices Research Conference*, Pittsburgh, PA, **1960**; D. Kahng, US Patent 3,102,230, 1963.

3 P. K. Weimer, *Proc. IRE* **1962**, *50*, 1462–1469.

4 W. E. Spear, P. G. Le Comber, *J. Non-Cryst. Solids* **1972**, *8–10*, 727–738.

5 G. W. Neudeck, A. K. Malhotra, *Solid-State Electron.* **1976**, *19*, 721–729.

6 M. Pope, C. E. Swenberg, *Electronic Processes in Organic Crystals and Polymers*, Oxford University Press, New York, **1999**.

7 D. F. Barbe, C. R. Westgate, *J. Phys. Chem. Solids* **1970**, *31*, 2679–2687.

8 M. L. Petrova, L. D. Rozenshtein, *Fiz. Tverd. Tela (Soviet Phys. Solid State)* **1970**, *12*, 961–962 (756–757).

9 F. Ebisawa, T. Kurokawa, S. Nara, *J. Appl. Phys.* **1983**, *54*, 3255–3259.

10 A. Tsumura, K. Koezuka, T. Ando, *Appl. Phys. Lett.* **1986**, *49*, 1210–1212.

11 A. Tsumura, H. Koezuka, Y. Ando, *Synth. Metal* **1988**, *25*, 11–23.

12 G. Horowitz, D. Fichou, X. Z. Peng, Z. G. Xu, F. Garnier, *Solid State Commun.* **1989**, *72*, 381–384.

13 G. Horowitz, X. Z. Peng, D. Fichou, F. Garnier, *J. Appl. Phys.* **1990**, *67*, 528–532.

14 H. E. Katz, *J. Mater. Chem.* **1997**, *7*, 369–376.

15 A. R. Brown, C. P. Jarrett, D. M. de Leeuw, M. Matters, *Synth. Metal.* **1997**, *88*, 37–55.

16 F. Garnier, *Chem. Phys.* **1998**, *227*, 253–262.

17 G. Horowitz, *Adv. Mater.* **1998**, *10*, 365–377.

18 C. D. Dimitrakopoulos, P. R. L. Malenfant, *Adv. Mater.* **2002**, *14*, 99–117.

19 Y. Y. Lin, D. J. Gundlach, S. F. Nelson, T. N. Jackson, *IEEE Electron. Device Lett.* **1997**, *18*, 606–608.

20 P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, S. D. Theiss, *Appl. Phys. Lett.* **2003**, *82*, 3964–3966.

21 J. Koenigsberger, J. Weiss, *Ann. Phys.* **1911**, *35*, 1–46.

22 An enlightening history of the emergence of semiconductors can be found in: F. A. Stahl, *Am. J. Phys.* **2003**, *71*, 1170–1173.

23 http://en.wikipedia.org/wiki/Semiconductor.

24 A. Kahn, N. Koch, W. Gao, *J. Polym. Sci. B, Polym. Phys.* **2003**, *41*, 2529–2548.

25 R. B. Campbell, J. M. Robertson, J. Trotter, *Acta Cryst.* **1961**, *14*, 705–711.

26 D. Holmes, S. Kumaraswamy, A. J. Matzger, K. P. C. Vollhardt, *Chem. Eur. J.* **1999**, *5*, 3399–3412.

27 B. Servet, G. Horowitz, S. Ries, O.

LAGORSSE, P. ALNOT, A. YASSAR, F.
DELOFFRE, P. SRIVASTAVA, R.
HAJLAOUI, P. LANG, F. GARNIER,
Chem. Mater. **1994**, *6*, 1809–1815.

28 F. GARNIER, A. YASSAR, R. HAJLAOUI,
G. HOROWITZ, F. DELOFFRE, B.
SERVET, S. RIES, P. ALNOT, *J. Am.
Chem. Soc.* **1993**, *115*, 8716–8721.

29 T. MINAKATA, I. NAGOYA, M. OZAKI,
J. Appl. Phys. **1991**, *69*, 7354–7356.

30 C. D. DIMITRAKOPOULOS, A. R.
BROWN, A. POMP, *J. Appl. Phys.* **1996**,
80, 2501–2508.

31 C. TANASE, E. J. MEIJER, P. W. M.
BLOM, D. M. DE LEEUW, *Org. Electron.*
2003, *4*, 33–37.

32 N. F. MOTT, R. W. GURNEY, *Electronic
Processes in Ionic Crystals*, Clarendon
Press, Oxford, **1940**.

33 J. C. SANCHO-GARCIA, G. HOROWITZ,
J. L. BREDAS, J. CORNIL, *J. Chem. Phys.*
2003, *119*, 12563–12568.

34 A. DODABALAPUR, L. TORSI, H. E.
KATZ, *Science* **1995**, *268*, 270–271.

35 P. V. NECLIUDOV, M. S. SHUR, D. J.
GUNDLACH, T. N. JACKSON, *J. Appl.
Phys.* **2000**, *88*, 6594–6597.

36 G. HOROWITZ, M. E. HAJLAOUI, R.
HAJLAOUI, *J. Appl. Phys.* **2000**, *87*,
4456–4463.

37 R. A. STREET, A. SALLEO, *Appl. Phys.
Lett.* **2002**, *81*, 2887–2889.

38 P. V. NECLIUDOV, M. S. SHUR, D. J.
GUNDLACH, T. N. JACKSON, *Solid-State
Electron.* **2003**, *47*, 259–262.

39 J. ZAUMSEIL, K. W. BALDWIN, J. A.
ROGERS, *J. Appl. Phys.* **2003**, *93*, 6117–
6124.

40 H. KLAUK, G. SCHMID, W. RADLIK, W.
WEBER, L. ZHOU, C. D. SHERAW, J. A.
NICHOLS, T. N. JACKSON, *Solid-State
Electron.* **2003**, *47*, 297–301.

41 E. J. MEIJER, G. H. GELINCK, E. VAN
VEENENDAAL, B. H. HUISMAN, D. M.
DE LEEUW, T. M. KLAPWIJK, *Appl. Phys.
Lett.* **2003**, *82*, 4576–4578.

42 S. LUAN, G. W. NEUDECK, *J. Appl.
Phys.* **1992**, *72*, 766–772.

43 G. HOROWITZ, P. LANG, M. MOTTAGHI,
H. AUBIN, *Adv. Funct. Mater.* **2004**, *14*,
1069–1074.

44 W. KALB, P. LANG, M. MOTTAGHI, H.
AUBIN, G. HOROWITZ, M. WUTTIG,
Synth. Metal. **2004**, *146*, 279–282.

45 R. J. CHESTERFIELD, J. C. MCKEEN,
C. R. NEWMAN, C. D. FRISBIE,
P. C. EWBANK, K. R. MANN, L. L.
MILLER, *J. Appl. Phys.* **2004**, *95*,
6396–6405.

46 I. YAGI, K. TSUKAGOSHI, Y. AOYAGI,
Appl. Phys. Lett. **2004**, *84*, 813–815.

47 K. SESHADRI, C. D. FRISBIE, *Appl.
Phys. Lett.* **2001**, *78*, 993–995.

48 L. BÜRGI, H. SIRRINGHAUS, R. H.
FRIEND, *Appl. Phys. Lett.* **2002**, *80*,
2913–2915.

49 L. BÜRGI, T. J. RICHARDS, R. H.
FRIEND, H. SIRRINGHAUS, *J. Appl.
Phys.* **2003**, *94*, 6129–6137.

50 N. KOCH, A. KAHN, J. GHIJSEN, J.-J.
PIREAUX, J. SCHWARTZ, R. L. JOHNSON,
A. ELSCHNER, *Appl. Surf. Sci.* **2003**, *82*,
70–72.

51 T. LI, P. P. RUDEN, I. H. CAMPBELL,
D. L. SMITH, *J. Appl. Phys.* **2003**, *93*,
4017–4022.

52 N. TESSLER, Y. ROICHMAN, *Appl. Phys.
Lett.* **2001**, *79*, 2987–2989.

53 N. J. WATKINS, L. YAN, Y. GAO, *Appl.
Phys. Lett.* **2002**, *80*, 4384–4386.

54 M. C. J. M. VISSENBERG, M. MATTERS,
Phys. Rev. B **1998**, *57*, 12964–12967.

55 N. KARL, J. MARKTANNER, R. STEHLE,
W. WARTA, *Synth. Metal.* **1991**, *42*,
2473–2481.

56 E. A. SILINSH, V. CÁPEK, *Organic
molecular crystals: Interaction,
localization, and transport phenomena*,
AIP Press, New York, **1994**.

57 V. M. KENKRE, J. D. ANDERSEN, D. H.
DUNLAP, C. B. DUKE, *Phys. Rev. Lett.*
1989, *62*, 1165–1168.

58 F. GARNIER, R. HAJLAOUI, A. YASSAR,
P. SRIVASTAVA, *Science* **1994**, *265*,
1684–1686.

59 Z. N. BAO, Y. FENG, A. DODABALAPUR,
V. R. RAJU, A. J. LOVINGER, *Chem.
Mater.* **1997**, *9*, 1299.

60 J. L. BRÉDAS, D. BELJONNE, J. CORNIL,
J. P. CALBERT, Z. SHUAI, R. SILBEY,
Synth. Metal. **2002**, *125*, 107–116.

61 R. C. HADDON, X. CHI, M. E. ITKIS,
J. E. ANTHONY, D. L. EATON, T.
SIEGRIST, C. C. MATTHEUS, T. T. M.
PALSTRA, *J. Phys. Chem. B* **2002**, *106*,
8288–8292.

62 Y. C. CHENG, R. J. SILBEY, D. A. DA
SILVA, J. P. CALBERT, J. CORNIL, J. L.

Brdas, *J. Chem. Phys.* **2003**, *118*, 3764–3774.

63 L. Giuggioli, J. D. Andersen, V. M. Kenkre, *Phys. Rev. B* **2003**, *67*, 045110.

64 G. Horowitz, R. Hajlaoui, P. Delannoy, *J. Phys. III France* **1995**, *5*, 355–371.

65 P. G. Le Comber, W. E. Spear, *Phys. Rev. Lett.* **1970**, *25*, 509–511.

66 J. A. Rogers, Z. N. Bao, A. Makhija, P. Braun, *Adv. Mater.* **1999**, *11*, 741–745.

67 Y. Xia, G. M. Whitesides, *Angew. Chem. Int. Ed.* **1998**, *37*, 550–575.

68 T. R. Hebner, C. C. Wu, D. Marcy, M. H. Lu, J. C. Sturm, *Appl. Phys. Lett.* **1998**, *72*, 519–521.

69 Y. Yang, S. C. Chang, J. Bharathan, J. Liu, *J. Mater. Sci. Mater. Electron.* **2000**, *11*, 89–96.

70 O. Yokoyama, *Optronics* **2003**, *254*, 119–122.

71 H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, E. P. Woo, *Science* **2000**, *290*, 2123–2126.

72 G. B. Blanchet, Y. L. Loo, J. A. Rogers, F. Gao, C. R. Fincher, *Appl. Phys. Lett.* **2003**, *82*, 463–465.

73 H. Sirringhaus, R. J. Wilson, R. H. Friend, M. Inbasekaran, W. Wu, E. P. Woo, M. Grell, D. D. C. Bradley, *Appl. Phys. Lett.* **2000**, *77*, 406–408.

74 H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveldvoss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwig, D. M. de Leeuw, Nature **1999**, *401*, 685–688.

75 G. M. Wang, J. Swensen, D. Moses, A. J. Heeger, *J. Appl. Phys.* **2003**, *93*, 6137–6141.

76 T. W. Kelley, D. V. Muyres, P. F. Baude, T. P. Smith, T. D. Jones, *MRS Symp. Proc.* **2003**, *771*, 169–179.

77 M. Halik, H. Klauk, U. Zschieschang, G. Schmid, S. Ponomarenko, S. Kirchmeyer, W. Weber, *Adv. Mater.* **2003**, *15*, 917–922.

78 D. J. Gundlach, Y. Y. Lin, T. N. Jackson, S. F. Nelson, D. G. Schlom, *IEEE Electron. Device Lett.* **1997**, *18*, 87–89.

79 W. A. Schoonveld, R. W. Stok, J. W. Weijtmans, J. Vrijmoeth, J. Wildeman, T. M. Klapwijk, *Synth. Metal.* **1997**, *84*, 583–584.

80 Y. Y. Lin, D. J. Gundlach, T. N. Jackson, S. F. Nelson, *IEEE Trans. Electron. Dev.* **1997**, *44*, 1325–1331.

81 C. P. Jarrett, K. Pichler, R. Newbould, R. H. Friend, *Synth. Metal.* **1996**, *77*, 35–38.

82 S. Kobayashi, T. Takenobu, S. Mori, A. Fujiwara, Y. Iwasa, *Appl. Phys. Lett.* **2003**, *82*, 4581–4583.

83 H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y. Y. Lin, A. Dodabalapur, *Nature* **2000**, *404*, 478–481.

84 P. R. L. Malenfant, C. D. Dimitrakopoulos, J. D. Gelorme, L. L. Kosbar, T. O. Graham, A. Curioni, W. Andreoni, *Appl. Phys. Lett.* **2002**, *80*, 2517–2519.

85 A. Facchetti, M. Mushrush, H. E. Katz, T. J. Marks, *Adv. Mater.* **2003**, *15*, 33–38.

86 H. Tada, H. Touda, M. Takada, K. Matsushige, *J. Porphyr. Phthalocyan.* **1999**, *3*, 667–671.

87 S. Hoshino, S. Nagamatsu, M. Chikamatsu, M. Misaki, Y. Yoshida, N. Tanigaki, K. Yase, *Synth. Metal.* **2003**, *137*, 953–954.

88 A. Facchetti, Y. Deng, A. C. Wang, Y. Koide, H. Sirringhaus, T. J. Marks, R. H. Friend, *Angew. Chem. Int. Ed.* **2000**, *39*, 4547–4551.

89 E. J. Meijer, D. M. De Leeuw, S. Setayesh, E. van Veenendaal, B. H. Huisman, P. W. M. Blom, J. C. Hummelen, U. Scherf, T. M. Klapwijk, *Nature Mater.* **2003**, *2*, 678–682.

90 G. Horowitz, F. Garnier, A. Yassar, R. Hajlaoui, F. Kouki, *Adv. Mater.* **1996**, *8*, 52–54.

91 M. Ichikawa, H. Yanagi, Y. Shimizu, S. Hotta, N. Suganuma, T. Koyama, Y. Taniguchi, *Adv. Mater.* **2002**, *14*, 1272–1275.

92 R. W. I. de Boer, T. M. Klapwijk, A. F. Morpurgo, *Appl. Phys. Lett.* **2003**, *83*, 4345–4347.

93 C. R. Newman, R. J. Chesterfield, J. A. Merlo, C. D. Frisbie, *Appl. Phys. Lett.* **2004**, *85*, 422–424.

94 C. Goldmann, S. Haas, C. Krellner, K. P. Pernstich, D. J. Gundlach, B. Batlogg, *J. Appl. Phys.* **2004**, *96*, 2080–2086.

95 V. Podzorov, V. M. Pudalov, M. E. Gershenson, *Appl. Phys. Lett.* **2003**, *82*, 1739–1741.

96 V. Y. Butko, X. Chi, D. V. Lang, A. P. Ramirez, *Appl. Phys. Lett.* **2003**, *83*, 4773–4775.

97 R. W. I. de Boer, M. E. Gershenson, A. F. Morpurgo, V. Podzorov, *Phys. Stat. Sol. (a)* **2004**, *201*, 1302–1331.

98 S. E. Fritz, S. M. Martin, C. D. Frisbie, M. D. Ward, M. F. Toney, *J. Am. Chem. Soc.* **2004**, *126*, 4084–4085.

99 D. J. Gundlach, J. A. Nichols, L. Zhou, T. N. Jackson, *Appl. Phys. Lett.* **2002**, *80*, 2925–2927.

100 A. Hepp, H. Heil, W. Weise, M. Ahles, R. Schmechel, H. von Seggern, *Phys. Rev. Lett.* **2003**, *91*, 157406.

101 C. Santato, R. Capelli, M. A. Loi, M. Murgia, F. Cicoira, V. A. L. Roy, P. Stallinga, R. Zamboni, C. Rost, S. F. Karg, M. Muccini, *Synth. Metal.* **2004**, *146*, 329–334.

102 V. Podzorov, E. Menard, A. Borissov, V. Kiryukhin, J. A. Rogers, M. E. Gershenson, *Phys. Rev. Lett.* **2004**, *93*, 086602.

103 F. J. Meyer zu Heringdorf, M. C. Reuter, R. M. Tromp, *Nature* **2001**, *412*, 517–520.

104 R. Ruiz, B. Nickel, N. Koch, L. C. Feldman, R. F. Haglund, A. Kahn, G. Scoles, *Phys. Rev. B* **2003**, *67*, 125406.

105 G. Horowitz, M. E. Hajlaoui, *Synth. Metal.* **2001**, *122*, 185–189.

106 D. Knipp, R. A. Street, A. Vlkel, J. Ho, *J. Appl. Phys.* **2003**, *93*, 347–355.

107 M. Shtein, J. Mapel, J. B. Benziger, S. R. Forrest, *Appl. Phys. Lett.* **2002**, *81*, 268–270.

108 J. Veres, S. D. Ogier, S. W. Leeming, D. C. Cupertino, S. M. Khaffaf, *Adv. Funct. Mater.* **2003**, *13*, 199–204.

109 C. D. Dimitrakopoulos, I. Kymissis, S. Purushothaman, D. A. Neumayer, P. R. Duncombe, R. B. Laibowitz, *Adv. Mater.* **1999**, *11*, 1372–1375.