

## 1

## Valve Metal, Si and Ceramic Oxides as Dielectric Films for Passive and Active Electronic Devices

Alexander Michaelis

## 1.1

### Introduction

Owing to their low electrochemical potential the group IVB and VB valve metals Ti, Zr, Hf, V, Nb and Ta readily react with water or oxygen to form a dense, protecting passive layer. This also holds for Al. Because of these protecting oxide films, the valve metals show an exceptional resistance towards corrosion in many aggressive environments. This explains why valve metals are widely used in the construction of chemical apparatus. An extensive number of papers and reviews exist that focus on the corrosion resistance of valve metal oxides [e.g. 1, 2].

In this treatise however another field is covered, namely the application of valve metals in electronics. The valve metal oxides show outstanding dielectric properties, which make them a key component in many passive and active devices such as capacitors, resistors and ICs (integrated circuits). Nevertheless, the most important oxide system in electronics is still Si/SiO<sub>2</sub>, which can be considered the bench mark system. Consequently, one chapter of this book is dedicated to Si/SiO<sub>2</sub> with special emphasis on its use in DRAM (dynamic random access memory) microchip fabrication, which can be considered the most advanced and demanding technology in microelectronics, as will be explained in Chapter 4. Electrochemically, p-Si/SiO<sub>2</sub> also behaves like a valve metal. Regarding their electronic properties, the valve metal oxides are related to another class of oxides, namely the perovskite structured ferroelectrics: BaTiO<sub>3</sub>, (Ba,Sr)TiO<sub>3</sub> (BST), Pb(Zr<sub>x</sub>Ti<sub>1-x</sub>)O<sub>3</sub> (PZT), SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> (SBT). These advanced electroceramics outperform the simple valve metal oxides in many respects, such as, by their exceptional high relative dielectric constant ( $\epsilon_r$ ) (sometimes also called relative permittivity). Therefore, both the valve metal and the perovskite oxides compete in many applications. For example, in passive component capacitor manufacturing Al/Al<sub>2</sub>O<sub>3</sub> and Ta/Ta<sub>2</sub>O<sub>5</sub> electrolyte capacitors share the market with multilayer ceramic capacitors (MLCC) that are BaTiO<sub>3</sub> based. However, owing to their more complex chemistry, the integration of perovskite layers into devices is difficult when ultra-thin nano-dielectric films are needed.

Therefore, this treatise focuses on the less complex valve metal oxides as ultra-thin nano-dielectrics (<100 nm). Some relevant oxide systems are summarized in Table 1.1. In anticipation of the results presented later, some parameters that are important for electronic applications are also given. For application as a capacitor dielectric material, for example, a high relative dielectric constant  $\epsilon_r$  is important but not sufficient. As indicated in Table 1.1 the anodically formed valve metal oxides differ in structure (some are amorphous, some crystalline), electronic behavior (some oxides behave like an n-type semiconductor), and some oxides show a pronounced texture dependence of oxide growth, that is the oxide properties vary with the crystallographic orientation of the substrate surface. Depending on the desired application of the oxides, an optimum combination of these properties has to be found. As will be discussed in the following chapters, Table 1.1 has to be used carefully, that is, it has to be kept in mind that the given parameters hold for certain 'typical' experimental conditions only. For instance, in the case of Ti/TiO<sub>2</sub> the texture dependence can be reduced by switching from potentiodynamic to potentiostatic oxide formation conditions. Therefore, Table 1.1 only gives a first, rough orientation of the electronic properties and behavior of the oxides. Depending on the experimental formation conditions a wide range of properties can often be obtained. This also explains why literature data often show a huge variation for almost all relevant parameters. Consequently, if data are to be compared, the experimental conditions have to be carefully considered.

### 1.1.1

#### Experimental Approaches

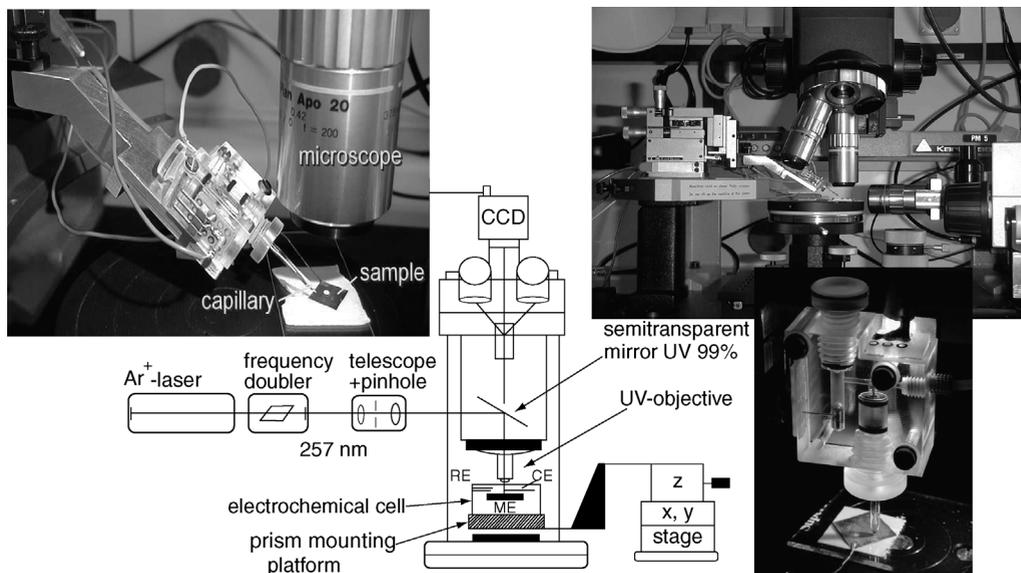
For the study of the oxide systems, electrochemical and optical methods can be applied. Valve metal oxides are formed conventionally electrochemically, with the important exception of SiO<sub>2</sub>, which is usually formed by thermal processing or chemical/physical vapor deposition (CVD/PVD). Conventional electrochemical methods show an excellent vertical resolution for the fundamental study of ultra-thin nano-oxide films on solid surfaces, but their application to micro- and nano-systems, which are of special importance in electronics, is limited because of the poor lateral resolution, with typical electrode areas in the mm<sup>2</sup> to cm<sup>2</sup> range. In order to gain deeper insight into local electrode reactions, microscopic *in situ* methods must be developed and employed that feature both high lateral and vertical resolution. Here an important new approach to address and solve this issue, that is the combination of conventional electrochemistry with optical and new electrochemical micro-methods, is presented. This enables one to characterize or/and modify solid surfaces at high lateral resolution, which is only limited by refraction of light in the μm<sup>2</sup> range. This is especially important for electronic applications as the critical dimensions of relevant structures are extremely small (sub-micron range) and the effect of structural heterogeneities on the film properties is essential for the reliability of the devices. Some fundamental aspects of optical methods employing focused light and their application to electrochemistry are discussed with emphasis on laser light sources. To allow for a high lateral resolution, even by conventional

**Table 1.1** Relative dielectric constant  $\epsilon_r$ , anodic formation factor  $m$ , density  $\rho$ , band gap energy  $E_g$ , cation transfer coefficient  $t_+$ , bias dependence and electronic behavior (SC = semiconductor), structure (a = amorphous, c = crystalline), texture dependence for some of the oxide systems described in this treatise (see also [20]).

System	$\epsilon_r$	$m$ (nmV <sup>-1</sup> )	$\rho$ (g cm <sup>-3</sup> )	$E_g$ (eV)	$t_+$	Bias dep. Electronic behavior	Structure	Texture dep.
Ti/TiO <sub>2</sub>	56 (anodic) [3]	1.4–2.2 [6, 7]	3.9	3.4	0.35 [3]	Yes, n-type SC	a [8]	Yes
Rutile	110 powder 90 ⊥, 170		4.25	3.0				
Anatase	48 (powder)		3.99	3.6				
Brookite	[4, 5]		4.13	3.0				
Zr/ZrO <sub>2</sub>	27 [9]	2.6–3.3	5.7	5	0 [10]	No, dielectric	c [8]	Yes
Ta/Ta <sub>2</sub> O <sub>5</sub>	25 [11, 12]	1.8 [13]	8.5	5.2	0.5 [14]	No, dielectric	a [15, 16]	No
Nb/Nb <sub>2</sub> O <sub>5</sub>	42 [19]	2.9 [20]	4.4	3.4	0.5 [10]	Yes, n-type SC	a [8]	No
Al/Al <sub>2</sub> O <sub>3</sub>	9 [22–24]	1.3 [25]	3.1	7	0.5 [26]	No, dielectric	a [27]	No
Hf/HfO <sub>2</sub>	16 [29]	2.0 [31]	10	5.1	0 [30]	No, dielectric	c [8]	Yes
p-Si/SiO <sub>2</sub>	3.8 [32, 33]	0.7 [38]	2.2	9	0	No, dielectric	a [36]	Yes
BaTiO <sub>3</sub>	≈2000		6			Ferroelectric		
WO <sub>3</sub>	23 [37]	1.8 [38]	6.5	3.1	0.5 [10]		a [8]	

electrochemistry itself, the nl-droplet method first introduced by Kudelka [6] is applied. Depending on the input/output signals, the *micro-methods* used throughout this text can be divided into three different classes:

1. Optical/optical methods (exciting and measured signal = light beam). Examples are the application of well established optical methods, such as ellipsometry, reflection spectroscopy, beam deflection, interferometry, Raman-spectroscopy, etc., along with electrochemistry [40–45]. The incident light beam is focused on a microscopic portion (e.g. a single substrate grain) of a macroscopic electrode and the optical information in the reflected or deflected light beam is analyzed and correlated with the simultaneously recorded electrochemical signals. For instance, micro-ellipsometry can be performed during cyclic voltammetric formation of a passive layer to record film thickness growth on a particular grain of a polycrystalline macroscopic electrode. Examples of this important application will be discussed in full detail later (Section 1.3). In order to allow for an accurate correlation of the signals to the deliberately chosen electrode areas, microscopic control is essential. Figure 1.1 shows a typical experimental setup for this purpose. *SAME* (spectroscopic anisotropy micro-ellipsometry) is introduced as the most important spectroscopic method. This newly developed method allows for the determination of structural properties such as the crystal orientation of the surface film along with conventional parameters, for example, the film thickness. In



**Figure 1.1** Typical experimental setup used for the combined application of micro-optical and electrochemical methods along with *in situ* microscopic sample monitoring. The electrochemical cell is mounted on an x,y,z-stage and can be scanned with sub-micron resolution. Besides the nl-photoresist droplet, the ‘contact cell’ shown can also be used [39].

the case of electroceramics such as YBCO even the chemical composition can be determined by SAME [308].

2. Optical/electrical or optical/chemical methods [measured signals such as electric current (photocurrent  $i_{ph}$ ), voltage, reaction rates, etc.]. A characteristic for this class is that the light beam is used to locally induce a reaction [46–51]. The type of reaction depends on thermal and electronic properties of the solid, the neighboring phase and energy or power density of the light beam. In metals, energy dissipation is very fast. Consequently, most of the energy is transformed into heat resulting in melting or even evaporation of the substrate. In dielectric materials bond breaking with subsequent reactions dominates. In semiconductors dissociation and ionization, reactions are often observed if high power densities are used. However, at low power densities electron/hole pair formation with an associated change of the potential distribution at the interface dominates. Both electron transfer (ETR) in addition to ion transfer (ITR) reactions can be induced. For instance, hole accumulation can cause redox reactions and film growth or removal (corrosion, etching) as will be discussed later. Laser-induced reactions under electrochemical conditions at low power densities, that is at quasi-isothermal conditions will be emphasized.
3. Electrical/electrical microelectrode methods under optical (microscopic) control. This class covers the conventional electrochemical methods, that is, application of an electrical signal (e.g. potential) to the electrode to induce a reaction. The role of optics here is twofold:
  - Samples are prepared by means of photolithography, that is, the local resolution of the electrical measurement is determined by focused laser radiation. In this context it has to be kept in mind that the high lateral resolution achieved in modern device and micro-system technology and research is mainly due to optical processing, that is, photolithography. Detailed examples for application of photoresist microelectrochemistry, namely the new photoresist nl-droplet method, will be given.
  - In order to measure on defined areas the electrode must be microscopically controlled (see Figure 1.1).

## 1.2 Fundamentals and Experimental Details

In this section some fundamentals of the methods used later are summarized. In particular, electrochemistry and photocurrent measurements (optical/electrical) are treated here.

### 1.2.1 Electrochemical Oxide Layer Formation on Valve Metals

Valve metals bear this name due to the fact that they pass current in only one direction (rectifying effect), that is, the anodic current is low for potentials lower than the

formation potential but a strong cathodic evolution of hydrogen is possible. Experimentally the following behavior is found for the anodic oxide formation [52, 295]:

$$i = i_0 e^{(\beta E)} \quad (1.1)$$

where  $i$  is the oxide formation current,  $i_0$  and  $\beta$  are material-dependent constants and  $E$  is the electric field strength in the oxide. This equation is called the *high field equation*. The corresponding high field model assumes an  $E$ -field supported, thermally activated ion movement (hopping) along the distance  $a$ , with  $a$  typically being the lattice parameter. There are many papers on this subject where the above equation is derived assuming specific mechanisms [e.g. 52–61]. Depending on the details in the used models, the rate determining step may be located within the oxide (Verwey, Güntherschulze and Betz), the oxide/electrolyte (Sato) or metal/oxide (Cabrera–Mott) interface. A detailed discussion and derivation of the high field equation can be found in Ref. [20]. An equation of the following form can be derived:

$$i = \nu \rho a \cdot e^{-\frac{W}{RT}} e^{\frac{\alpha z F E}{RT}} \quad (1.2)$$

with  $\nu$  = hopping frequency,  $\alpha$  = transfer coefficient,  $\rho$  = concentration of mobile charge,  $a$  = hopping distance,  $W$  = activation energy for hopping,  $R$  = gas constant,  $T$  = temperature and  $F$  = Faraday's number.

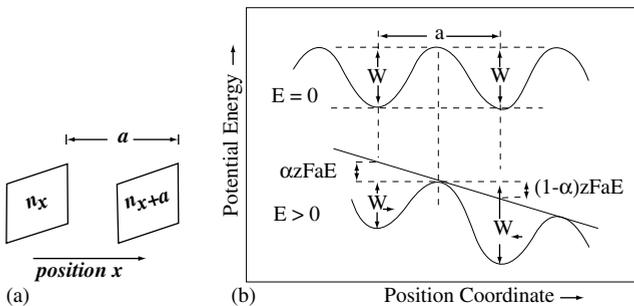
This equation is identical to the experimental Equation 1.1 using the equalities:

$$\beta = \frac{\alpha z F}{RT} \quad \text{and} \quad i_0 = \nu \rho a \cdot e^{-\frac{W}{RT}} \quad (1.3)$$

The parameters occurring in these equations are illustrated in Figure 1.2.

For homogeneous oxide layers the field strength  $E$  can be determined from the potential drop  $\Delta\phi_{\text{ox}}$  across the oxide and the layer thickness  $d_f$ .

$$i = i_0 e^{(\beta E)} = i_0 e^{\left(\beta \frac{\Delta\phi_{\text{ox}}}{d_f}\right)} \quad (1.4)$$



**Figure 1.2** Illustration of the high-field model: (a) adjacent lattice planes in the oxide and (b) effect of the  $E$ -field on the activation energy  $W$  (source Ref. [20]).

For *galvanostatic oxide growth* ( $\log i = \text{const}$ ) the  $E$  field has to be constant resulting immediately in the proportionality:

$$d_f \propto \Delta\varphi_{\text{ox}} \Rightarrow d_f = m \cdot \Delta\varphi_{\text{ox}} \quad (1.5)$$

This equation defines the oxide formation factor:  $m$  ( $\text{nm V}^{-1}$ ), that is, the layer thickness increases linearly with the applied potential.

Equation 1.4 directly implies the time behavior (rate) of oxide growth. An inverse logarithmic growth law according to the following expression can be derived to a good approximation (Cabrera and Mott [55]):

$$\frac{1}{d_f} = A - \frac{1}{\beta \cdot \Delta\varphi_{\text{ox}}} \cdot \ln t \quad (1.6)$$

with  $A$  being a constant.

### 1.2.2

#### The $C(U)$ Curve of a Valve Metal Electrode

The total potential drop  $\Delta\varphi_{\text{tot}}$  across an electrode is made up of four parts: the potential drop at the metal/oxide interface, the potential drop in the oxide, the potential drop in the Helmholtz layer and the potential drop in the electrolyte (diffuse double layer):

$$\Delta\varphi_{\text{tot}} = \Delta\varphi_{\text{Me/ox}} + \Delta\varphi_{\text{ox}} + \Delta\varphi_{\text{H}} + \Delta\varphi_{\text{el}} \quad (1.7)$$

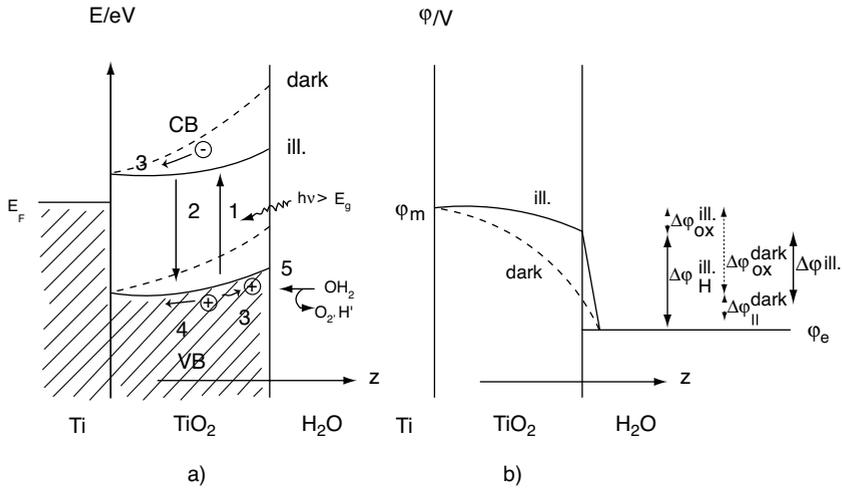
The potential drop  $\Delta\varphi_{\text{tot}}$  correlates with the applied electrode voltage  $\Delta U$  by:  $\Delta\varphi_{\text{tot}} = \Delta U - \text{const}$ . For high electrolyte concentrations ( $>0.1$  M), the last part  $\Delta\varphi_{\text{el}}$  can be neglected. In addition, the first part  $\Delta\varphi_{\text{Me/ox}}$  is normally small. The potential drop in the Helmholtz layer is usually determined by the reaction of adsorption of protons and hydroxyl groups. The corresponding reaction rate is high, that is, equilibrium is reached almost instantaneously. Therefore, the corresponding potential drop is constant resulting in a constant double layer capacitance of about  $20 \mu\text{F cm}^{-2}$ . The potential drop  $\Delta\varphi_{\text{ox}}$  can be calculated using the Poisson equation  $\nabla E = \rho_c / (\epsilon_r \epsilon_0)$  with  $\rho_c$  being the charge density given by the defect state concentration  $N_D$ . This is:

$$\Delta\varphi_{\text{ox}} = \Delta\varphi_{\text{ox, scl}} + \Delta\varphi_{\text{ox, isol}} = -\frac{eN_D d_{\text{scl}}^2}{2\epsilon_r \epsilon_0} + \Delta\varphi_{\text{id, isol}} \quad (1.8)$$

where  $\Delta\varphi_{\text{id,isol}}$  describes the potential drop in the ideal insulator part,  $e$  is the electronic charge,  $d_{\text{scl}}$  is the extension of the space charge layer scl. Inversion of the  $\Delta\varphi_{\text{ox, scl}}$  semiconductor part of this equation yields the following expression for the extension of the space charge layer:

$$d_{\text{scl}} = \sqrt{\frac{2\epsilon_r \epsilon_0 \Delta\varphi_{\text{ox, scl}}}{eN_D}} \quad (1.9)$$

Hence a potential (bias) dependent capacitance  $C_{\text{scl}}$  can be defined with use of the simple capacitor equation  $C_{\text{scl}}/A = \epsilon_r \epsilon_0 / d_{\text{scl}}$ . (As the  $E$  field is completely shielded



**Figure 1.3** (a) Band scheme and (b) potential drops for the dark and illuminated situations. The Ti/TiO<sub>2</sub> system is chosen here for illustration.

inside the scl region, the potential drop  $\Delta\phi_{id,isol}$  vanishes for small applied voltages.) Linearized with respect to the potential drop this yields the so called *Schottky–Mott relationship* [62, 310] (for  $T > 0$ , a  $(K_B T/e)$  part has to be subtracted, which describes the thermal discharging of defect states into the conduction band):

$$\frac{1}{C_{scl}^2} = \frac{2}{\epsilon_r \epsilon_0 e N_D} \cdot \left( \Delta\phi_{ox, scl} - \frac{K_B T}{e} \right) \quad (1.10)$$

This equation holds for the case of small applied voltages when the extension of the scl is smaller than the oxide thickness. Evaluation of the slope of the  $1/C_{scl}^2$  ( $\Delta\phi_{ox,scl}$ ) curve allows for the determination of the product  $\epsilon_r N_D$ . Once the scl reaches completely through the oxide film, the capacitance is determined by  $d_f$ , again yielding the conventional potential independent capacitance  $C/A = \epsilon_r \epsilon_0 / d_f$ . A schematic representation of the relevant potential drops as well as the band structure is shown in Figure 1.3 for the case of the Ti/TiO<sub>2</sub> system. An example of an illuminated surface (induced photocurrent) is also shown here, which is required later.

### 1.2.3

#### Application of Lasers in Electrochemistry

As laser radiation plays an important role in some of the experimental methods employed later, some fundamental aspects of lasers are discussed briefly here. The fact that lasers are more and more replacing conventional light sources in all types of optical applications can be understood by considering their fundamental advantages. Perhaps the most striking feature of laser radiation is its directionality due to a very

low angle of divergence, typically in the order of 1 rad. This has basically two important implications:

1. Laser radiation can be focused down to dimensions of the wavelength of light.
2. A large amount of energy can be concentrated into small spots, yielding high power densities.

In fact, the focusability of laser radiation is the most applied feature. Optimum focusing of laser radiation demands a high mode quality of the laser beam. The best suited mode is the TEM<sub>00</sub>, which shows a Gaussian spatial intensity distribution. This fundamental mode can always be obtained by using intra-cavity apertures, which are small enough to suppress the higher modes. For lasers operated in the TEM<sub>00</sub> mode, the minimum obtainable spot diameter  $s$  (diffraction limit) is given by Airy's formula:

$$s = \lambda \frac{f}{D\pi} \quad (1.11)$$

where  $f$  is the focal length of the focusing system used,  $\lambda$  is the wavelength of the laser and  $D$  is the maximum effective beam diameter (aperture) of the focusing system (beam expanders are an advantage).

However, it is not only the spot size  $s$  that governs the final spatial resolution of the electrode reaction, but illumination of the sample is just the first step in a whole series of induced processes resulting in the final state of the system. For instance, in semiconductor interfaces the lateral hole drift causes an extension of the reaction zone. For the thermally activated processes, the heat conductivity of the sample determines the reaction zone. Therefore, both optical and physical effects determine the final spatial resolution of optical/electrical laser methods.

Other important properties of laser radiation are its narrow spectral bandwidth, coherence and polarization. These features are used in numerous spectroscopic and interferometric applications, such as Raman, polarization, interference spectroscopy, spectroscopic ellipsometry, holography. Moreover, the possibility to create very short light pulses by Q-switching or mode-locking should be mentioned. Pulses below fs-duration are possible and allow for the elucidation of fast transient phenomena such as short spontaneous lifetimes or fast relaxation processes. Laser illumination results in thermal heating, chemical reactions and/or potential changes. In the following experiments laser-induced reactions under electrochemical conditions at low power densities, that is, at quasi-isothermal conditions, are emphasized. Thermal processes are discussed briefly below.

### 1.2.3.1 Thermal Effects

With the assumption of a Gaussian temperature distribution (TEM<sub>00</sub>-mode) on the laser affected zone, the temperature increase  $\Delta T$  can be estimated by the following equation [63]:

$$\Delta T = \frac{A}{2\kappa\sqrt{\pi/2}} \cdot P.r. \arctan \sqrt{\frac{8\kappa t}{\rho c r^2}} \quad (1.12)$$

where  $A$  is absorption,  $\rho$  is density,  $c$  is specific heat,  $\kappa$  is heat conductivity,  $r$  is spot radius =  $s/2$  and  $P$  is power density.

For times  $t \gg \pi r^2 \rho c / [8\kappa]$  ( $t > 10^{-2}$  s) the temperature becomes time independent, a continuous wave (cw) condition. The local temperature is then given by:

$$\Delta T = \frac{APr}{2\kappa} \cdot \sqrt{\frac{\pi}{2}} \quad (1.13)$$

The temperature effect often disturbs precise measurements if isothermal conditions cannot be maintained and if it leads to damage of the sample. Equation 1.12 shows that at constant power density the temperature effect decreases with decreasing pulse times. Therefore, the application of short pulses may be of advantage to avoid damages. If, however, the modification of the surface requires a large amount of total energy, it should be delivered with low power density. On the other hand, there are numerous applications of the thermal heating. It can be used to evaporate or to dissociate the substrate (LAMMA) [64], to enhance reaction rates at the surface or the convection of the electrolyte [65–67]. Finally, it can be employed to study electrode reaction rate constants and the dynamics of the double layer [68].

#### 1.2.4

#### **Electrochemical Photocurrent Measurements (Optical/Electrical Method Class), Introduction of a New Model**

The theoretical formalisms for the interpretation of the pure optical (optical/optical) and the pure electrochemical methods are well established and can be found in numerous publications. It is far beyond the scope of this treatise to review the corresponding models. However, the quantitative interpretation of optical/electrical measurements (photoelectrochemistry) is still incomplete and will be discussed here. For instance, multiple internal reflections within the thin films must be considered, causing  $i_{ph}$  to depend on the layer thickness. This experimental fact has already been described by Schultze *et al.* [69] and later by Di-Quarto and coworkers [70, 71]. However, no quantitative analysis or model were given. The quantitative optical model was independently derived by Smyrl and coworkers [72, 73], Gärtner [75] and Michaelis and Schultze [74]. This optical model has to be combined with the Butler–Gärtner model [75, 76], which itself holds only for crystalline bulk materials. The extended model describes  $i_{ph}$  as a function of the layer thickness  $d_f$ , the optical constants of the substrate and layer, the extension of the space charge layer  $d_{scl}$ , and such electronic properties as the defect state concentration  $N_D$  and the relative dielectric constant  $\epsilon_r$ . However, this model is still not accurate for an exact description of the  $i_{ph}$  behavior of amorphous oxide layers, but another,  $E$ -field depending term, taking the recombination efficiency  $r(E)$  into account, must be coupled to the model. This yields a further dependence of  $i_{ph}$  on the film thickness and on the applied anodic potential. This complete photocurrent model consisting of three different parts, namely the Gärtner-, optics- and  $r(E)$ -parts, was first introduced by Michaelis and Schultze [74] and allows for a complete description of the

experimental results presented later. Consequently, both electronic and optical film properties can principally be determined allowing for a mutual confirmation of the pure optical and electrical methods. We will discuss in which potential and film thickness ranges the different parts of the model dominate and whether a quantitative evaluation of optical and electronic properties is really possible.

#### 1.2.4.1 Photocurrent Model for Ultra-thin, Amorphous Films With $\text{TiO}_2$ as an Example

Illumination of anodically polarized n-type semiconducting oxide films such as  $\text{TiO}_2$  with photon energies above the band gap energy ( $E_g \approx 3.5$  eV for  $\text{TiO}_2$ ) results in electron/hole pair formation. These charges are separated within the space charge layer (scl) causing a photocurrent  $i_{\text{ph}}$ . According to the Butler–Gärtner model, the main contribution to  $i_{\text{ph}}$  can be attributed to electron/hole pairs, which are generated directly within the space charge layer, namely  $i_{\text{scl}}$ . Another contribution is due to charges diffusing into the scl that is,  $i_{\text{ph}} = i_{\text{scl}} + i_{\text{diff}}$ . The generation of  $i_{\text{ph}}$  is in competition with recombination processes throughout the entire layer. These recombination processes are not considered explicitly in the Gärtner approach. The electronic layer parameters enter into the Gärtner model only because of their effect on the extension of the scl ( $d_{\text{scl}}$ ) (see Equation 1.9):

$$d_{\text{scl}} = \sqrt{\frac{2\epsilon_r \epsilon_0 (\Delta\phi_{\text{ox}})}{eN_{\text{D}}}} \quad (1.14)$$

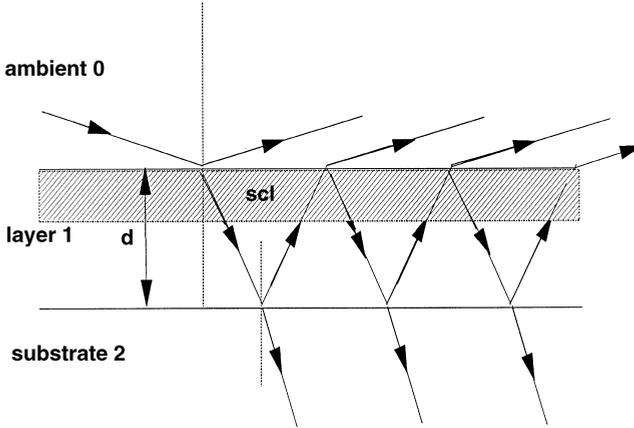
However, the optical film properties describing the absorption of light, that is, the number of photons  $g$  generating the electron/hole pairs have not yet been considered.

This generation number  $g$  is plainly given by the change in the light intensity  $I$  per unit length  $z$ , that is:

$$g(z) = -\frac{d}{dz} I \quad (1.15)$$

In the classical Butler–Gärtner model, light absorption is simply described in terms of Lambert–Beer’s law, containing just one optical constant, the extinction coefficient  $k$ . However, this approach holds for bulk semiconductors only. In the case of ultra-thin semiconducting layers dealt with here, multiple internal reflections must be considered [74–76] if the penetration depth  $\delta$  of the light is larger than the film thickness  $d_f$ . This is illustrated in Figure 1.4. The light energy flux  $I$  into the volume now has to be described by the Poynting vector  $\vec{I}$ . A detailed description of the derivation of this quantity can be found in Ref. [74]. In this case,  $n$  and  $k$  of both the layer and substrate enter into the expression for  $i_{\text{ph}}$  and, even more importantly, the layer thickness  $d_f$  is now considered quantitatively. In principle, this optical model can be coupled to any electronic model. Here, the Butler–Gärtner approach will be kept, yielding

$$i_{\text{ph}} = -e \int_0^{d_{\text{scl}}} \left( \frac{d\vec{I}(z)}{dz} \right) dz \quad (1.16)$$



**Figure 1.4** Multiple internal reflections within ultra-thin semiconducting films (penetration depth of light  $\delta \gg d_f$ ). The extension of the space charge layer scl depends on the applied potential  $U$  and on the electronic layer properties (defect density  $N_D$ , dielectric constant  $\epsilon$ ). It is assumed that only electron/hole pairs generated within the scl contribute to the photocurrent [74].

if only the contribution of electron/hole pairs generated within the scl is considered. It can be shown that the neglect of the diffusion contribution is small [75, 80]. More severe and decisive is the complete neglect of recombination processes in Equation 1.16. Recombination processes are of particular interest for amorphous semiconductors because of the large number of recombination centers. The recombination, that is the efficiency of the electron/hole pair separation, must clearly depend on the  $E$ -field gradient, which itself is a function of the applied potential and the layer thickness. Therefore, a recombination factor  $r(E)$  must be coupled to the above equation. For  $r(E)$  the following approach obeying the boundary conditions of  $r(E) = 0$  for vanishing  $E$ -fields and  $r(E) = 1$  for high fields can be chosen:

$$r(E) = \left( 1 - \frac{1}{\text{const} \cdot E + 1} \right) \quad (1.17)$$

yielding

$$i_{\text{ph}} = -e \left( 1 - \frac{1}{\text{const} \cdot \frac{\Delta\phi_{\text{ox}}}{d_{\text{scl}}} + 1} \right) \cdot \int_0^{d_{\text{scl}}} \left( \frac{d\vec{I}}{dz} \right) dz \quad (1.18)$$

with a linear  $E$ -field approximation. The unknown constant in this equation can be determined by fitting of the experimental  $i_{\text{ph}}(U_{\text{tot}})$  curves. The function used for  $r(E)$  is a good approximation of the expression for the recombination efficiency derived by Pai and Enck [77] for amorphous materials, which has already been discussed in this

**Table 1.2** Contributions of the different parts [ $d_{\text{scl}}$  change, recombination efficiency  $r(E)$ , optics] of the presented photocurrent model to the potential and thickness dependence of the photocurrent [ $i_{\text{ph}}(U)$  and  $i_{\text{ph}}(d)$ ]. The ‘up arrow’, ‘down arrow’ symbols refer to an increase and decrease in the corresponding parameters, respectively.

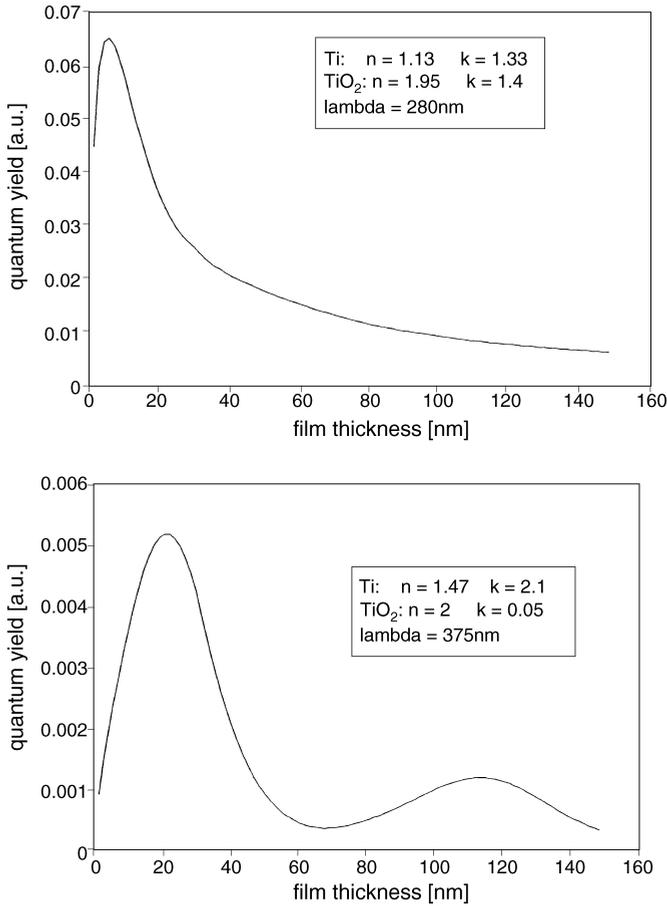
Case	Varied parameter			Effect on $i_{\text{ph}}$ divided into the different parts of the model			
	$d_{\text{lay}}$	$U$	$d_{\text{scl}}$	$r(E)$	Multiple reflections	Lambert–Beer	
1	$d_{\text{scl}} < d_{\text{lay}}$	↑	const	const	const	↑↓	not valid
2	and	const	↑	↑	↑	const	n.v.
3	$d_{\text{lay}} \ll \delta$	↑	↑	↑	↑	↑↓	n.v.
4	$d_{\text{scl}} < d_{\text{lay}}$	↑	const	const	const	n.v.	↓
5	and	const	↑	↑	↑	n.v.	const
6	$d_{\text{lay}} > \delta$	↑	↑	↑	↑	n.v.	↓
7	$d_{\text{scl}} = d_{\text{lay}}$	↑	const	↑	↓	↑↓	n.v.
8	and	const	↑	const	↑	const	n.v.
9	$d_{\text{lay}} \ll \delta$	↑	↑	↑		↑↓	n.v.
10	$d_{\text{scl}} = d_{\text{lay}}$	↑	const	↑	↓	n.v.	↓
11	and	const	↑	const	↑	n.v.	const
12	$d_{\text{lay}} > \delta$	↑	↑	↑		n.v.	↓

context in Refs. [71, 76]. The comparison of both equations shows that the constant has to be a function of the thermalization length, which itself depends on the mobility of the charge carriers and the photon energy of the exciting light.

In Table 1.2 the contributions of the three different parts of the model to the experimental output signals are summarized for various cases. The three parts are:

- The classical Gärtner part describing the effect of the extension of the space charge layer  $d_{\text{scl}}$ , which itself depends on the electronic properties  $\epsilon_r$  and  $N_D$ .
- The exact optical model describing multiple internal reflections, which are important for thin films where the penetration depth of the light  $\delta$  is larger than the layer thickness. Because of this part,  $i_{\text{ph}}$  depends on the layer thickness and the optical constants of both substrate and layer. This optical part mainly explains the observed variation in  $i_{\text{ph}}(d_f)$  found in the photocurrent spectra.
- The third part describes the electron/hole pair recombination efficiency  $r(E)$  which causes a further dependence of  $i_{\text{ph}}$  on the layer thickness for very thin films, high potentials, respectively ( $d_{\text{scl}} = d_f$ ), and superimposes on the thickness dependence due to the optical part.

The ‘up arrow’, ‘down arrow’ symbols in the table denote an increase or decrease in the applied potential  $U_{\text{tot}}$  and  $d_f$  or  $i_{\text{ph}}$ , respectively. For example, the  $i_{\text{ph}}$  thickness



**Figure 1.5** Simulations according to the photocurrent model for two different wavelengths. The optical constants used are given in the insets. It was assumed that the  $E$ -field gradient reaches through the entire film (dielectric behavior), applied potential 2 V.

dependence in cases 1 and 4 ( $d_{\text{scl}} < d_f$ ) is given solely by the effect of multiple internal reflections or the Lambert–Beer law, depending on whether the penetration depth  $\delta$  of the light is larger or smaller than  $d_f$ . Therefore, these cases can be used to judge the optical model and to determine the optical parameters. In the case of the ultra-thin films only  $d_f \ll \delta$  applies. The experiments for the valve metal oxides presented later can be understood by referring to particular cases of this table.

Figure 1.5 shows  $i_{\text{ph}}(d_f)$  simulations according to the model for two different wavelengths (280 and 375 nm) under potentiostatic conditions (applied potential 2 V). The optical constants used for these calculations were determined by ellipsometry (isotropic approximation) and are given in the insets of the figures. Owing to the strong light absorption at 280 nm ( $k = 1.4$ ) no interference is observed at this wavelength. The decrease in the photocurrent at high film thicknesses is due to the

dominating  $E$ -field effect  $r(E)$  corresponding to cases 7 and 10 of Table 1.2. For this, an insulating  $\text{TiO}_2$  film behavior was assumed, that is, the  $E$ -field gradient reaches through the entire film ( $d_{\text{scl}} = d_f$ ). At 375 nm (3.3 eV) case 7 clearly dominates ( $\delta \ll d_f$ ), that is, the interference effect is obvious. Note that in this case the photon energy is below the direct bandgap energy of  $\text{TiO}_2$ . In this spectral range the photocurrent is caused by indirect or intraband excitations. As this intraband mechanism differs from the direct interband one, the electronic part of the model is not fully applicable and slight deviations between measurement and simulation have to be expected (see the experiments below).

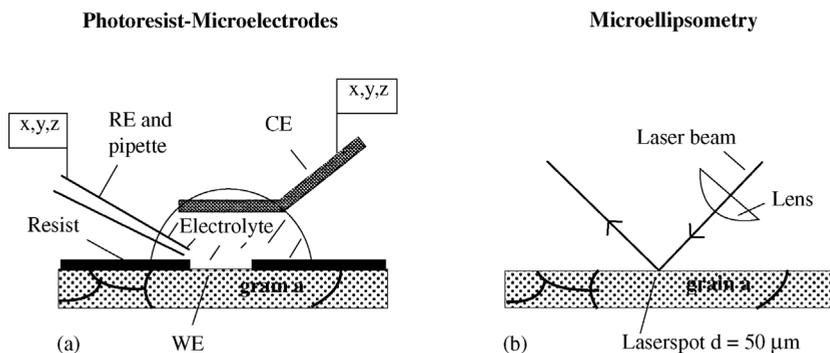
### 1.3 Valve Metal Systems

#### 1.3.1 Ti/TiO<sub>2</sub> System

As a first example for the combined application of the aforementioned methods for characterization and modification of local areas on technically relevant polycrystalline materials, the Ti/TiO<sub>2</sub> system is used. All subsequent experiments were performed under microscopic control on well-defined and deliberately chosen single substrate grains. For this the photoresist microelectrode method was applied, which allows all types of electrochemical measurements at high lateral resolution to be performed in a droplet of nl-volume (Kudelka [78]). As the optical/optical method, micro-ellipsometry, in particular SAME, will be emphasized as it allows for a complete determination of both the optical parameters of the system and the film thickness  $d_f$  [81–83]. SAME uses a generalized ellipsometry approach and allows for the determination of crystallographic properties such as the orientation of substrate grains, which than can be correlated with the film properties [308]. This allows for quantification of the effect of the substrate/film interface on film properties. For instance, recrystallization of semiconducting films or epitaxial film growth can be studied. The electronic film parameters are correlated with the substrate texture yielding an insight into the growth mechanisms of this system. Figure 1.6 illustrates the combined application of ellipsometry and the nl-photoresist microelectrode method on technically relevant polycrystalline electrode materials. Additionally, photocurrent spectroscopy and UV-laser scanning measurements are presented to give an example for the aforementioned optical/electrical methods.

##### 1.3.1.1 Experimental Details

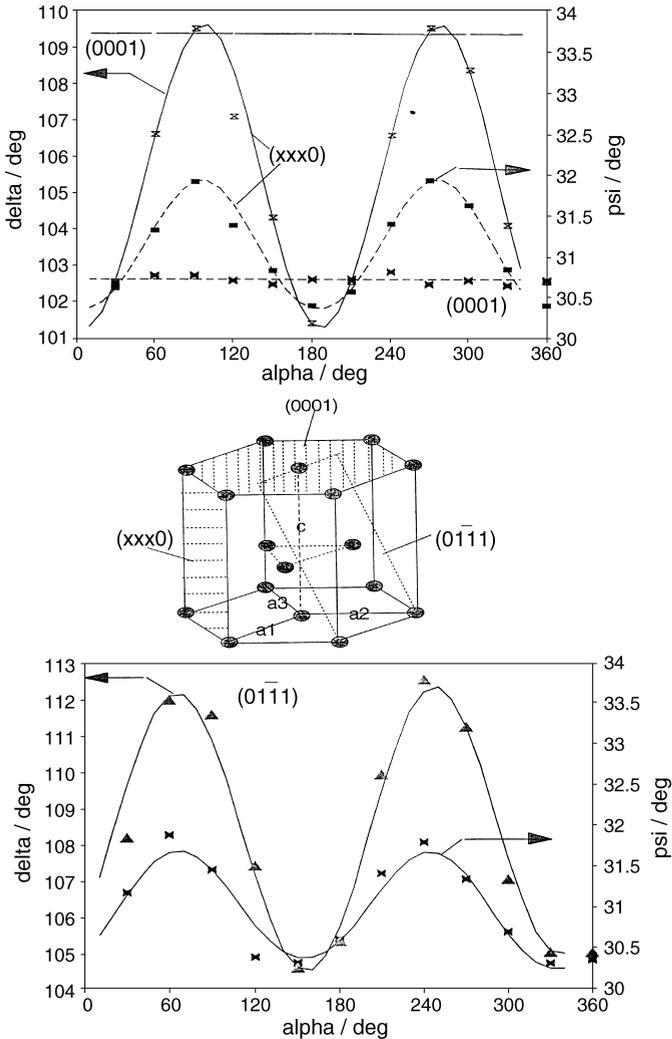
Owing to its pronounced heterogeneity, the Ti/TiO<sub>2</sub> system is particularly suitable for demonstrating the advantages of micro-methods. The heterogeneity of the Ti/TiO<sub>2</sub> system can immediately be observed visually, by looking at a Ti/TiO<sub>2</sub> surface with open grain boundaries through a microscope. The TiO<sub>2</sub> passive film properties significantly depend on the substrate texture resulting in a variation of the TiO<sub>2</sub> interference colors from grain to grain. The objective of the presented experiments is



**Figure 1.6** Electrochemical and optical micro-methods under microscopic control: (a) photoresist nl-droplet method according to Kudelka and (b) optical micro-methods can be applied on the same portion of the heterogeneous sample. Measurements on a single grain of technically relevant polycrystalline samples can be performed.

the quantification of this phenomenon. For all experiments Ti high-purity (99.98%) samples with a coarse grain texture were used (grain diameter  $>600 \mu\text{m}$ ). This allows several independent experiments to be performed on each single grain. The crystallographic orientation of the substrate grains was determined *in situ* by SAME. In order to prepare samples with open grain boundaries, the surfaces were electro-polished. As the electrolyte  $0.5 \text{ M H}_2\text{SO}_4$  was chosen. Potentials are given with respect to the standard hydrogen electrode (SHE) throughout this treatise.

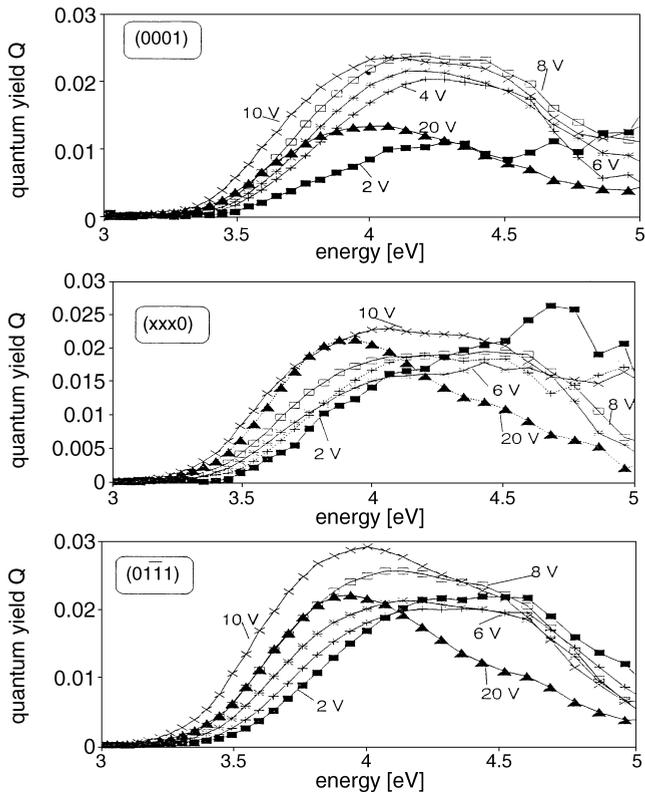
For ellipsometry, a rotating analyzer configuration with an HeNe laser ( $632.8 \text{ nm}$ ) as the light source was employed. SAME requires rotation of the sample around the surface normal (denoted by an angle  $\alpha$ ). In order to allow for this sample rotation, a particular *in situ* cell was constructed. For this, the cell windows were mounted on the ellipsometer arms using an alignable connector and simply dipped into the electrolyte. Therefore, rotation of the entire cell containing the sample in three-electrode configuration is possible without affecting the window alignment [81, 84]. For the optical/electrical (photoelectrochemical) experiments at high lateral resolution, the setup shown in Figure 1.1 was used (UV laser scanning setup) [79, 80]. The light of a frequency doubled  $\text{Ar}^+$ -laser ( $\lambda = 257 \text{ nm}$ , i.e.  $4.8 \text{ eV}$ ) is focused onto the sample surface by means of the same microscope that is used to control the optical/optical and electrical/electrical methods, that is the measurements can be carried out simultaneously. A minimum spot radius of about  $1 \mu\text{m}$  was achieved yielding power densities up to some  $\text{kW cm}^{-2}$ . The sample/cell configuration can be scanned normal to the light beam by using a computerized  $x,y$ -stage (step size =  $1 \mu\text{m}$ ). For the detection of photocurrent spectra, the laser is substituted by a standard  $1 \text{ kW Xe}$  high pressure arc lamp and a monochromator. In this instance the lateral resolution is about  $50 \mu\text{m}$ . The whole set-up is based on a modular concept, that is all measurements can be performed simultaneously under microscopic control and further tools such as reflection-spectroscopy or video-microscopy can be added. Details of the nl-droplet photoresist method (electrical/electrical) are given below.



**Figure 1.7** SAME on three different Ti grains with (0001), (0111) and (xxx0) orientation. The crystallographic orientations are illustrated in the displayed Ti lattice.

### 1.3.1.2 Determination of Ti Substrate Grain Orientation by SAME

In order to determine the crystallographic orientation of single Ti grains, SAME was applied. SAME yields the angle  $\varphi$  between the surface normal and the optical axis ( $c$ -axis). For this, the ellipsometric measurables  $\Delta$  and  $\Psi$  are measured as a function of the angle  $\alpha$ , which describes rotation of the sample about the surface normal. The corresponding experimental curves are shown in Figure 1.7 for the example of two different Ti grains. The grains are covered by anodically formed 4 V  $\text{TiO}_2$  layers, which themselves are amorphous and therefore do not contribute to the  $\Delta(\alpha)$  and



**Figure 1.8** Photocurrent spectra (quantum yield  $Q$ ) of  $\text{TiO}_2$  passive films for different film thicknesses (formation potential, respectively). The measurements were carried out on three differently oriented Ti single grains. Electrolyte 0.5 M  $\text{H}_2\text{SO}_4$ , anodic potential 2 V.

$\Psi(\alpha)$  variation. The quantitative analysis of these curves allows the determination of the crystallographic orientation [82, 83, 308]. The planes determined from the curves of Figure 1.7 are illustrated in the Ti crystal structure shown. The (0001) surface ( $\varphi = 0^\circ$ ) is the closest packed surface with  $1.15 \text{ \AA}^{-2}$  (lattice parameters:  $a = 0.2951 \text{ nm}$ ,  $c = 0.4679 \text{ nm}$ ), (xxx0) refers to any plane perpendicular to the  $c$ -axis ( $\varphi = 90^\circ$ ).

### 1.3.1.3 Photocurrent Spectra and $i_{\text{ph}}(U)$ Measurements on Single Ti/ $\text{TiO}_2$ Grains

Micro-photocurrent spectra, (quantum yield  $Q$ ) taken on different oriented single Ti grains in 0.5 M  $\text{H}_2\text{SO}_4$  are shown in Figure 1.8. The  $\text{TiO}_2$  films were formed potentiodynamically in the same solution at the indicated formation potentials (2 V up to 20 V) before the spectra were recorded at a constant anodic potential of 1 V. Consequently, the data show the dependence of the photocurrent spectra on both the  $\text{TiO}_2$  film thickness and the grain orientation. The formation factor was measured for each of the different orientations by ellipsometry (value averaged over all orientations:  $2 \text{ nm V}^{-1}$ ). This allows for a quantitative correlation of the spectra with the

film thickness. Evaluation of the  $Q^2$  and  $Q^{0.5}$  curves allows for the determination of the direct and indirect bandgap energies.  $E_{\text{dir}}$  varies between 3.7 and 3.4 eV for the different orientations and shows a slight decrease with increasing film thickness. The same holds for  $E_{\text{indir}}$ , which varies between 3.3 and 3 eV. For energies below the bandgap, an Urbach tail was found with a slope of 120 meV for the disorder energy. This indicates the amorphizity of the  $\text{TiO}_2$  passive films, that is, there is no sharp bandgap but a mobility gap. The mobility gap energy is close to the bandgap energies of the  $\text{TiO}_2$  modification anatase, therefore indicating a relationship between this modification and the amorphous  $\text{TiO}_2$  layers found here (near order). The variation of  $i_{\text{ph}}$  with the Ti grain orientation confirms that in spite of the amorphicity of the  $\text{TiO}_2$  films, their properties depend sensitively on the substrate texture. It has to be emphasized that the dependence of  $i_{\text{ph}}$  on  $d_f$  caused by internal reflections and the recombination processes mentioned in the above photocurrent model is evident across the entire spectral range: up to 10 V  $i_{\text{ph}}$  increases, thereafter  $i_{\text{ph}}$  decreases. This interference pattern is in excellent agreement with the simulation curves shown in Figure 1.5, therefore confirming this model. In order to allow for a more quantitative check of the model, the photocurrent was measured as a function of the formation potential, film thickness, respectively. Four experimental curves covering the spectral range from 280 up to 375 nm are shown in Figure 1.9 for an 0001 oriented grain. During illumination, an anodic potential of 2 V was applied. For the wavelength of  $\lambda = 280$  nm, clearly case 10 from Table 1.2 applies, that is, the  $r(E)$  term dominates over the entire thickness range. As the penetration depth of the light increases with increasing wavelength, the interference effect becomes more and more prominent at longer wavelengths, confirming the contribution of the internal reflections to  $i_{\text{ph}}$ . The simulations shown in Figure 1.9 agree well with the experimental curves. The minor deviations between model and experiment can be attributed to the different mechanisms for direct and sub-band excitations.

#### 1.3.1.4 Microscopic Modification of the $\text{TiO}_2$ Films by Means of Laser Scanning

The migration of holes to the oxide/electrolyte interface leads to an accumulation of positive charge at the surface, which causes a change to the potential distribution within the oxide, namely the photopotential. Under potentiostatic conditions, the potential drop in the Helmholtz layer will be increased accordingly, enhancing the charge transfer of oxygen through the oxide/electrolyte interface. This affects the film formation which itself is a simple anodic ion transfer reaction without direct contribution of holes as:

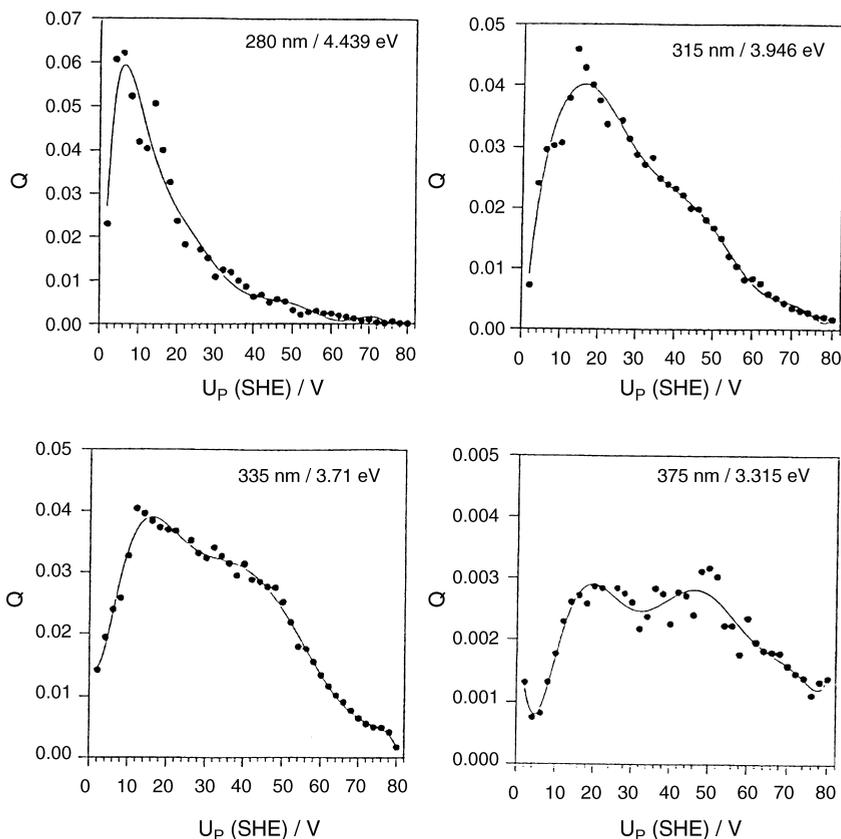


On the other hand, the holes are directly involved in two reactions, oxygen formation and photo-corrosion, as:



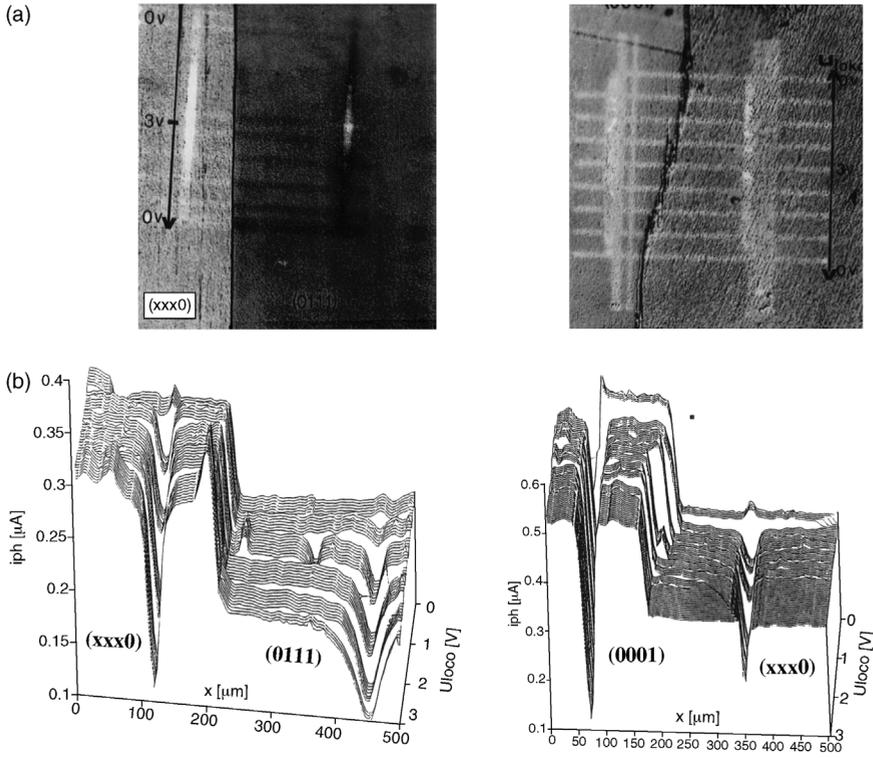
and





**Figure 1.9** Photocurrent (quantum yield  $Q$ ) as a function of the  $\text{TiO}_2$  formation potential  $U_P$ , film thickness, respectively. During illumination a potential of 2 V was applied to the electrode.

As will be shown below, at high anodic potentials reaction 19 dominates allowing for a light induced modification of the surfaces, that is, laser induced film growth. This effect was first discovered by Leitner and Schultze [49]. An example from Michaelis [7] is demonstrated in Figure 1.10, where the results of so-called locodynamic experiments across grain boundaries between single Ti grains of known orientation are shown. For this, the illuminated samples were scanned in  $\mu\text{m}$ -steps normal to the laser beam while the electrode potential was increased, as in a conventional cyclic voltammogram. The advantage of this procedure is that the laser beam always hits an almost fresh surface area, allowing the potential dependence of the photo-reactions to be investigated without previous modification of the initial semiconducting films. Figure 1.10a shows micrographs of the resulting modified Ti surfaces on four substrate grains. The surface orientations and the grain boundaries between the single grains are indicated. The locodynamic experiments were performed on anodic  $\text{TiO}_2$  films formed potentiodynamically at 20 V. The UV-laser power was  $50 \text{ kW cm}^{-2}$ , the applied potential  $U_{\text{loco}}$  during illumination was cycled



**Figure 1.10** (a) Micrographs of the (0001)/(xxx0) and (0111)/(0001) grains (anodic 20V TiO<sub>2</sub> films). The applied electrode potential  $U_{loco}$  was cycled between 0 and 3 V, laser power = 50 kW cm<sup>-2</sup>. The visible laser traces indicate formation of a gradient in the TiO<sub>2</sub> film thickness. (b) Laser scanning analysis across the laser traces and the grain boundaries (imaging of the film properties).

between 0 and 3 V. The lateral dimensions of the laser modified line (parallel to the grain boundaries) significantly exceed the illuminated area (spot radius 2 μm), indicating lateral transport mechanisms such as hole diffusion beyond the laser focus. The color of the laser traces varies with the applied anodic potential  $U_{loco}$  indicating formation of a gradient in the film thickness.

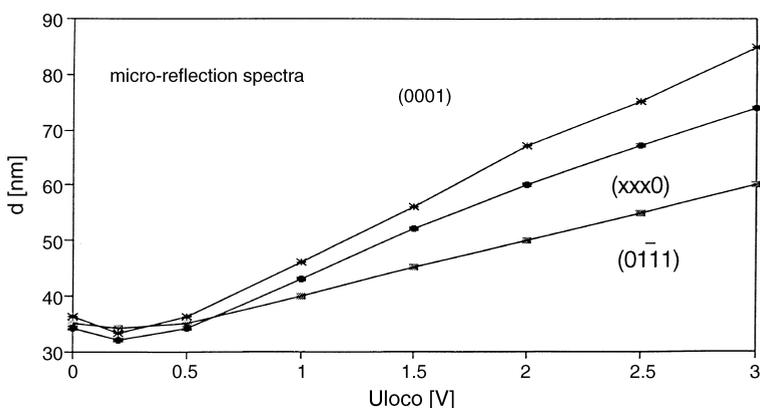
### 1.3.1.5 Characterization of the Modified TiO<sub>2</sub> Films

**1.3.1.5.1 UV-Laser Scanning Analysis** For a quantitative analysis of the laser-modified films, laser-scanning experiments normal to the laser traces and across the grain boundaries were carried out using reduced laser power below the threshold of modification (50 μW). The results [ $i_{ph}(x,y)$ ] are shown in Figure 1.10b. The scale of the  $x$ -axis holds for both the micrograph and the corresponding  $i_{ph}(x)$ -curve. These curves give a sectional profile of the laser-modified site corresponding to the potential

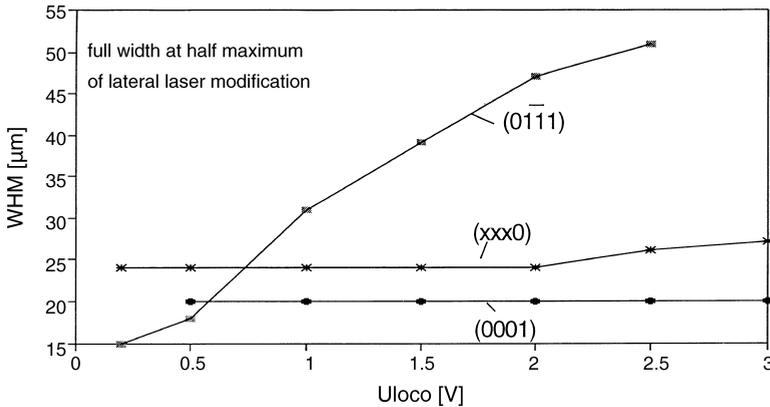
$U_{\text{loco}}$  applied in the locodynamic experiment previously. From the  $x$ -scan the lateral dimensions of the laser-induced modification can be evaluated. Scanning of the surface  $i_{\text{ph}} = f(x, y)$  in both dimensions allows for an imaging of the entire potential dependence  $i_{\text{ph}} = f(x, y = U_{\text{loco}})$  of the laser induced modification. The photocurrent fluctuations on the unmodified crystal surfaces are below 1%. Crossing from one crystal surface to the other (scanning across the grain boundary) yields an immediate  $i_{\text{ph}}$  change of about a factor of 2 due to the dependence of  $i_{\text{ph}}$  on the texture, as discussed previously. From the decay of this sudden change, the lateral resolution of the method can be estimated to be about  $2 \mu\text{m}$ , which agrees well with the laser focus. Hence, it can be concluded that laser scanning allows imaging of passive layer properties at heterogeneities such as grain boundaries. For instance, as in Figure 1.10a, the fringed structure of the grain boundary between the (0001)/(xxx0) surfaces, visible in the micrograph can be imaged accurately.

**1.3.1.5.2 Micro-Reflection Spectroscopy** Figure 1.11 shows the film thickness measured on top of the modified region by means of micro-reflection spectroscopy. For the evaluation of the film thickness, averaged optical constants were used, which were determined by ellipsometry. At locodynamic potentials exceeding 0.25 V an increase of the film thickness is observed, proving reaction 19 to be dominant in this potential regime. However, below 0.25 V a thinning of the  $\text{TiO}_2$  film took place, which can be attributed to photocorrosion, i.e. reaction 21. This leads to the important conclusion that UV-laser illumination can be used for both a thickening (writing) or thinning (erasing) of semiconducting films. The applied potential ( $U_{\text{loco}}$ ) determines which reaction dominates and therefore can be used to control the layer thickness. One important application of this method is the generation of semiconducting films with thickness gradients. Such gradients can be realized by means of locodynamic illumination of the sample surface.

Additionally,  $d_f$  and the lateral extension of the laser modified films depend on the substrate orientation, which therefore must be known. To do this, SAME can be



**Figure 1.11** Micro-reflection spectroscopically determined film thickness of the UV-laser generated  $\text{TiO}_2$  gradients as a function of the applied electrode potential  $U_{\text{loco}}$ .



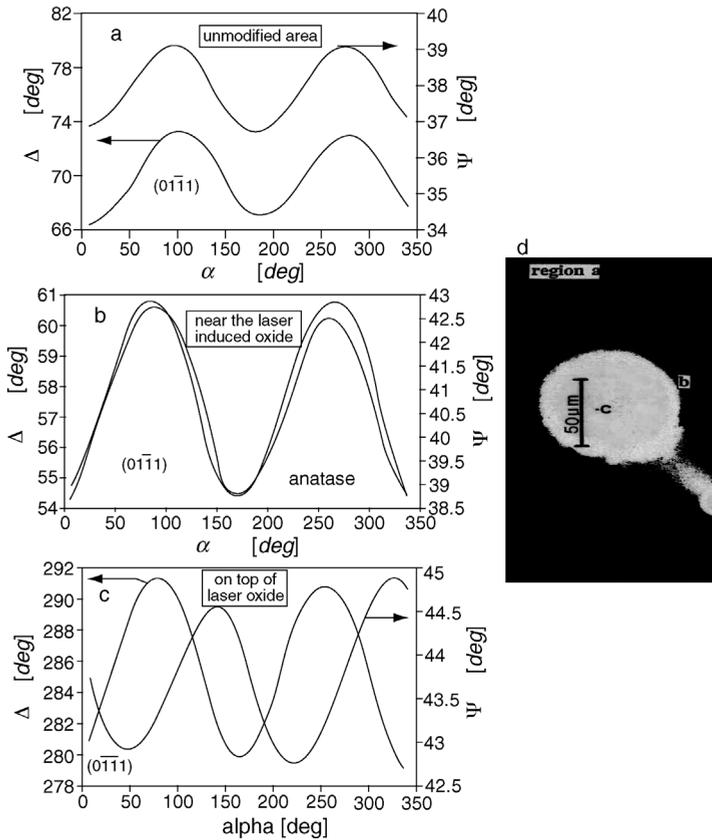
**Figure 1.12** Lateral extension (full width at half maximum) of the TiO<sub>2</sub> gradients as a function of the applied electrode potential  $U_{loco}$ . The focus spot diameter during illumination was 2  $\mu\text{m}$ .

applied *in situ*. For all substrate orientations it was found that the lateral extension of the modified regions exceeds the illuminated site significantly. In the case of the (0001) and (xxx0) orientation, the lateral extension of the modified site is almost independent of  $U_{loco}$ . In contrast, the (0111) surface shows a significant dependence of the laser line extension on  $U_{loco}$ . This is quantified in Figure 1.12, showing the full width at half maximum of the laser scans shown in Figure 1.10b as a function of  $U_{loco}$ . These curves correlate well with the reflection spectra results shown in Figure 1.11, that is the laser induced oxides are vertically thicker but less extended for the (0001) and (xxx0) than for the (0111) orientation. This suggests that the amount of the laser-induced oxide is determined by the number of electron/hole pairs generated and is almost constant for the different orientations. The difference in the lateral and vertical extension of the laser-modified region for the different grains is due to the different electronic properties of the original semiconducting films determining the lateral hole diffusion.

**1.3.1.5.3 SAME Analysis of the Modified Films** In order to analyze the structure of the UV laser modified anodic TiO<sub>2</sub> films (formation potential: 20 V), SAME was carried out ( $U_{loco} = 2$  V). Figure 1.13 shows the resulting SAME-curves  $\Delta(\alpha)$  and  $\Psi(\alpha)$  for the (0111) grain as an example. Three SAME experiments at different sites of the sample were performed, that is:

1. at large a distance from the laser modified region (characterization of unmodified passive film)
2. close to the illuminated area (effect of lateral hole diffusion on passive film)
3. on top of the illuminated area.

At a large distance from the laser illumination, the typical SAME curve for an amorphous TiO<sub>2</sub> with 35 nm thickness was measured. The film properties completely correspond to the films measured previously in Figure 1.7. More interesting were the SAME results from experiment 2. The corresponding curves show a significant



**Figure 1.13** SAME curves recorded on potentiodynamically formed 20 V  $\text{TiO}_2$  films on a (0111) oriented Ti substrate grain. (a) A large distance from a laser modified spot; (b) close to the modified region; (c) on top of the laser modified area; (d) photograph of laser modified surface.

change in amplitude, phase and average value in comparison with the SAME curve of experiment 1. The optical parameters of crystalline anatase were then derived, suggesting a recrystallization of the  $\text{TiO}_2$  films. However, this phenomenon did not occur on the other two grain orientations. Lateral hole diffusion is most prominent on the (0111) orientation. This agrees with the laser scanning measurements of Figure 1.10 where the largest extension of the laser traces appears on the (0111) surface.

Experiment 3 again shows a clear change in amplitude, phase and average value of the  $\Delta(\alpha)$  and  $\Psi(\alpha)$  curves. The increase in the  $\Delta(\alpha)$  and  $\Psi(\alpha)$  average values can be attributed to an increased film thickness (reaction 19, i.e. film growth). The alteration of both phase and amplitude again indicates a structure change of the  $\text{TiO}_2$  films. Quantitative SAME evaluation reveals that a two-layer model now has to be applied. It was found that the initial films (metal/oxide interface) recrystallized into anatase

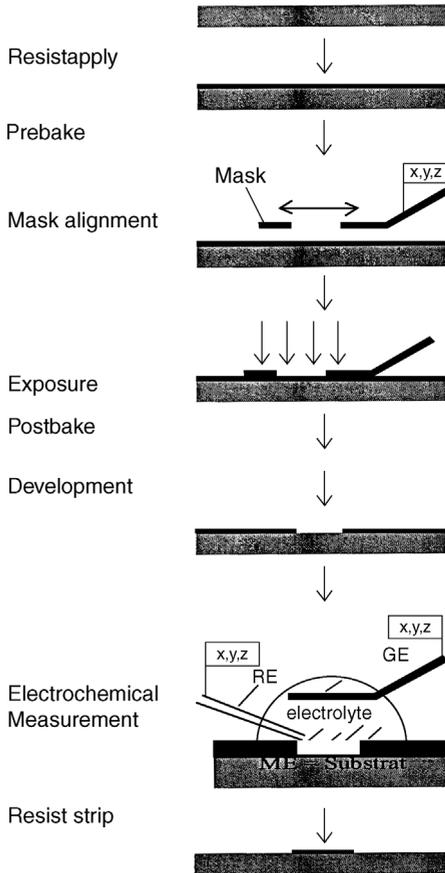
analogues in experiment 2 (optical parameters  $n_{\text{ao}} = 2.48$ ,  $n_{\text{o}} = 2.55$ , ordinary and extraordinary refractive index, respectively). On top of this crystallized film an amorphous layer was found exhibiting a low density of about  $3 \text{ g cm}^{-3}$  (estimated by analysis of the determined optical constants [85, 86]). Therefore, these oxides can clearly be distinguished from each other and from the original anodic films. These experiments illustrate well that even on homogeneous electrode areas, in this case one single (0111)-oriented grain, optical micro-methods can be applied to characterize and elucidate local electrode reactions.

#### 1.3.1.6 Photoresist Microelectrochemistry (Nanoliter Droplet Method)

As described in the preceding sections, the application of focused laser light is a powerful instrument for the detection of local thin film properties such as morphology, thickness and photocurrent. In order to complement this information in terms of electrochemical reactivity, such as electron and ion transfer rates, capacitance and potential, a flexible photolithographic technique in combination with electrochemical measurements in small droplets under optical control has been applied to scale down classical electrochemical experiments [6]. In comparison with the well established scanning electrochemical microscope (SECM) [87], the technique employed here uses a patterned fixed ultra-microelectrode with a well defined surface area and a three-electrode configuration. Hence, the local resolution is limited by the lithographic resolution in the sub-micrometer range and by the electronic detection limit of the current amplifier.

**1.3.1.6.1 Preparation and Measurement Technique** In order to allow the preparation of the photoresist microelectrode at the point of interest, the preparation as well as the measurement was carried out under microscopic control as described in the flow chart in Figure 1.14. Following the resist-coating (positive tone,  $d_{\text{resist}} 1 \mu\text{m}$ ) and prebake, the microelectrode is exposed under proximity conditions at the desired spot of the sample. A preconditioning of a highly reflective metal surface with HMDS (hexamethyldisilane) and an antireflective coating was avoided due to the possible impact on the electrochemical reactivity of the surface, though limiting the performance of the lithography. Pinhole masks are positioned by an  $x,y,z$ -stage and exposed by UV light, which is fed through the microscope. The distance between two adjacent microelectrodes can be as low as  $50 \mu\text{m}$ . A postbake and the development completes the preparation.

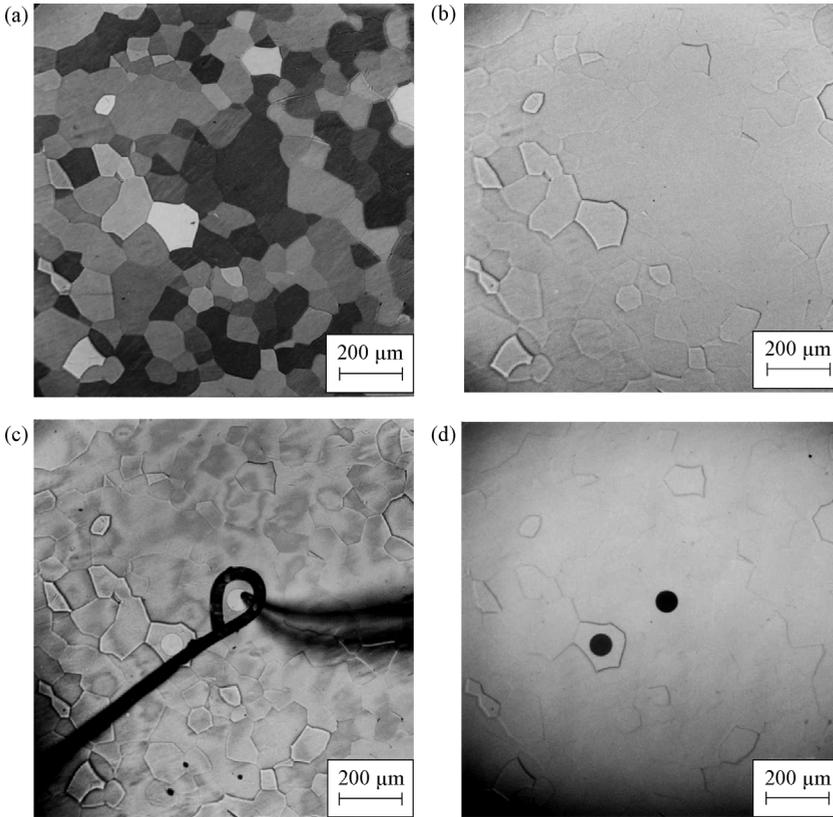
A schematic drawing and the microscopic view of the experimental setup are shown in Figures 1.14 and 1.15. A glass capillary is filled with electrolyte and is connected to the reference electrode (e.g.  $\text{Hg}/\text{Hg}_2\text{SO}_4$ ,  $U_0 = +0.68 \text{ V}$ ) and an electrolyte reservoir with a nanopipette, so that nanoliter droplets can be dispensed on the photoresist microelectrode. The diameter of the droplet is usually set to twice the diameter of the microelectrode. Micromanipulators are used to position the electrodes. A platinum wire is dipped into the droplet as a counter electrode, completing the experimental setup. Microelectrodes with a diameter of  $5 \mu\text{m}$  can be realized using proximity exposure with reproducible surface areas. Figure 1.15 shows an example of a microelectrode preparation on single grains of a polycrystalline Ti sample as viewed



**Figure 1.14** Process steps for the preparation and electrochemical measurement of photoresist microelectrodes. All steps are carried out under microscopic control with micro-manipulators to handle the mask and the microelectrodes: GE, counter electrode; RE, reference electrode; ME = working electrode. (Method introduced by Kudelka and Schultze 1993 [6].)

with the microscope. Individual grains are identified on the electropolished surface when the resist is applied. The localization of the electrode reaction is demonstrated by the different colors of the anodic oxide layers. Each electrode can be addressed separately. A more detailed description, including the effects of the photoresist preparation on the electrochemical measurements, is given in Ref. [88].

**1.3.1.6.2 General Aspects** It is beyond the scope of this treatment to discuss the current and potential distribution for photoresist microelectrodes in detail. Therefore, only a few comments will be made on the influence of the geometry and the resist barrier on electrochemical measurements. Photoresist microelectrodes can be treated as a recessed microdisk electrode. The diffusion field and the current distribution are



**Figure 1.15** Microscopic view of sample preparation and measurement as expressed in Figure 1.14. The same area of a polycrystalline Ti sample is shown after different treatments: (a) with 20 V anodic oxide layer formed in 0.5 M  $\text{H}_2\text{SO}_4$  potentiodynamically with  $60 \text{ mV s}^{-1}$ ; (b) after electropolishing; (c) during the electrochemical measurement on a  $100 \mu\text{m}$  photoresist microelectrode; and (d) after growing anodic oxide layers and stripping of the photoresist.

not hemispherical, as the aspect ratio increases. Model calculations [87, 88] have shown that for a microelectrode with an aspect ratio of 0.1 (diameter of the electrode  $d_{\mu} = 10 \mu\text{m}$ ,  $d_{\text{resist}} = 1 \mu\text{m}$ ) the resistivity increases by 15% in comparison with a planar microdisk electrode. For an aspect ratio of 1 the value increases to 50%. These limitations are negligible unless very high current densities in the order of  $\text{A cm}^{-2}$  occur. For potential step measurements, high currents occur due to the capacitance charging of the double layer, microelectrodes with  $d_{\mu} = 50 \mu\text{m}$  have been used in this study. Here, the assumptions of planar microelectrodes are still applicable. The time constant for charging a capacitance of  $C_{\text{H}} = 20 \mu\text{F cm}^{-2}$  in 0.5 M  $\text{H}_2\text{SO}_4$  ( $3.7 \Omega\text{cm}$ ) at a  $50 \mu\text{m}$  microelectrode is less than  $1 \mu\text{s}$ , thus allowing kinetic studies in the ms range, as will be demonstrated in the next section. In addition, the distance between the microelectrode and the reference and counter electrode was adjusted to some  $\mu\text{m}$ , which helps to control the potential of the electrode.

Owing to the finite electrolyte volume of the nanoliter droplet, the diffusion boundary layer reaches the dimensions of the droplet within seconds, assuming a diffusion coefficient of for example  $D = 1 \cdot 10^{-5} \text{ cm}^2 \text{ s}^{-1}$ . A constant diffusion gradient can not be established because the bulk concentration is reduced. Thus, measurements of diffusion limited currents are not stable over time. The electron transfer reactions discussed below were carried out on anodic oxide layers with maximum current densities 3 to 4 orders of magnitude lower than the diffusion limited current densities, thus ensuring a stable support of consumables over the time of the measurement. In order to prevent evaporation of electrolyte, the ambient was saturated with water vapor.

The use of a small electrolyte covered resist area around the microelectrode is essential when capacitance measurements are performed, as the resist capacitance is parallel to the electrode capacitance. With a specific resistance of  $\sigma = 10^{12} \Omega \text{ cm}$  and a dielectric constant of  $\epsilon = 1.5$  for the resist, and assuming a typical electrode capacitance of  $10 \mu\text{F cm}^{-2}$  with a  $50 \mu\text{m}$  electrode, an error of 5% is obtained, if the electrolyte covered surface is  $10^{-3} \text{ cm}^2$  ( $f = 1000 \text{ Hz}$ ) [88]. Thus, for capacitance measurements, the use of nanoliter droplets is essential.

### 1.3.1.7 Applications of Photoresist Microelectrodes

In the following sections the electrochemical reactivity of single grains of polycrystalline Ti is explored by using the nl-droplet method. The results from electrochemical measurements and the optical laser techniques from the previous section are combined to yield a band structure model for anodically grown anodic oxide layers. Other applications of this method to study laser induced corrosion, texture dependent photocurrent and corrosion of anodic oxide films are described in Refs. [89, 90 and 91].

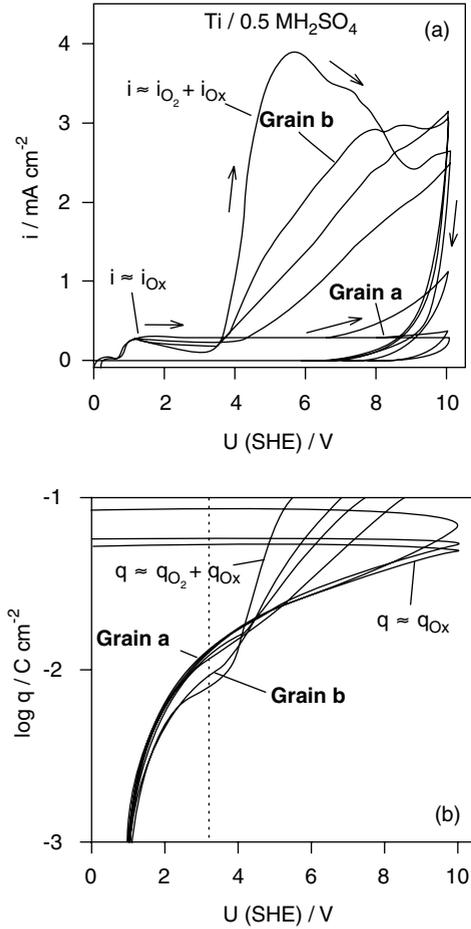
#### 1.3.1.7.1 Cyclovoltammetry

*Anodic Passive Layer Formation on Single Ti Grains* The following measurements were performed on single grains of polycrystalline Ti. In some instances the experimental results are discussed for two deliberately selected grains (a) and (b), because the aspects of the different behavior are represented sufficiently. Prior to the electrochemical measurements, the surface orientation of these grains and the thickness of the anodic oxide layers was determined by SAME. In Figure 1.16 several cyclic voltammograms are shown, which were obtained on a freshly electropolished Ti sample. Obviously, the texture has a significant influence on the anodic current density. The total anodic current density  $i$  is composed of four contributions:

$$i = i_{\text{ox}} + i_{\text{O}_2} + i_{\text{corr}} + i_{\text{C}} \quad (1.22)$$

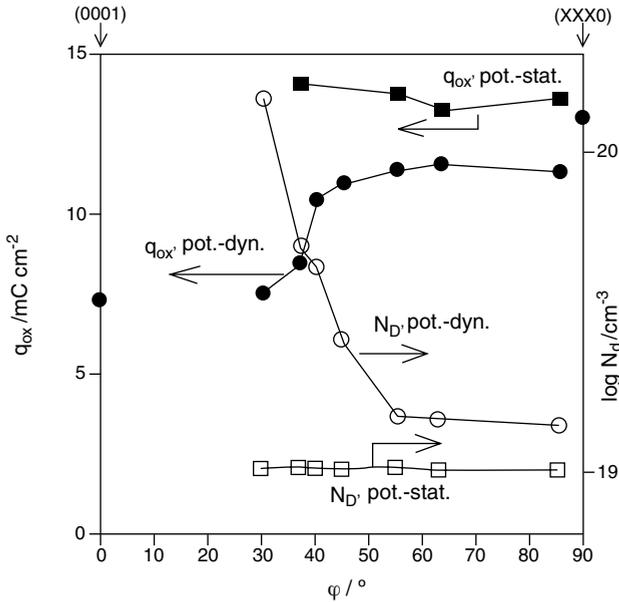
where  $i_{\text{ox}}$  is oxide formation,  $i_{\text{O}_2}$  oxygen evolution,  $i_{\text{corr}}$  corrosion current and  $i_{\text{C}}$  is due to capacitive charging. The last two contributions can be neglected as  $i_{\text{C}}$  does not exceed  $2 \mu\text{A cm}^{-2}$  ( $dU/dt = 50 \text{ mV s}^{-1}$ ,  $C_{\text{H}} = 20 \mu\text{F cm}^{-2}$ ) and  $i_{\text{corr}}$  was found to be less than 8% in the potentiodynamic preparation mode [92].

In the potential region from 0 to 3 V SHE the oxygen evolution can be excluded and the anodic current density is purely the oxide formation  $i_{\text{ox}}$ . Thus, the anodic charge of the oxide layer formation depends on the texture of the underlying Ti. For grain (a),



**Figure 1.16** Current density (a) and charge (b) during the anodic oxidation on different grains of a polycrystalline Ti sample. Diameter of the microelectrode 20  $\mu\text{m}$ ,  $dU/dt = 50 \text{ mV s}^{-1}$  in 0.5 M H<sub>2</sub>SO<sub>4</sub> [6].

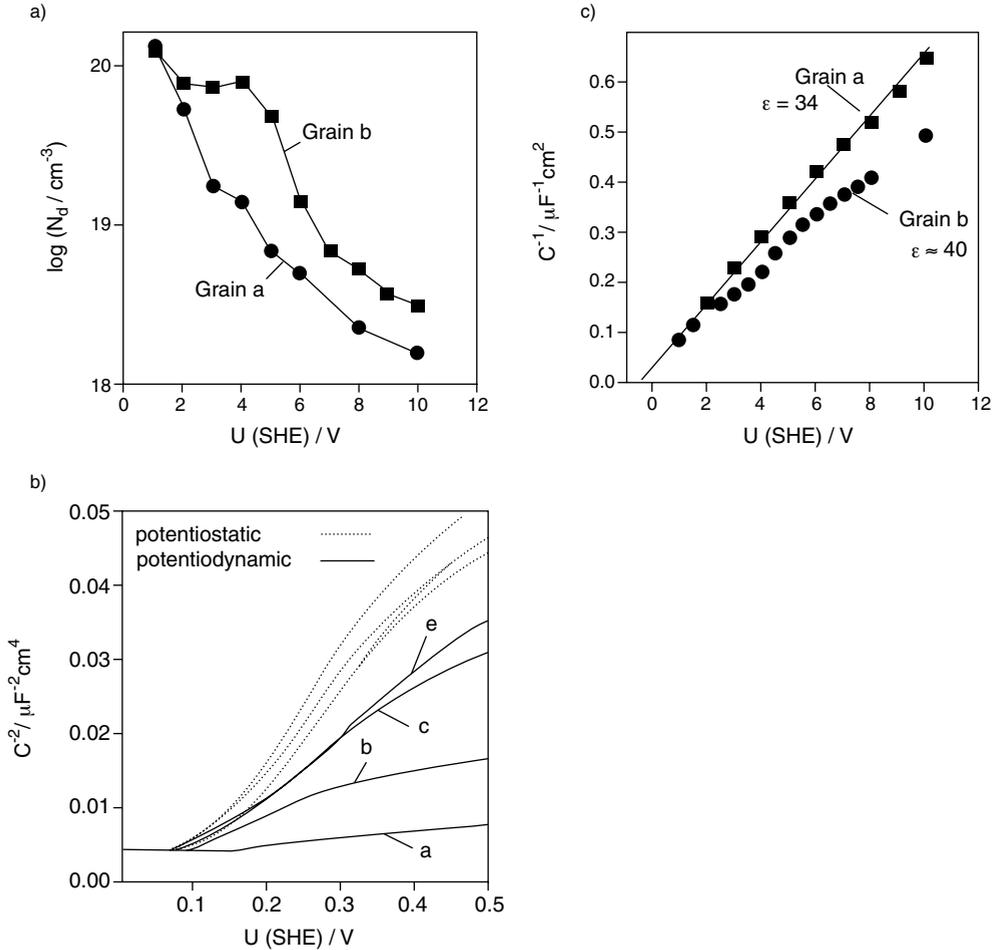
with an orientation angle  $\phi = 85^\circ$ , the current density is independent of the potential, corresponding to a proportional growth of the oxide thickness with the potential  $U$ . For grain (b), with an orientation angle  $\phi = 37^\circ$ ,  $i$  decreases with  $U$ , thus the oxide formation rate is potential dependent. The relationship between surface orientation, expressed by the orientation angle  $\phi$ , and anodic oxide charge  $q_{ox}$  is systematic, as plotted in Figure 1.17. At orientation angles  $<30^\circ$ , [near to the (0001) orientation] the anodic charge is 30% less than at orientation angles  $>50^\circ$ . A sharp transition is observed at  $40^\circ$ . The values for the (0001) and (xxx0) orientation are taken from measurements at macroscopic single crystal electrodes. These experiments prove that standard electrochemical measurements can be extended into the  $\mu\text{m}$  range.



**Figure 1.17** Anodic charge  $q_{ox}$  and donor density  $N_D$  as a function of the orientation angle  $\varphi$  for (0001) and (xxx0) orientation and potentiostatically (fast) grown oxide layers. For the potentiodynamically grown oxides, the oxide charge was integrated from 0.5 to 3 V (SHE), for the potentiostatic grown oxides from 0 to 4 V. Values for (xxx0) and (0001) orientation were taken from measurements on macroscopic single crystal electrodes [6].

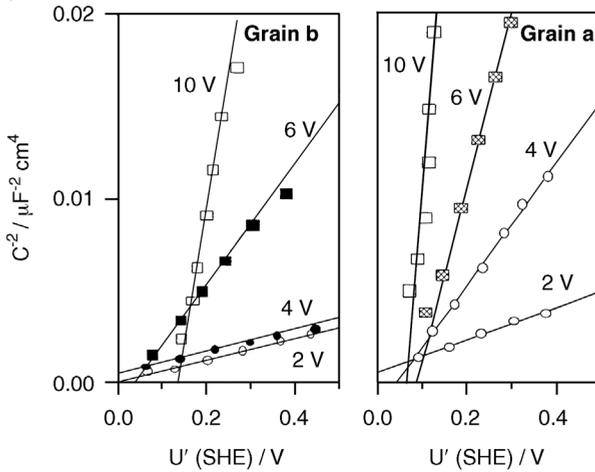
In the potential region above 3 V, additional oxygen evolution may contribute, which also depends on the surface orientation. On grain (a) [close to (xxx0)] only a slight increase in the current density can be observed at  $U > 8$  V, whereas on grain (b) [close to (0001)] the current rises up to 10-times the oxide formation current. A correlation with the oxide formation current can again be found. The oxygen evolution increases with a decrease in the anodic charge between 0.5 and 3 V. As demonstrated below, this is due to an increased conductivity of the oxide layers.

**1.3.1.7.2 Capacitance Measurements** As outlined earlier, the resist capacitance can be neglected, if the electrolyte covered resist surface is reduced, for example,  $3 \cdot 10^{-4} \text{ cm}^2$  for a  $50 \mu\text{m}$  electrode. Typical capacitance values of a  $50 \mu\text{m}$  diameter electrode at anodic potentials of  $U > 5$  V are  $> 100$  pF. Figure 1.18a and b shows the capacitance measurements and the corresponding Schottky–Mott charts for four different grains, including again the grains a and b. Two different measurement conditions namely potentiodynamic and potentiostatic are compared (analogues with the conditions chosen for Figure 1.17). In addition, in Figure 1.18c the reciprocal capacitance is shown as a function of the formation potential for grains a and b under potentiodynamic conditions. Experimental values are represented by a straight line for grain (a) (xxx0) orientation. A dielectric constant of  $\epsilon = 34$  can be calculated by a simple capacitor model. In contrast, for example, for grain (b) (0001) a nonlinear behavior reflects the nonlinear growth. An average dielectric constant of  $\epsilon = 40$  can be



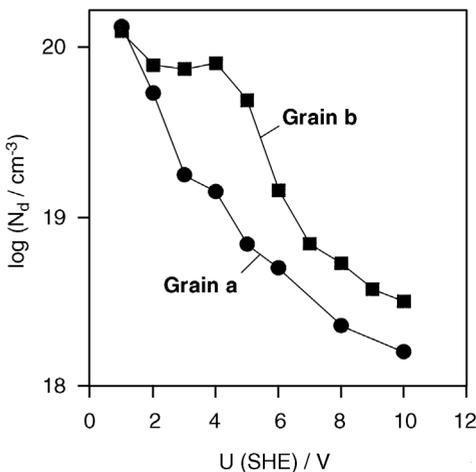
**Figure 1.18** (a) Capacitance measurements and formation potential  $U$  for grains a and b (potentiodynamic formation,  $0.5 \text{ M H}_2\text{SO}_4$ ,  $20 \text{ mV s}^{-1}$ .) The capacitance was measured at the upper formation potential with  $f = 1030 \text{ Hz}$ . The film thickness was measured ellipsometrically [6]. (b) Schottky–Mott plot for four different Ti grains and two different experimental formation conditions (potentiodynamic and potentiostatic). (c) Reciprocal capacitance  $C$  plotted against the

estimated, which still lies significantly below the values given in the literature (see e.g. Table 1.1). The corresponding evaluation for the potentiostatic oxide formation gives  $\epsilon_r$  values much closer to the literature of about 60. This again confirms the importance of the experimental formation conditions on the electronic properties of the oxides. At lower potentials than the formation potential, for films formed at 2, 4, 6 and 10 V the capacitance values are plotted according to the Schottky–Mott equation in Figure 1.19 (only the potentiodynamic case is shown). The slope of the curves is a function of the relative dielectric constant  $\epsilon_r$  and the donor density  $N_D$  as pointed out

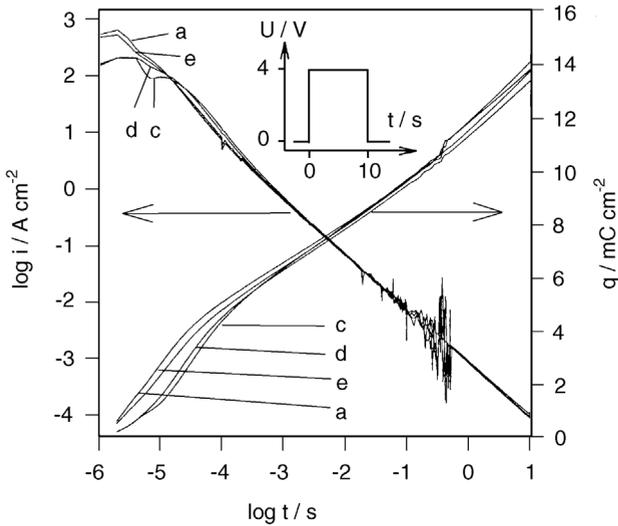


**Figure 1.19** Evaluation of the capacitance according to the Schottky–Mott equation for grains a and b for oxide layers grown potentiodynamically at different formation potentials  $U$  (100  $\mu\text{m}$  electrodes,  $f = 1030 \text{ Hz}$ ,  $dU/dt = 20 \text{ mV s}^{-1}$ ) [6].

in Section 1.2.2. Below 0.5 virtually straight lines are observed. Here only the slopes of the curves were evaluated. In the case of grain (a) (xxx0), the slope increases with the formation potential. In contrast, grain (b) (0001) shows an almost constant slope up to a formation potential of 4 V. According to the Schottky–Mott equation, donor densities are calculated and plotted as a function of the formation potential, shown in Figure 1.20. In the potential region between 3 and 5 V (SHE) donor densities differ



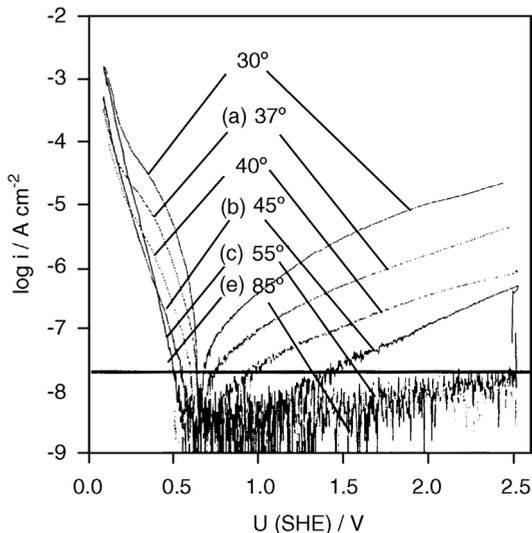
**Figure 1.20** Defect state densities  $N_D$  of the passive films on grains a (xxx0) and b (0001) as a function of formation potential derived from the Schottky–Mott plots [6].



**Figure 1.21** Double logarithmic plot of current density and time  $t$  for a potentiostatic pulse of from 0 to 4 V (SHE) on four different grains with different orientations. Microelectrode diameter was 100  $\mu\text{m}$ .

by almost one order of magnitude, underlining the texture dependent electronic properties of the passive layers. Again, the change in the donor density is a systematic function of the crystal orientation, as already indicated in Figure 1.17 for potentiodynamically formed oxides.

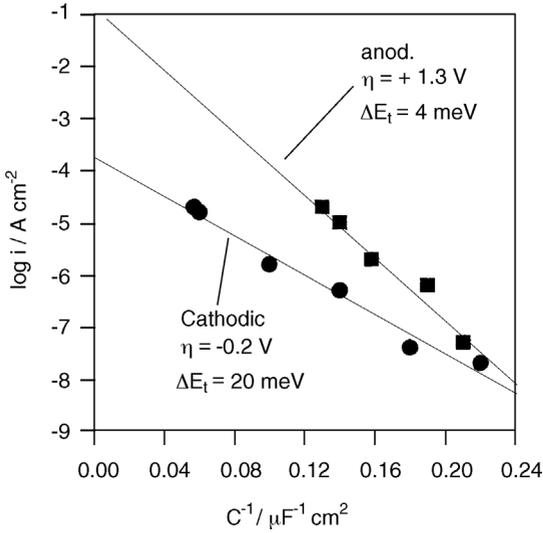
**1.3.1.7.3 Transient Measurements** One of the main features of microelectrodes is their suitability for the study of fast electrode reactions. Owing to a low potential drop in the electrolyte and low absolute currents, the potential of the microelectrode can be controlled very accurately. In this instance, the formation of anodic oxide layers was investigated as a current response to a potential-step experiment (potentiostatic oxide formation). The potential of the oxide free electrode (natural oxide) is jumped abruptly to the formation potential. Figure 1.21 shows time and current in a double logarithmic plot for an anodic pulse from  $U = 0$  to 4 V (SHE). The potential control of the electrode was achieved within a few microseconds. High current densities of more than  $100 \text{ A cm}^{-2}$  could be realized, with the absolute values of only some  $\text{mA cm}^{-2}$ . Time and current could be followed over almost seven orders of magnitude by using a fast transient recorder in combination with automatic amplifier sense switching. In contrast to the slowly grown potentiodynamically formed oxides, for all grain orientations, charge and current is almost identical. Again, prior to the measurement the orientation of each grain was determined by microellipsometry. Thus, for fast grown oxides the influence of the texture is decreased drastically. The slope  $d \log i / d \log t = -1$  is in agreement with an oxide growth according to a high field mechanism. Additional evidence for the grain independent properties of the fast grown oxides has already been indicated in the capacitance measurements of



**Figure 1.22** Tafel plots of ETR with  $0.5 \text{ M Fe}^{2+}/\text{Fe}^{3+}$  redox system in  $0.5 \text{ M H}_2\text{SO}_4$  on different grains of a polycrystalline sample. The orientation of the grains is given as the angle  $\varphi$ . The current without the redox system is subtracted. The current detection limit is indicated by the horizontal line ( $d = 200 \mu\text{m}$ ,  $dU/dt = 5 \text{ mV s}^{-1}$ ) [6].

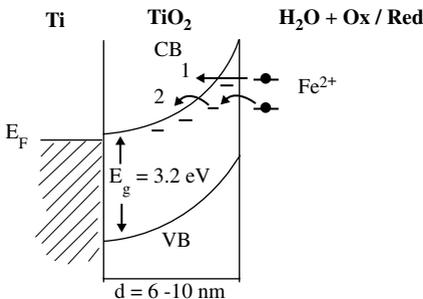
Figure 1.18 and will be further confirmed by the electron transfer reaction (ETR) measurements below. The donor densities of the fast grown oxide layers are lower than for the potentiodynamically formed oxides, indicating a more isolating character (see Figure 1.17) [258].

**1.3.1.7.4 Electron Transfer Measurements** ETR measurements were carried out in a  $0.5 \text{ M Fe}^{2+}/\text{Fe}^{3+}$  redoxsystem in  $0.5 \text{ M H}_2\text{SO}_4$  after the oxide layers were formed in a slow growth mode, also in  $0.5 \text{ M H}_2\text{SO}_4$  with a formation potential of  $4 \text{ V}$ . Capacitive charging and ionic currents are subtracted, so that the Tafel plots in Figure 1.22 represent only the contribution of ETR. Again, each curve represents a grain with a different crystal orientation. As it is not the subject of this text to elaborate on the various mechanisms of ETR, only a few comments will be made here. A more detailed description is available in Ref. [42]. A direct electron exchange with the metal can be excluded due to the oxide thickness of  $6.5\text{--}10 \text{ nm}$ . On the cathodic and on the anodic site,  $\log i$  decreases with increasing orientation angle  $\varphi$ , which means from (0001) to (xxx0) orientation. In the same direction, the donor density decreases, which results in a increasing extension of the space charge layer. As the extension of the space charge layer is proportional to  $1/C$  at a given potential, the plot of  $\log i$  versus  $C^{-1}$  in Figure 1.23 suggests that a tunneling mechanism is the rate-determining step. Oxide layers with the highest donor concentration show the highest anodic current densities because of the reduced tunneling distance to the conduction band



**Figure 1.23** Cathodic and anodic ETR current densities at a constant overvoltage of  $\eta = -0.2$  V and  $\eta = 1.3$  V taken from Figure 1.22, plotted versus the corresponding reciprocal capacitance  $C^{-1}$  at the same  $\eta$ .

(reduced Debye length). For the (xxx0) orientation (grain e), the anodic reaction is totally blocked. On the cathodic branch at high overvoltages ( $\eta < -500$  mV), the ETR is independent of texture, which is typical for a direct elastic tunneling process (see process 1 in Figure 1.24). At lower overvoltages a texture dependent shoulder in the current density is observed, which can be explained by a resonance tunneling process (see process 2 in Figure 1.24). Oxide layers formed by a potentiostatic pulse experiment (see the previous section) show the behavior of grain (e), independent of the crystallographic orientation, underlining the insulating character.



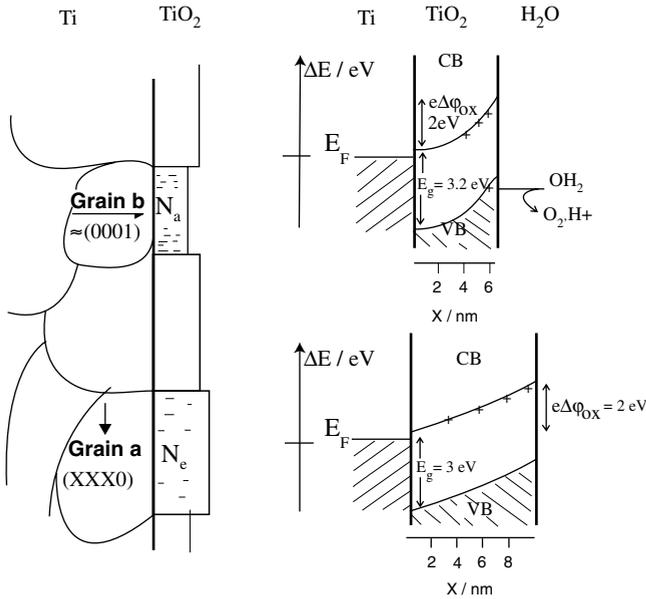
**Figure 1.24** Schematic representation of electron transfer reaction to the conduction band for direct (1) and resonance tunneling (2).

### 1.3.1.8 Summary and Conclusions for the Ti/TiO<sub>2</sub> System

The complete employment of the micro-optical and micro-electrochemical methods, which were introduced in Section 1.2, has been demonstrated for the Ti/TiO<sub>2</sub> system. Owing to its pronounced heterogeneity Ti/TiO<sub>2</sub> is ideally suited for this purpose. For the other valve metal systems that will be discussed in the following sections only results with methods relevant for the specific system will be further presented. In order to elucidate local electrode reactions it was essential that all measurements were performed under microscopic control. This allows precise measurement on deliberately chosen electrode areas. For instance, all measurements presented in this section were carried out on the same single grains of only one electropolished Ti sample.

The properties of the semiconducting TiO<sub>2</sub> films depend sensitively on the substrate texture. The new SAME method was used for *in situ* determination of the substrate grain orientation. The electronic and optical TiO<sub>2</sub> film parameters were determined by means of photoresist micro-electrochemistry and micro-ellipsometry and then correlated with the Ti substrate grain orientation. The results using photoresist microelectrodes show that conventional electrochemical measurement techniques provide valuable information on the electronic properties, even in  $\mu\text{m}$  areas. The passive layer formation on Ti depends on the grain structure in terms of anodic charge, growth factor, oxygen evolution rate, electron transfer rate and donor density. The most important results can be summarized in a geometric film model shown schematically in Figure 1.25. Because of the semiconducting character of the passive film, the potential drop across the metal electrolyte interface is mainly located in the space charge layer. The extension of this space charge layer and the corresponding distribution and availability of energetic states determine the rate of electron transfer. The electron exchange takes place over the conduction band. For the low density packed Ti surface (xxx0), the oxide growth is a linear function of the potential. The donor density is comparably low,  $10^{19} \text{ cm}^{-3}$ . Anodic reactions such as the oxygen evolution reaction are blocked. On the close packed (0001) surface, the films grow more slowly above 2 V, are highly doped,  $10^{20} \text{ cm}^{-3}$ , and allow anodic reactions due to a thinner space charge layer and reduced tunnel barrier. High growth rates reduce the effect of texture and show a more isolating character. This explains the systematic variation of the film properties such as layer thickness and defect state concentration with the substrate orientation. The micro-electrochemically determined electronic and optical film parameters were confirmed by photocurrent measurements. The anodic TiO<sub>2</sub> films were found to be amorphous with mobility gap energies close to those of the TiO<sub>2</sub> modification anatase. The TiO<sub>2</sub> films were modified at high local resolution by means of focused UV-laser illumination. Both a thickening (writing) or thinning (erasing) of the films could be realized depending on the applied potential, which therefore could be used to control the layer thickness. This allows preparation of unique structures such as semiconducting films with thickness gradients. Pitting could be also induced.

Besides the pronounced dependence of the electronic oxide properties on the substrate orientation, an especially important result is that the film properties also depend sensitively on the formation conditions. This important result is illustrated in Figure 1.17 where the cases of potentiodynamic and potentiostatic formation are



**Figure 1.25** Calculated band structure of anodically grown oxides on (xxx0) and (0001) grains at a potential of  $U = +2$  V (SHE). The oxides are formed at the same upper potential of  $U_{ox} = 4$  V with  $d_{ox} = 10$  and 6.5 nm. Dielectric constant, donor density and flat band potential were taken from measurements using photoresist.

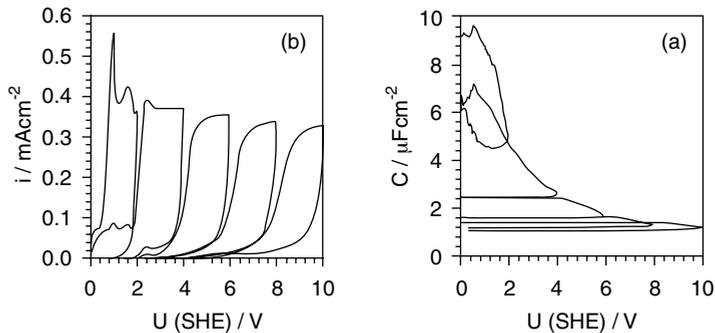
compared. The texture dependence is suppressed significantly if a potentiostatic formation mode is used and the defect state concentration  $N_D$  is decreased. This is of paramount importance for electronic applications where a homogeneous oxide is desired, to ensure maximum reliability. Consequently, a potentiostatic formation mode should be chosen for Ti if an electrolyte capacitor similar to the well established Ta/Ta<sub>2</sub>O<sub>5</sub> capacitors is to be developed. However, even then the defect state concentration of TiO<sub>2</sub> is still significantly higher than for Ta<sub>2</sub>O<sub>5</sub>, as is confirmed directly by capacitance measurements where Ti/TiO<sub>2</sub> always shows a pronounced bias dependence (Schottky–Mott behavior) whereas Ta/Ta<sub>2</sub>O<sub>5</sub> shows only dielectric behavior with no texture dependence at all. Results for the Ta/Ta<sub>2</sub>O<sub>5</sub> system will be presented in Section together with Nb/Nb<sub>2</sub>O<sub>5</sub> and Al/Al<sub>2</sub>O<sub>3</sub>. Also, the Zr/ZrO<sub>2</sub> system shows dielectric behavior only, but here again a pronounced texture dependence can be found, as will be discussed in the following section.

### 1.3.2

#### Zr/ZrO<sub>2</sub> and Hf/HfO<sub>2</sub> Systems

##### 1.3.2.1 Zr/ZrO<sub>2</sub>

For Zr/ZrO<sub>2</sub> a strong effect of the substrate texture on the oxide properties can be expected. This expectation is based on the fact that the transport number of the



**Figure 1.26** (a) Cyclic voltammogram and (b) simultaneous capacitance measurement (lock-in amplifier) during potentiodynamic  $\text{ZrO}_2$  formation on a mechanically polished Zr sample:  $0.5 \text{ M H}_2\text{SO}_4$ ,  $dU/dt = 20 \text{ mV/s}$ ,  $f = 1013 \text{ Hz}$ , amplitude  $1.13 \text{ mV}$  [17].

cations during oxide growth is approximately zero (see Table 1.1). Thus, the role of the metal/oxide phase boundary can be expected to exert a pronounced influence on film formation and will therefore cause a strong correlation between substrate crystallography and passive film properties. Unlike the usually amorphous  $\text{TiO}_2$  films, anodic  $\text{ZrO}_2$  films are predominantly crystalline [93–96]. As all  $\text{ZrO}_2$  modifications are optically anisotropic, they are amenable to SAME investigations, which should therefore reveal the potential grain-dependent differences in crystallinity. A first important elucidation of the electronic behavior of the  $\text{Zr}/\text{ZrO}_2$  system can be drawn from capacitance measurements recorded during potentiodynamic oxide formation in  $0.5 \text{ M H}_2\text{SO}_4$  at a sweep rate of  $20 \text{ mV s}^{-1}$ . This experiment, which was performed with a macroscopic, mechanically polished (homogenized) Zr electrode, is shown in Figure 1.26a. The cyclic voltammograms show the typical valve metal behavior similar to the  $\text{Ti}/\text{TiO}_2$  measurements shown in Figure 1.16. However, different to with  $\text{Ti}/\text{TiO}_2$ , no oxygen evolution occurs at potentials higher than  $3 \text{ V}$ . This is a first hint at a more insulating behavior of  $\text{ZrO}_2$ . This finding is confirmed by the corresponding capacitance measurements, which show a complete bias independence. The defect state density  $N_D$  therefore has to be well below  $10^{19} \text{ cm}^{-3}$ , which is several orders of magnitude lower than the values for  $\text{TiO}_2$ . The important conclusion therefore is that  $\text{ZrO}_2$  is an excellent dielectric. This finding is confirmed by Figure 1.26b, where a similar measurement is shown. Here an electropolished (open grain boundaries) sample was used and the sweep rate was  $100 \text{ mV s}^{-1}$ .

**1.3.2.1.1 SAME** The SAME parameters relevant to the  $\text{Zr}/\text{ZrO}_2$  system are shown schematically in Figure 1.27. The angle  $\varphi_{\text{ox}}$  describes the orientation of the oxide, the angle  $\varphi_{\text{met}}$  describes the orientation of the bare Zr surface, which has to be known before the derivation of  $\varphi_{\text{ox}}$ . Therefore, first SAME measurements on the bare Zr surfaces are presented. The results are used subsequently for the quantitative determination of the crystalline oxide parameters.

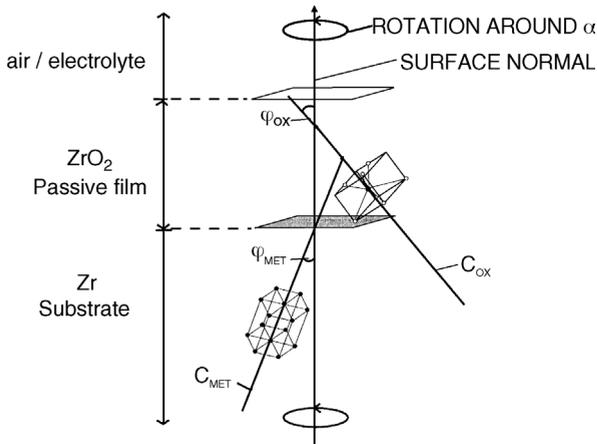


Figure 1.27 SAME parameters for the Zr/ZrO<sub>2</sub> system [17].

**SAME on Bare Zr Surfaces** As with Ti, Zr also crystallises in an hcp (hexagonal closed package) structure and is therefore also optically birefringent. In order to determine the ordinary ( $n_o$ ) and extraordinary ( $n_{ao}$ ) complex refractive indexes of the bare Zr substrate, SAME measurements on four differently oriented, freshly electropolished grains were carried out. These experimental curves were fitted simultaneously for each substrate by a least square fit procedure as explained in Ref. [308]. The resulting  $\Delta(\alpha)$  and  $\Psi(\alpha)$  simulation curves are shown as a function of the orientation angle  $\varphi$  in Figure 1.28. The experimental curves, which were recorded on the aforementioned four different Zr grains, are also indicated in this figure. Consequently, the corresponding grain orientation angles  $\varphi_{met}$  for these grains can be determined and are

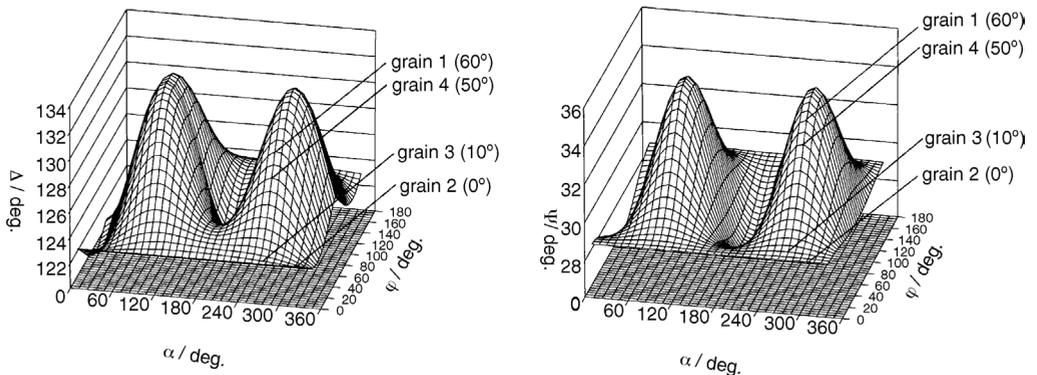


Figure 1.28 Calculated SAME curves as a function of sample rotation about angle  $\alpha$  and as a function of the orientation angle  $\varphi_{met}$ . The experimental curves for four different Zr grains are indicated together with the orientation angles  $\varphi_{met}$  determined for these grains [84, 98].

also given in Figure 1.28. The substrate parameters calculated from the simulation for a wavelength of 632.8 nm are:

$$n_o(\text{Zr}) = 2.18 - i3.41 \text{ and } n_{a0} = 2.23 - i2.54$$

These parameters can be checked independently by their consistency with macroscopically determined ones on mechanically polished samples. Mechanical polishing yields an amorphous and therefore isotropic Beilby layer resulting in an averaged isotropic complex refractive index  $n_{\text{iso}}$ . The correlation between  $n_{\text{iso}}$  and the anisotropic parameters is given by the equation:

$$n_{\text{iso}} = 2/3n_{a0} + 1/3n_o$$

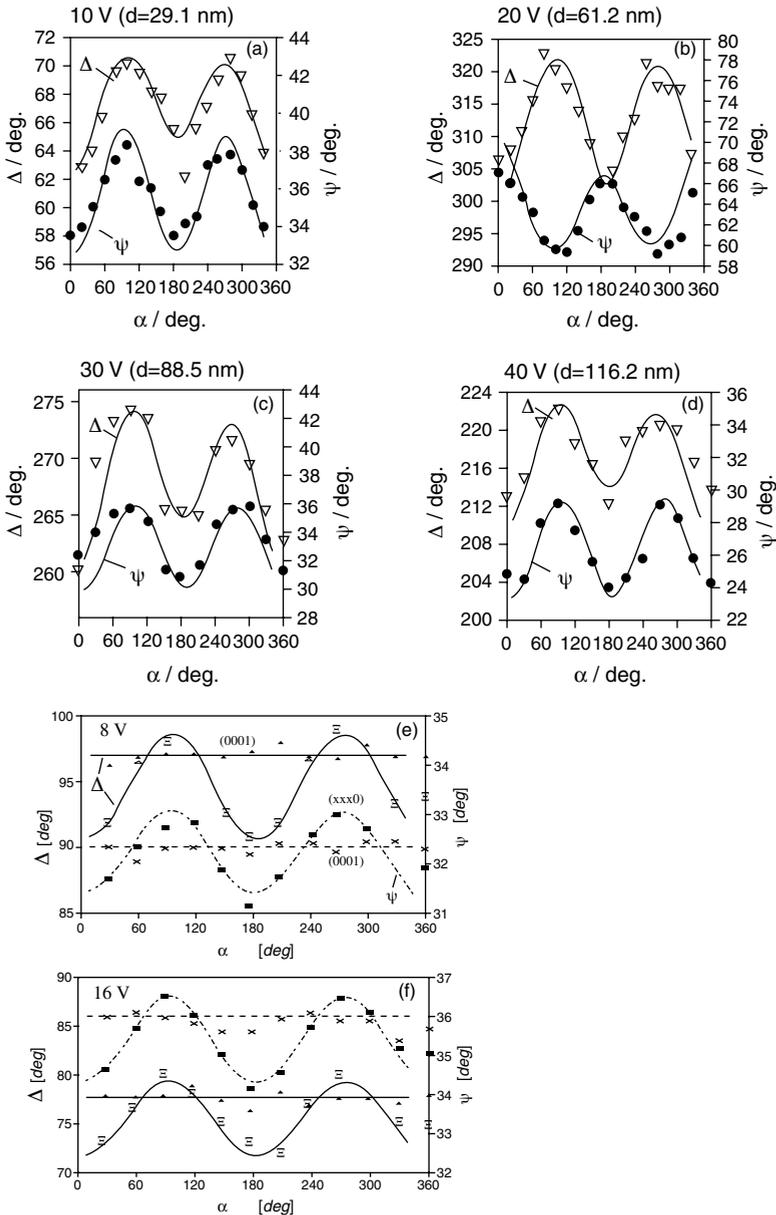
A value of  $n_{\text{iso}}(\text{Zr}) = 2.21 - i2.83$  was measured showing excellent agreement with the calculated value, according to the above equation, therefore confirming the determined anisotropic parameters.

**SAME on Zr/ZrO<sub>2</sub>** The most important ZrO<sub>2</sub> modification is baddeleyite, which has a monoclinic unit cell ( $a = 0.5169 \text{ nm}$ ,  $b = 0.5232 \text{ nm}$ ,  $c = 0.5341 \text{ nm}$ ,  $\beta = 99.15^\circ$ ). In addition, tetragonal and hexagonal ZrO<sub>2</sub> structures are discussed in the literature [94, 95]. Figure 1.29a–d shows SAME measurements taken on an (0111) oriented Zr grain for four different formation potentials (potentiodynamic,  $20 \text{ mV s}^{-1}$ ) between 10 and 40 V. Clearly, a strong dependence of the amplitudes and phase relationship between the  $\Delta/\Psi(\alpha)$  curves on the formation potential is observed. These amplitude changes and phase shifts are clearly due to the ZrO<sub>2</sub> films that contribute to the anisotropy of the system. This specific anisotropy effect of the anodic oxide constitutes clear evidence for the formation of an ordered crystalline passive film with a well defined epitaxial relationship to the substrate grain. In contrast, no such effect [phase shifts in the  $\Delta/\Psi(\alpha)$  curves] was found for TiO<sub>2</sub>, indicating the amorphous status of the TiO<sub>2</sub> oxides. For completeness, the corresponding TiO<sub>2</sub> curves are also shown in Figure 1.29, e and f. The measured curves for ZrO<sub>2</sub> can be fitted assuming a film orientation angle  $\rho$  of  $22.5^\circ$  and the following optical constants

$$n_o(\text{ZrO}_2) = 2.13 - i0, \quad n_{a0}(\text{ZrO}_2) = 2.20 - i0$$

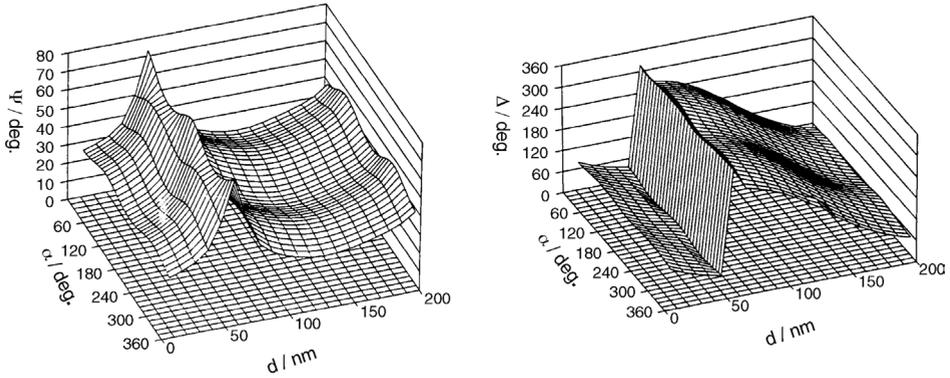
These values are consistent with literature data for monoclinic crystalline ZrO<sub>2</sub> [97]. The excellent fits of experimental data (dots) and simulations (solid lines) in fig. 1.29(a–d) is strong evidence for a *texture-dependence of crystallization processes* in anodic ZrO<sub>2</sub>films.

In spite of the biaxial nature of this material, a uniaxial approximation can be used because the two extraordinary indices are almost equal and can therefore be treated as being identical. Figure 1.30 shows the calculated  $\Delta(\alpha)$  and  $\Psi(\alpha)$  curves as a function of the film thickness using the determined parameters. Similar results were obtained on grains with orientation angles  $\phi$  between  $10$  and  $60^\circ$ . No grains with higher orientation angles could be found on the investigated polycrystalline sample. The ZrO<sub>2</sub> films exhibited two major film axis orientations, namely  $\phi_f = 22.5^\circ$  for  $\phi_{\text{sub}} > 30^\circ$  and  $\phi_f = 45^\circ$  for  $\phi_{\text{sub}} < 30^\circ$ . Apparently, in all these instances an anisotropic/anisotropic system exists and SAME reveals its full power for the study of



**Figure 1.29** (a–d) SAME curves on an (0111) oriented Zr single grain after potentiodynamic growth of the  $\text{ZrO}_2$  [84]. (d and f) Similar curves for three different Ti grains (orientation indicated) at two different formation potentials (10–40 V). The symbols refer to the experimental data, the lines represent the fit results (SAME determination of the orientation angles). Significant amplitude variations and phase shift of the  $\Delta$  curves with respect to the  $\Psi$  curves are

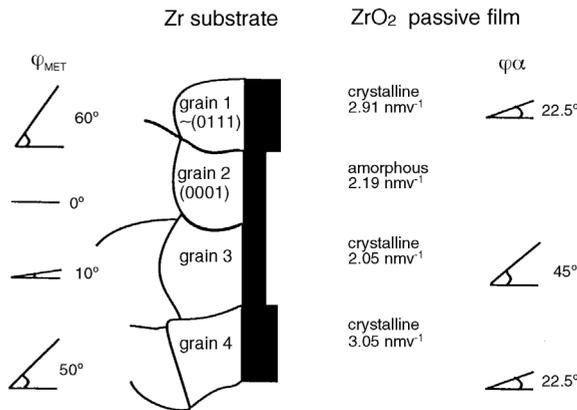
observed, indicating an epitaxial, crystalline growth of the  $\text{ZrO}_2$  [84]. (d and f) Similar curves for three different Ti grains (orientation indicated) at two different formation potentials. No amplitude and phase shifts occur constituting the amorphous character of the  $\text{TiO}_2$  films [7].



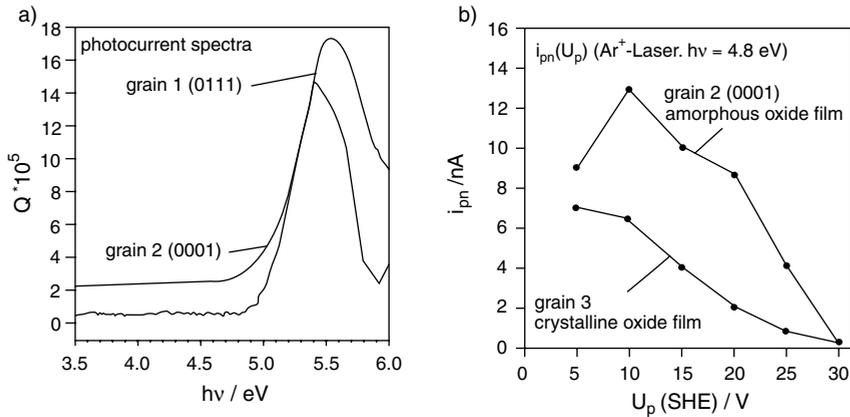
**Figure 1.30** Calculated SAME curves. The dependence of the  $ZrO_2$  thickness on the ellipsometric measureables is shown for the (0111) oriented Zr grain [17].

epitaxy relationships for this system class. However, on (0001) oriented grains (closest-packed surfaces) no anisotropy contribution of the films were observed indicating an amorphous or nano-crystalline character of the layers formed on this particular orientation. A similar behavior (amorphous film formation) is also found on mechanically polished samples. The epitaxial relationships found between substrate and films are summarized schematically in Figure 1.31, where the ellipsometrically determined film formation factors are also given.

**1.3.2.1.2 Photocurrent Spectra** Further correlation with the electronic structure of the films can be obtained by photocurrent measurements. The results are shown in Figure 1.32, with grains 1 and 2 as examples. As indicated from the photocurrent spectra (Figure 1.32a), the photocurrent quantum yield above the bandgap of 5.0 eV is



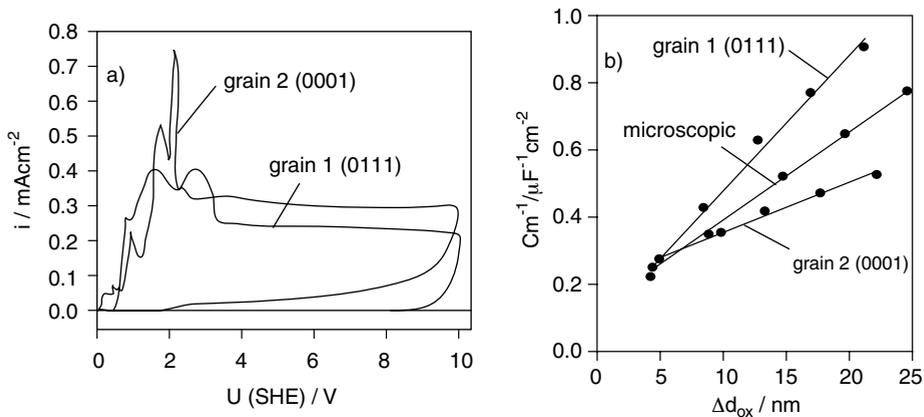
**Figure 1.31** Model for the texture dependent oxide growth on Zr surfaces. The crystallographic orientation angles of substrate Zr and oxide film  $ZrO_2$  are given in addition to the electrochemically (photoresist method) determined formation factors [17].



**Figure 1.32** Photocurrent spectra: (a) as a function of photon energy for grains 1 and 2 and (b) as a function of the formation potential; 0.5 M  $\text{H}_2\text{SO}_4$ , 23 Hz,  $U = 3$  V. The amorphous film on the grains exhibits a higher photocurrent in the sub-band regime due to the states within the mobility gap [17].

higher for the crystalline oxide films on grain 1. In contrast, the sub-bandgap photocurrent is much higher for the amorphous films on (0001) oriented grains (Figure 1.32b). This clearly points towards a higher density of states in the bandgap for the latter case, again corroborating the grain-dependent crystalline versus amorphous behavior found in the SAME experiments.

**1.3.2.1.3 Photoresist Microelectrodes** The local cyclic voltammograms on photoresist-microelectrode prepared on grains 1 and 2 are shown in Figure 1.33a. Clearly, the shape of the curves is different for each case. On grain 2, the measured anodic

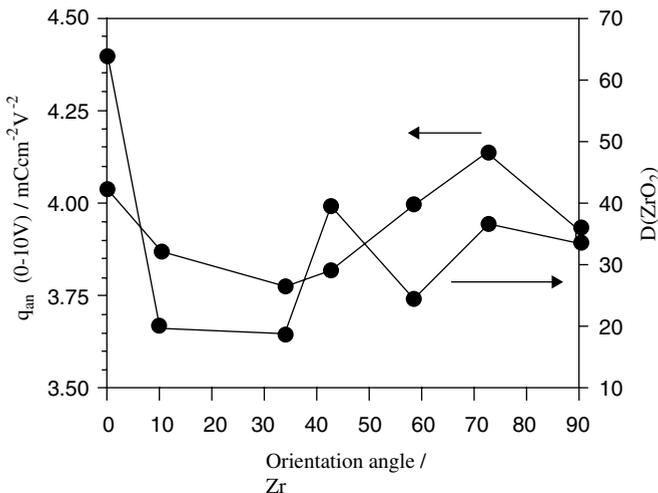


**Figure 1.33** Photoresist microelectrodes: (a) cyclic voltammograms and (b) capacitance analysis for grains 1 and 2 [17].

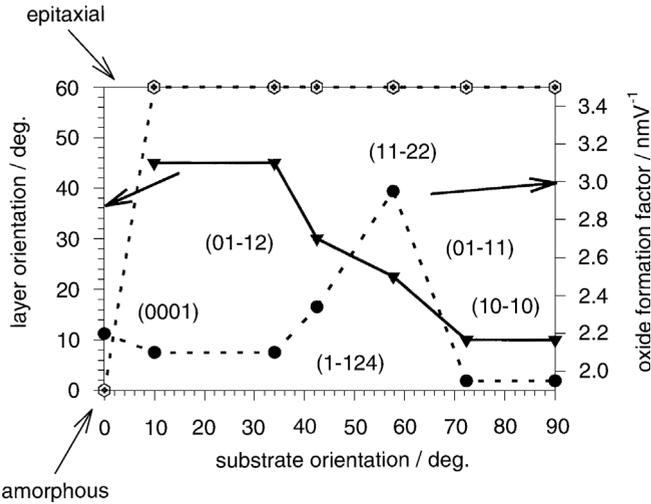
current density is higher over the entire potential range, although the layer formation factor is lower (2.2 versus 2.9 nm V<sup>-1</sup> for grain 1). This is probably due to extended side reactions in this instance, which are supported by the higher defect density. Different electronic properties can be deduced from analysis of local capacitance curves (Figure 1.33b). The capacitance is potential-independent for potentials below the formation potential, constituting the insulating behavior of ZrO<sub>2</sub>. This insulating behavior is found on all Zr grains regardless of substrate orientation. However, the absolute capacitance values show a strong dependence on the substrate. Assuming a simple capacitor model this points towards a variation in the relative permittivities for the ZrO<sub>2</sub> films formed on different substrate grains. The crystalline films on grain 1 exhibit the lowest apparent dielectric constant whereas the amorphous films on (0001) faces represent the other extreme case. These relationships are shown in Figure 1.34 for a whole variety of grains, together with the layer formation charge.

**1.3.2.1.4 Conclusions for the Zr/ZrO<sub>2</sub> System** Over the entire ZrO<sub>2</sub> film thickness range investigated here (4 up to 100 nm) and under all experimental formation conditions (potentiostatic, potentiodynamic) no bias dependence of capacitance on the applied potential was found. Apart from passive film growth, no anodic reaction could be found in the cyclic voltammograms, indicating an ideal valve metal behavior. Therefore, in contrast to the n-type semiconducting TiO<sub>2</sub>, passive ZrO<sub>2</sub> shows an ideal insulating behavior with a defect state concentration well below 10<sup>19</sup> cm<sup>-3</sup>.

SAME measurements performed on single grains of polycrystalline Zr reveal the presence of well ordered, single crystalline oxide films on all substrate orientations except (0001). The crystal structure of the oxides depends on the grain orientation in a clearly defined way. This finding is summarized in Figure 1.35, where the ZrO<sub>2</sub> film orientation angle and the oxide formation factor is shown as a function of the



**Figure 1.34** ZrO<sub>2</sub> film formation charge and relative dielectric constant ( $\epsilon_r = D$ ) as a function of the orientation angle of the Zr substrate [17].



**Figure 1.35**  $ZrO_2$  film orientation angle and oxide formation factor as a function of the Zr substrate orientation [17].

substrate orientation. Therefore, as with the Ti/TiO<sub>2</sub> system, the results for Zr/ZrO<sub>2</sub> again emphasize the strong grain-dependence of passive film growth but unlike the usually amorphous TiO<sub>2</sub> films, anodic ZrO<sub>2</sub> films are predominantly crystalline. The corresponding SAME data show excellent agreement with model calculations within the framework of SAME theory. The crystal orientations of the substrate and layer are the only adjustable parameters, and they can be determined separately by SAME measurements on the bare substrate and anodized surfaces, respectively, thus strongly supporting the consistency of the model presented here. The anisotropic/anisotropic Zr/ZrO<sub>2</sub> system is therefore ideally suited to demonstrating the full power of SAME for analysis of crystallographic properties. Both the orientation of the Zr substrate and the orientation of the epitaxial growing ZrO<sub>2</sub> films could be determined quantitatively. The pronounced texture dependence of the ZrO<sub>2</sub> film properties confirms the decisive role of the metal/oxide phase boundary on anodic oxide formation. Consistently, it was found that the cation transport number for ZrO<sub>2</sub> formation is almost zero.

The measurements presented here illustrate impressively that it is essential to consider the effect of substrate heterogeneities on passive film growth. Measurements of passive films on macroscopic surfaces can, in principle, not be quantitatively understood in terms of classical models without taking texture effects into account, as macroscopic measurements can yield only averaged values.

**1.3.2.1.5 Application of ZrO<sub>2</sub> to Electronics** For potential electronic applications of ZrO<sub>2</sub> as a dielectric or insulating film the following facts are important:

1. ZrO<sub>2</sub> shows no bias dependence of capacitance therefore proving its excellent insulating behavior.

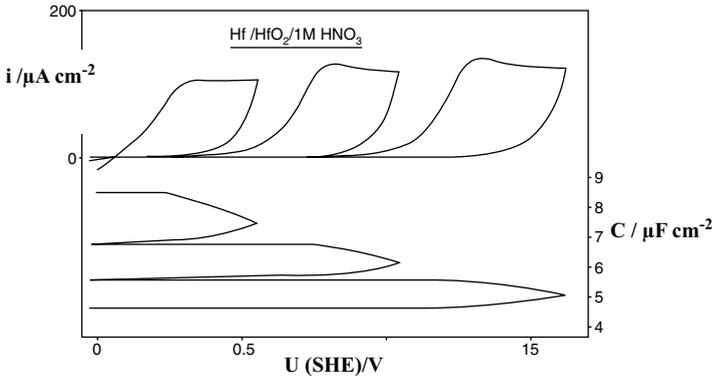
2. The relative dielectric constant  $\epsilon_r$  of  $\text{ZrO}_2$  depends strongly on the crystallographic orientation of the Zr substrate. The average value is about 27.
3.  $\text{Zr}/\text{ZrO}_2$  shows a strong texture dependence of film formation.
4. The  $\text{ZrO}_2$  films are predominately crystalline.

The last two points in particular are critical for potential applications in electronics as a thin dielectric film ( $d_f < 300$  nm). Owing to grain boundaries in the crystalline film, which act as leakage paths, and due to electronic avalanche processes, which are much more likely in crystalline than in amorphous films (because of the higher trap density in amorphous films), the breakdown voltage will be low. Additionally, the oxide thickness variation due to the texture dependence of oxide growth may cause reliability problems in the electronic devices. Nevertheless,  $\text{ZrO}_2$  has been discussed for electronic thin film applications as an additive for  $\text{Ta}_2\text{O}_5$  dielectric films or even more interestingly as a nano-laminate component in successively deposited films [99–102]. As will be discussed next, a very similar behavior is found for the  $\text{Hf}/\text{HfO}_2$  system.

### 1.3.2.2 Hf/HfO<sub>2</sub>

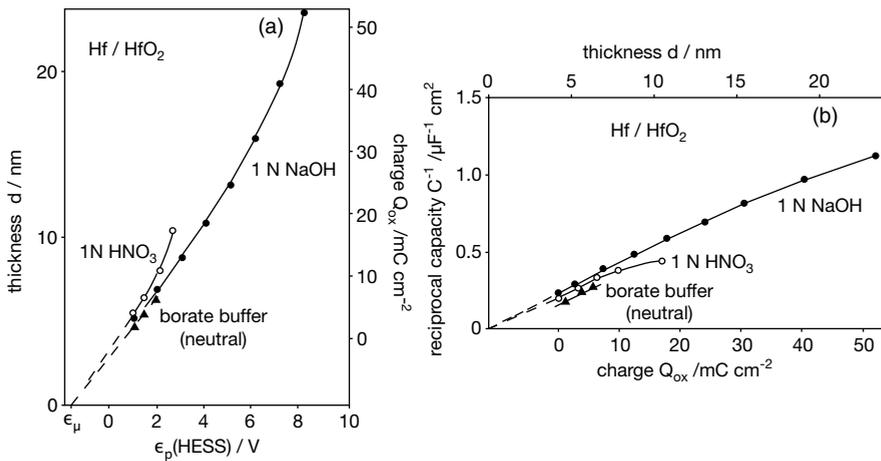
Owing to their close similarity, it makes sense to treat the  $\text{Hf}/\text{HfO}_2$  system in the same context as the  $\text{Zr}/\text{ZrO}_2$  system. The relationship between the two systems begins with their natural occurrence. Zr and Hf are typically found together ores, although Zr is much more frequent (megaton production) than Hf (about 100 ton per year). With the exception of nuclear shielding applications (reactor grade Zr), Zr materials always contain significant amounts of Hf as an impurity, which usually does no harm. Nuclear shielding is an exception because of the higher absorption efficiency of Hf (much higher density) for neutron radiation. Shielding of neutron radiation is one of the major applications of bulk quantities of Hf. However, as will be shown here,  $\text{HfO}_2$  is also an excellent dielectric material (similar to  $\text{ZrO}_2$ ), which makes it an interesting material for electronics at least in thick film applications ( $d_f > 500$  nm). In recent publications  $\text{HfO}_2$  has been discussed as a promising dopant material for advanced CVD electroceramic thin film dielectrics in IC-MOSFET (metal oxide semiconductor field effect transistor) [99–102, 104].

The first evidence of the excellent dielectric properties of  $\text{HfO}_2$  films can be seen immediately in the anodic film formation cyclic voltammograms and the simultaneously recorded capacitance measurements shown in Figure 1.36. The experiments were performed in 0.5 M  $\text{HNO}_3$  as the electrolyte with a sweep rate of  $25 \text{ mV s}^{-1}$  using a mechanically polished pure (99.9%) Hf electrode. The capacitance curves were recorded by means of a lock-in amplifier set to a frequency of 1013 Hz with a signal amplitude of 2 mV. Similar results were obtained in NaOH or borate buffer as the electrolytes indicating the outstanding stability of the oxides to aggressive environments. The results were taken from Ref. [103]. As for the  $\text{Zr}/\text{ZrO}_2$  system, no bias dependence of capacitance is found for potentials below the formation potential confirming the insulating character of the oxides. Again an ideal valve metal behavior is found with almost zero current density for anodic potentials below the formation potential. The coulometrical analysis [ $d_f = q_{\text{ox}}M/(zF\rho r)$ ] of the cyclic



**Figure 1.36** Cyclic voltammograms of  $\text{HfO}_2$  film formation and simultaneously recorded capacitance measurements in 0.5 M  $\text{HNO}_3$  [103].

voltammograms yields an  $\text{HfO}_2$  formation factor of about  $2 \text{ nm V}^{-1}$ . For this, a surface roughness factor  $r$  of 1.5,  $M = 210.5 \text{ g cm}^{-3}$  and density  $\rho = 9.7 \text{ g cm}^{-3}$  were assumed. The corresponding curves for all three mentioned electrolytes are shown in Figure 1.37. Evaluation of the reciprocal capacitance as a function of the formation charge or film thickness, respectively, allows for determination of the dielectric constant (see Figure 1.37b). A dielectric constant  $\epsilon_r$  of 16 could be determined, which is significantly lower than the corresponding values for  $\text{ZrO}_2$  ( $\epsilon_r = 27$ ) and  $\text{TiO}_2$  ( $\epsilon_r = 56$ ).



**Figure 1.37** (a) Coulometrically determined film thickness and film formation charge as a function of the formation potential. Determination of formation factor, ca.  $2 \text{ nm V}^{-1}$ . (b) Reciprocal capacitance and film thickness as a function of formation charge for determination of the relative dielectric constant  $\epsilon_r = 16$  [103].

**1.3.2.2.1 Texture Dependence of HfO<sub>2</sub> Film Formation** Hf also crystallises in an hcp structure and the HfO<sub>2</sub> oxides show the same monoclinic structure as the ZrO<sub>2</sub> oxides (coordination number = 7). Owing to the zero cation transfer number, again a pronounced texture dependence of the oxide formation with crystalline oxide films is to be expected. This can immediately be confirmed by looking at the interference colors of the anodically formed layers on an electropolished (open grain boundaries) electrode surface. As for the Zr/ZrO<sub>2</sub> system, the interference colors of the formed HfO<sub>2</sub> oxides vary from grain to grain. This means that all the measurements presented for Zr/ZrO<sub>2</sub> in the previous section could be repeated. In particular, SAME could be successfully applied again. This is a task for a forthcoming study and has not yet been carried out.

However, some important facts that are crucial for potential electronic applications have already been established at this stage. Basically, the same conclusions as for the Zr/ZrO<sub>2</sub> system hold, that is:

1. Anodic HfO<sub>2</sub> shows an insulating behavior without any bias dependence of capacitance.
2. The dielectric constant on mechanically polished surfaces is 16.
3. Hf/HfO<sub>2</sub> shows a strong texture dependence of film formation.
4. The oxide films are predominantly crystalline.

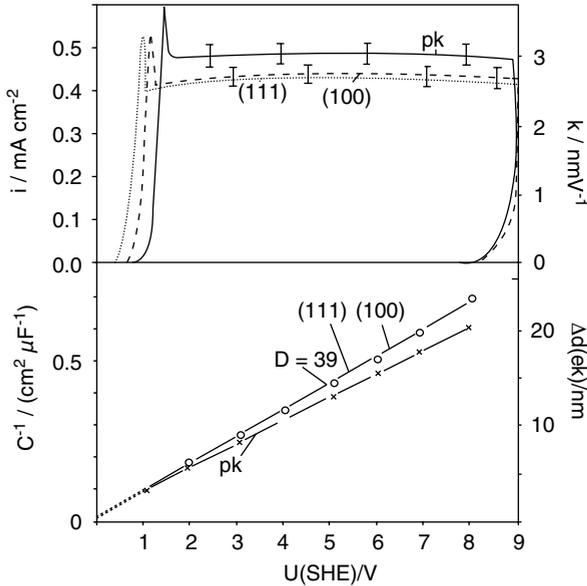
Therefore, as for ZrO<sub>2</sub>, a thin film application of pure HfO<sub>2</sub> in electronics as a functional dielectric film is doubtful, since it tends to crystallization. However, if crystallization and grain boundary formation could be suppressed, then both HfO<sub>2</sub> and ZrO<sub>2</sub> could be of interest.

### 1.3.3

#### **Systems: Nb/Nb<sub>2</sub>O<sub>5</sub>, Ta/Ta<sub>2</sub>O<sub>5</sub> and Al/Al<sub>2</sub>O<sub>3</sub>**

In contrast to the aforementioned systems Ti/TiO<sub>2</sub>, Zr/ZrO<sub>2</sub> and Hf/HfO<sub>2</sub>, the valve metal systems Nb/Nb<sub>2</sub>O<sub>5</sub>, Ta/Ta<sub>2</sub>O<sub>5</sub> and Al/Al<sub>2</sub>O<sub>3</sub> show no texture dependence on oxide growth at all. Consistently the cation transfer number of these systems is >0.5, indicating a less pronounced influence of the metal/oxide interface on electrochemical oxide formation. The anodically formed oxides are amorphous with no tendency to any crystallization even if they are exposed to high temperatures. These properties are very desirable for electronics, explaining why these materials dominate in passive component and IC applications where ultra-thin dielectrics are needed. Only the Si/SiO<sub>2</sub> system, which also exhibits amorphous oxides but with a pronounced texture dependence, can keep up with them.

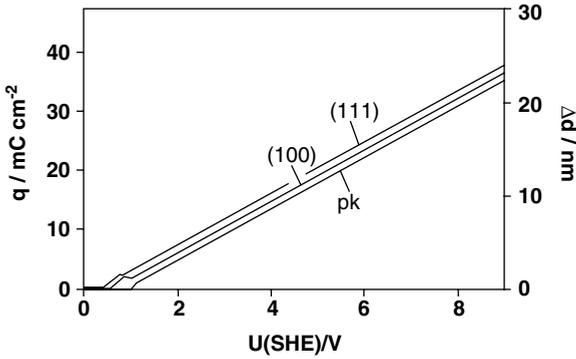
The substrate atomic structure of all of these systems shows an isotropic, cubic symmetry. Therefore, SAME can not be applied here. Owing to the texture independence of oxide growth, already indicated by the homogeneous interference colors on electropolished surfaces (no grain to grain variations), application of SAME would make no sense anyway. Only a potential crystallization of the oxides that are predominantly optical anisotropic could possibly be detected. However, no indication of any crystallization under the experimental conditions used here was found. Therefore, no SAME measurements are presented in this section.



**Figure 1.38** Potentiodynamic oxide formation cyclic voltammograms for a polycrystalline Nb electrode and two different single crystal Nb surfaces in addition to the corresponding reciprocal capacitance curves  $0.5 \text{ M H}_2\text{SO}_4$ ,  $100 \text{ mV s}^{-1}$  [18].

### 1.3.3.1 Nb/Nb<sub>2</sub>O<sub>5</sub> System

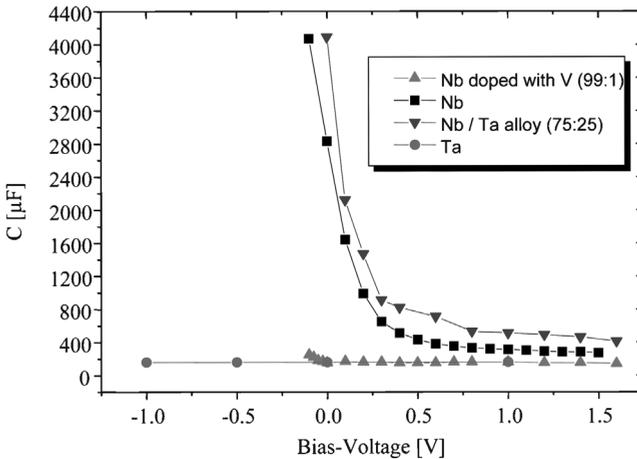
The texture independence of film formation for the Nb/Nb<sub>2</sub>O<sub>5</sub> system is confirmed in Figure 1.38, where potentiodynamic film formation cyclic voltammograms for two differently oriented Nb surfaces, (111) and (100), and an electropolished polycrystalline surface (pk) are shown together with the corresponding reciprocal capacitance curves. The cyclic voltammograms show the typical valve metal behavior. The minor differences in the current densities are due to slight differences in the surface roughness of the samples. The higher surface roughness of the polycrystalline sample can be attributed to its open grain structure. This also explains the slight difference in the slopes of the reciprocal capacitance curves. There is a small difference in the oxide formation onset potential, which might indicate a minor texture dependence of native (thermal) oxide formation. In anticipation of the results presented later, it has to be pointed out that there is no indication of any texture dependence of anodic oxide formation. The results were taken from Ref. [18]. Evaluation of the reciprocal capacitance slope yields a dielectric constant  $\epsilon_r$  of 39 in good agreement with literature values of 42. The determination of the formation factor by coulometric analysis of the formation charge and film thickness curves, respectively, is shown in Figure 1.39. A constant formation factor  $m$  of  $2.8 \text{ nm V}^{-1}$  was found, independent of the surface orientation. The measurements were performed in  $0.5 \text{ M H}_2\text{SO}_4$ , the potentiodynamic sweep rate was  $100 \text{ mV s}^{-1}$ . The



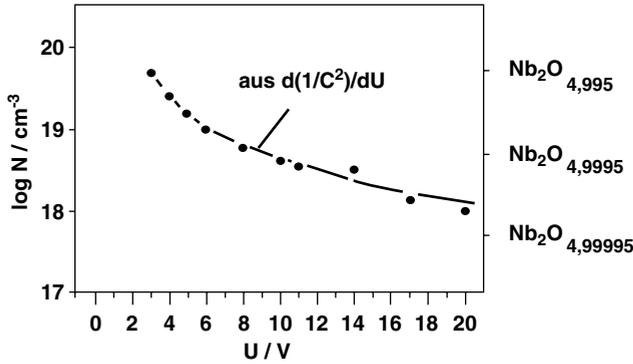
**Figure 1.39** Oxide formation charge and coulometrically determined film thickness as a function of the formation potential for three different electrode surfaces [18].

capacitance was measured in the usual way during the oxide formation using a lock-in amplifier at 1013 Hz with a signal amplitude of 2 mV.

In Figure 1.40 a comparison of  $C(V)$  curves for Nb, Ta, vanadium-doped Nb and Nb/Ta alloy electrodes is shown. Prior to these capacitance measurements, the oxides were formed at a formation potential of 30 V. In contrast to Ta, Nb and the Nb/Ta alloy show a clear bias dependence (Schottky–Mott behavior) of the capacitance indicating an n-type semiconducting behavior of the  $\text{Nb}_2\text{O}_5$ . Therefore, similar to  $\text{TiO}_2$ ,  $\text{Nb}_2\text{O}_5$  is not an ideal dielectric but exhibits a high defect state concentration  $N_D$ , which can be attributed to oxygen vacancies. This is an important finding with respect to a potential application of Nb oxide as a capacitor dielectric. In comparison with  $\text{Ta}_2\text{O}_5$  or  $\text{Al}_2\text{O}_3$ , a higher dielectric leakage and less thermal stability with respect to



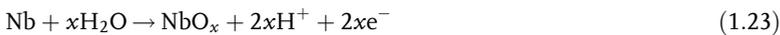
**Figure 1.40** Bias dependence of capacitance on Nb, Ta, Nb/Ta alloy and V-doped Nb. Prior to these measurements an oxide was formed at a formation potential of 30 V.



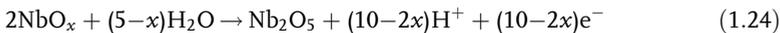
**Figure 1.41** Defect state concentration  $N_D$  determined by Schottky–Mott analysis of capacitance curves and corresponding Nb oxide stoichiometry as a function of the formation potential [18].

dielectric breakdown can be expected for Nb oxides. Interestingly, the bias dependence can be completely suppressed by a V-doping. V seems to stabilize the Nb<sub>2</sub>O<sub>5</sub> structure and decrease the oxygen vacancies [104]. The defect state, that is, the oxygen vacancy concentration of pure Nb, however, turns out to be a function of the formation potential and film thickness, respectively. This finding is shown in Figure 1.41. The  $N_D$  data were obtained by Schottky–Mott analysis of capacitance curves for various formation potentials. The defect state concentration decreases with increasing film thickness and seems to reach saturation at a formation potential above 20 V. The defect state concentration can be correlated with the stoichiometry of the Nb oxides, that is, the number  $x$  of oxygen vacancies in Nb<sub>2</sub>O<sub>5-x</sub> can be determined quantitatively. The result is also shown in Figure 1.41. For the 20 V film, a defect state concentration  $x$  in the ppm regime is found. Consistently, it was found that a V-doping in the ppm regime is sufficient to suppress the bias dependence.

For completeness, it has to be mentioned that through XP-spectra (X-ray photoelectron spectroscopy) an indication of the formation of an Nb suboxide film NbO<sub>*y*</sub> between the Nb metal and the Nb<sub>2</sub>O<sub>5</sub> was found [18]. Electrochemically this would point towards a two-step oxide formation. In the first step a thin metal-like, conducting suboxide forms at the metal/oxide interface according to the reaction:



In the second step this oxide is further oxidized to the dielectric Nb<sub>2</sub>O<sub>5</sub> form:



The oxide formation according to this two-step process is consistent with the thermodynamics. In the corresponding Pourbaix diagram, stable NbO and NbO<sub>2</sub> modifications exist between Nb and Nb<sub>2</sub>O<sub>5</sub>. The formation of the suboxide in the first step can not be seen in the capacitance measurements due to its conductivity. Therefore, a more anodic oxide formation potential  $U_{\text{ox}}$  is determined from the reciprocal capacitance curve. However, the slope of the curve used for determination

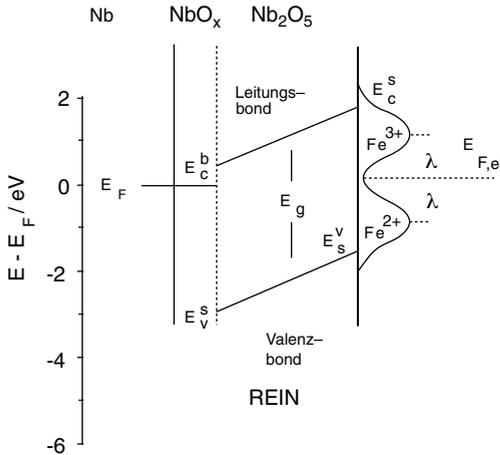


Figure 1.42 Resulting model for band structure for Nb and Nb<sub>2</sub>O<sub>5</sub>.

of the dielectric constant is not affected. The resulting model for the band structure is shown in Figure 1.42.

A good direct confirmation of the texture independence of the Nb oxide formation on Nb substrate is shown in Figure 1.43. Here SEM micrographs of sintered Nb-particles are shown after anodic formation of a Nb<sub>2</sub>O<sub>5</sub> layer. As will be discussed in full detail later (chapter 3.4), such sponge-like structures are used for fabrication of ultra-high capacitance electrolyte capacitors. The Nb works as the anode with Nb<sub>2</sub>O<sub>5</sub> as the capacitor dielectric. This structure is impregnated with MnO<sub>2</sub> which works as the cathode counter electrode. The cross-sections in Figure 1.43 clearly show the Nb cores, which are uniformly covered by the Nb<sub>2</sub>O<sub>5</sub> film and a thin flake-like MnO<sub>2</sub> layer on top of the surface. The particles are crystalline, that is, a huge variation of crystal surfaces are exposed. The Nb<sub>2</sub>O<sub>5</sub> film shows no thickness variation at all, which is

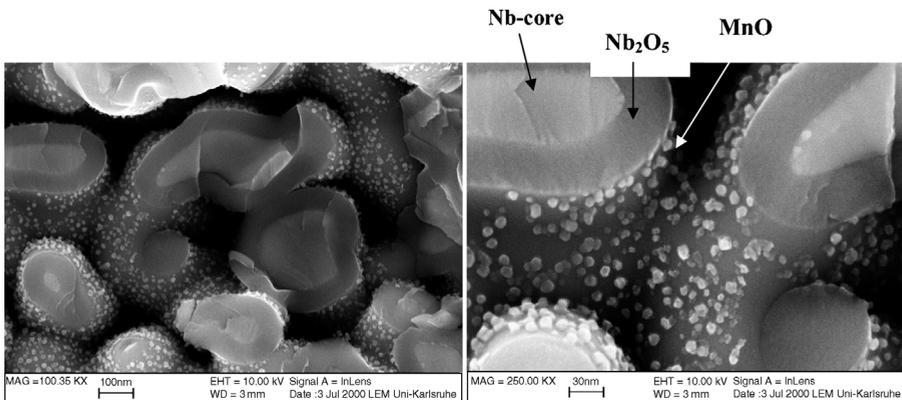


Figure 1.43 SEM cross-sections through Nb/Nb<sub>2</sub>O<sub>5</sub>/MnO<sub>2</sub> capacitor structures proving the uniform, texture independent anodic film formation on Nb,  $d_f$  ca. 90 nm [117].

beneficial behavior for such a type of capacitor application. Additional details about the electrochemical behavior of Nb/NbO<sub>2</sub> can be found in Refs. [105–152, 319, 235]. Nb/Nb<sub>2</sub>O<sub>5</sub> for electronic applications, as a capacitor material in particular, is discussed in Refs. [153–164].

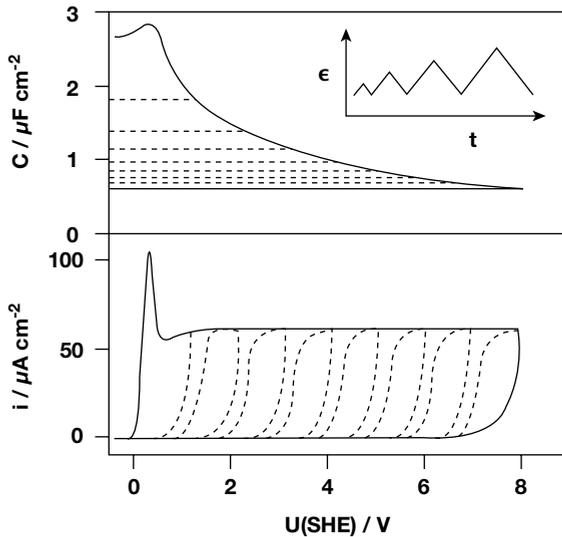
**1.3.3.1.1 Electronic Application of Nb/Nb<sub>2</sub>O<sub>5</sub> in Capacitors** The following facts are important for potential applications of thin Nb<sub>2</sub>O<sub>5</sub> films as dielectrics in electronic devices:

1. Anodic Nb<sub>2</sub>O<sub>5</sub> is amorphous with a dielectric constant  $\epsilon_r$  of about 42.
2. There is no or only negligible texture dependence of film growth in the Nb/Nb<sub>2</sub>O<sub>5</sub> system.
3. Nb<sub>2</sub>O<sub>5</sub> shows a pronounced bias dependence of capacitance, that is, Nb<sub>2</sub>O<sub>5</sub> is not a perfect insulator but shows n-type semiconducting behavior.
4. The anodic oxide formation factor  $m$  is about 2.9 nm V<sup>-1</sup>. The higher dielectric constant for Nb<sub>2</sub>O<sub>5</sub> (42) in comparison with Ta<sub>2</sub>O<sub>5</sub> (25) is, therefore, compensated by the thicker anodic oxides for a constant formation voltage, that is, capacitance-wise no advantage (capacitance gain) for Nb<sub>2</sub>O<sub>5</sub> with respect to Ta<sub>2</sub>O<sub>5</sub> is to be expected. Conversely, the capacitance volume efficiency will degrade by a factor of about 2 due to the different densities of the metal substrates (8.6–16.6 g cm<sup>-3</sup> for the metals Nb to Ta).

The first two points are beneficial for an electronic application. However, because of the last two points, no advantage with respect to tantalum, which will be discussed below, can be expected but the leakage current will be higher (point 3) and the volume efficiency for a specific charge powder will be lower. However, the cost of Nb is significantly below that of Ta.

### 1.3.3.2 Al/Al<sub>2</sub>O<sub>3</sub> System

The Al/Al<sub>2</sub>O<sub>3</sub> system is treated only briefly here, as the electrochemical film formation behavior corresponds to that of the previously discussed valve metal system. The oxide formation cyclic voltammograms and the corresponding capacitance measurements are shown in Figure 1.44. The experiments were performed in acetate buffer (pH 5.9) with a potentiodynamic sweep rate of 20 mV s<sup>-1</sup>. The cyclic voltammograms show the typical valve metal behavior and the reverse capacitance curves show no dependence on the applied bias at all, indicating a perfect dielectric behavior of the oxides. The measurements were taken from Ref. [21]. The pronounced ‘overshoot’ in the cyclic voltammogram at the onset of oxide formation is discussed in full detail in Refs. [20, 21, 165]. Evaluation of the reciprocal capacitance in the usual way yields a dielectric constant of 9, in good agreement with literature values. The coulometric analysis of the oxide formation cyclic voltammograms gives an oxide formation factor  $m$  of 2.2 nm V<sup>-1</sup>. There is no variation of the oxide interference colors on electropolished surfaces with open grain boundaries, confirming the texture independence of oxide growth. X-ray diffraction analyses give no



**Figure 1.44** Cyclic voltammogram of oxide formation for Al/Al<sub>2</sub>O<sub>3</sub> and corresponding capacitance measurements recorded simultaneously with the voltammograms. Electrolyte acetate buffer,  $dU/dt = 20 \text{ mV s}^{-1}$  [21].

indication of any crystallinity, but the oxides are strictly amorphous. The Al<sub>2</sub>O<sub>3</sub> properties can be summarized as follows:

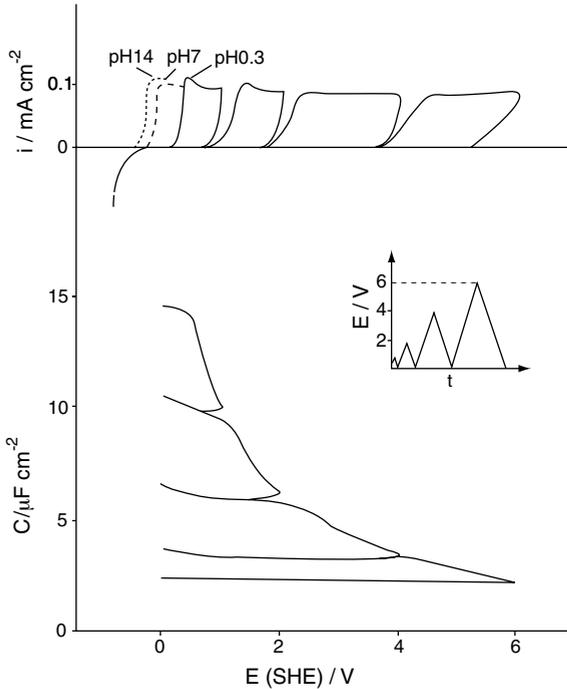
1. Al<sub>2</sub>O<sub>3</sub> shows dielectric behavior without any bias dependence of capacitance,  $\epsilon_r = 9$ .
2. The Al<sub>2</sub>O<sub>3</sub> films are amorphous.
3. There is no texture dependence of Al<sub>2</sub>O<sub>3</sub> film growth.

Thus, these oxides exhibit perfect properties for application as dielectric materials in electronics. Consistently, Al<sub>2</sub>O<sub>3</sub> is one of the most commonly applied electronic dielectrics.

A similar conclusion can be drawn for the Ta/Ta<sub>2</sub>O<sub>5</sub> system, which is treated next. Here again the electrochemical behavior will be dealt with only briefly but an extensive account of the application of this system to passive component manufacturing and the research issues involved will be given. One of the major differences between the Al/Al<sub>2</sub>O<sub>3</sub> and Ta/Ta<sub>2</sub>O<sub>5</sub> systems shows up in the way devices such as electrolyte capacitors are fabricated. For Al an etched foil technology has to be employed, whereas for Ta a sintered powder technology is possible (the difference in the metal melting point between Ta/Nb/Al is 2996/2468/660 °C). The latter technology (sintering) provides a much higher surface area, therefore allowing higher capacitance volume efficiencies to be achieved.

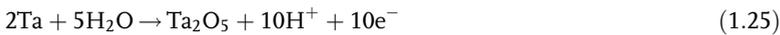
### 1.3.3.3 Ta/Ta<sub>2</sub>O<sub>5</sub> System

The typical electrochemical oxide formation on Ta is shown in Figure 1.45. Again simultaneously taken potentiodynamic cyclic voltammograms (upper part) and



**Figure 1.45** Potentiodynamic oxide formation on Ta and simultaneously recorded capacitance. 0.5 M H<sub>2</sub>SO<sub>4</sub>, with neutral (borate buffer) and alkaline (NaOH) electrolyte as dashed curves.  $dU/dt = 25 \text{ mV s}^{-1}$  (source Refs. [11, 13]).

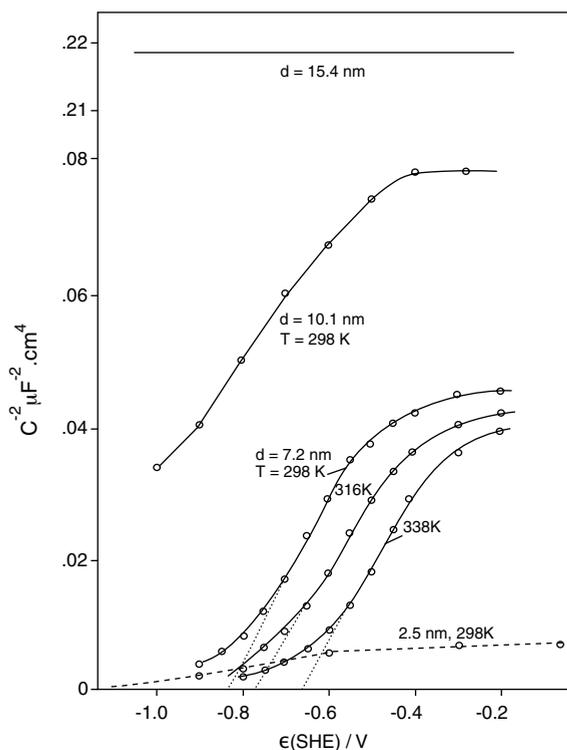
capacitance  $C$  (lower part) measurements are shown, with 0.5 M H<sub>2</sub>SO<sub>4</sub> as the electrolyte. The potentiodynamic sweep started at 0 V (SHE) and ended at increasing potentials of 1, 2, 4 and 6 V, as shown in the small potential–time program (inset of Figure 1.45). In the upper potential curve, the result of a negative run down to  $-1$  V is also shown for a qualitative demonstration of hydrogen evolution. The measurements were taken from Refs. [11, 13]. As for all of the aforementioned systems, the anodic oxide formation is an irreversible process, that is, a stable oxide is formed, which is not reduced in the reverse sweeps. According to literature [167, 168], the reaction



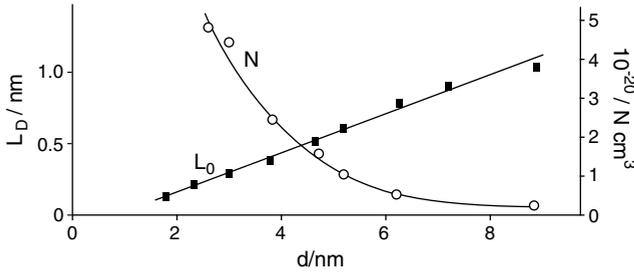
takes place with an equilibrium potential of about  $U_o = 0.75$  V (HESS) [167] ( $-0.81$  V given in Ref. [17]). In the negative run, the oxide formation stops almost immediately and the current density becomes 0. The oxide growth strictly follows the ‘high field mechanism’ with a reciprocal logarithmic film growth for potentiostatic [169, 170] and linear growth for potentiodynamic or galvanostatic conditions [166, 171], as discussed in Section 1.2.1. From the negligible current densities during repeated cycling between 0 V and the formation potential, it can be concluded that side reactions such as anodic oxygen evolution, anodic corrosion and anodic or cathodic

reactions of electrolyte compounds can be excluded. Consequently, the anodic charge  $Q$  can again be taken for a coulometric thickness determination of the films formed. From this analysis a *formation factor*,  $m$ , of  $1.9 \text{ nm V}^{-1}$  results. If the electrode is polarized in NaOH or borate buffer solution, the anodic oxide formation starts at lower potentials, referred to the SHE. This can be seen from the dashed (pH 7) and dotted lines (pH 14) in Figure 1.45 close to 0 V (see Refs. [11, 13]). The shift in the onset of oxide formation is the only difference between the acidic and neutral or alkaline solutions. The capacitance in Figure 1.45 shows the typical capacitor behavior, that is, a thickness proportional decrease during the oxide formation. Evaluation of the corresponding reciprocal capacitance as a function of film thickness allows determination of the dielectric constant. An  $\epsilon_r$  of 25.3 was determined, in excellent agreement with literature values [172].

However, the reverse capacitance scans reveal an interesting effect. For extremely thin films, formed at formation potentials below 6 V, a significant bias dependence of capacitance exists. This bias dependence decreases with increasing formation potential, or film thickness, accordingly. In Figure 1.46 a closer look is taken at this phenomenon. Here, the Schottky–Mott curves for a whole variety of  $\text{Ta}_2\text{O}_5$  film



**Figure 1.46** Schottky–Mott analysis of the capacitance measurements for a variety of  $\text{Ta}_2\text{O}_5$  film thicknesses up to 15 nm (source Refs. [11, 13]).



**Figure 1.47** Defect state density  $N_D$  and Debye length  $L_D$  as a function of  $\text{Ta}_2\text{O}_5$  film thickness (source Refs. [11, 13]).

thicknesses are shown. For the thickest film,  $d_f = 15.4$  nm, the capacity is independent of the electrode potential, which means a clear insulating behavior. For thinner films, the electrode capacity increases and the slope of the Schottky–Mott curves decrease with decreasing potentials, which means an increasing n-type semiconducting behavior (increasing number of defect states  $N_D$ ). In the region between  $-0.8$  and  $-0.4$  V almost straight lines are observed for film thickness values from 3 to 9 nm allowing the determination of the defect state concentration  $N_D$ . The corresponding result, that is, the decrease in the defect states with increasing film thickness, is shown in Figure 1.47 together with the Debye length  $L_D$ , which correlates to the space charge layer extension  $d_{\text{scl}}$  defined in Equation 1.14 previously by:

$$d_{\text{scl}} = L_D \sqrt{2e/kT \cdot \Delta\phi_{\text{ox,scl}}} \quad (1.26)$$

This result corresponds to the results discussed earlier for Ti (see also [28]) and Nb (see also [173]). With increasing film thickness, the film is exhausted of defects  $N_D$  (decrease of oxygen vacancies) and behaves as a true insulator. For capacitor applications, usually a film thickness well above 20 nm is applied. Therefore, Ta/ $\text{Ta}_2\text{O}_5$  is a perfect system for fabrication of dielectric layers in electronics. The  $\text{Ta}_2\text{O}_5$  properties are very similar to those of  $\text{Al}_2\text{O}_3$  and can be summarized as follows:

1.  $\text{Ta}_2\text{O}_5$  shows perfect dielectric behavior without any bias dependence of capacitance for a film thickness  $>15$  nm,  $\epsilon_r = 25$ .
2. The  $\text{Ta}_2\text{O}_5$  films are amorphous.
3. There is no texture dependence of film growth in the Ta/ $\text{Ta}_2\text{O}_5$  system.

Further details about the electrochemical behavior of the Ta/ $\text{Ta}_2\text{O}_5$  can be found in Refs. [174–234]. In the next section, the application of valve metal oxides in passive component fabrication with particular focus on the Ta/ $\text{Ta}_2\text{O}_5$  system is discussed.

### 1.3.4

#### Application of Valve Metals in Electrolytic Capacitor Manufacturing

##### 1.3.4.1 Capacitor Fundamentals

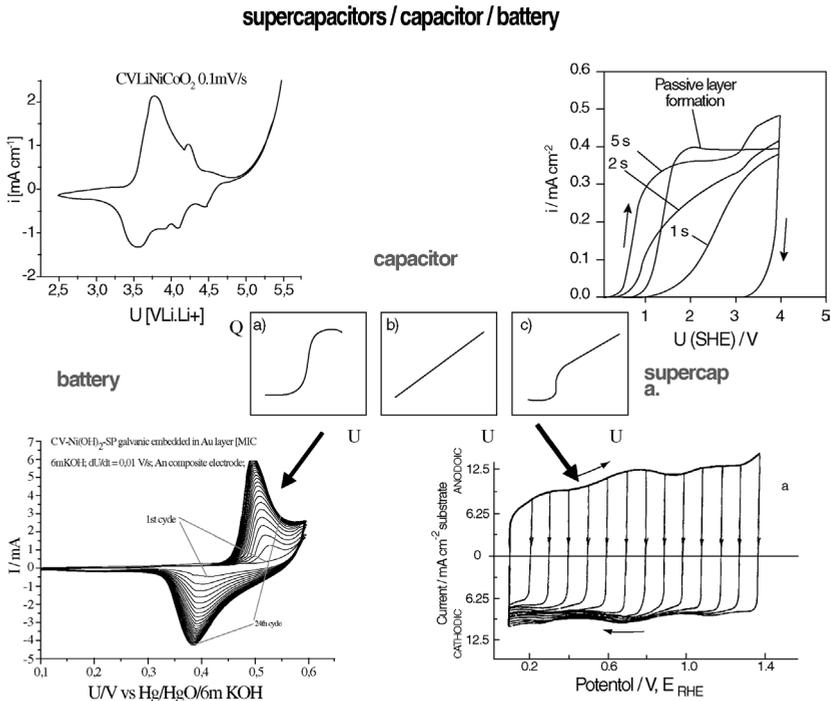
The basic function of a capacitor is the storage of electrical charge  $Q$ . This task is similar to that of a battery but in contrast to a battery, the charge in a capacitor has to be stored electrostatically and not by Faradaic processes. The capacitance of a capacitor is

simply defined by the equation:

$$Q = C U$$

that is, the capacitance  $C$  is the factor of proportionality between the applied potential and the charge. The *capacitance*  $C$  of a capacitor is not to be confused with the *capacity*  $C_{\text{bat}}$  of a battery, which is defined in a completely different manner (the theoretical specific capacity  $C_{\text{bat}}$  of a battery is defined by  $C_{\text{bat}} = nF/M$ , where  $n$  is the number of electrons involved and  $M$  the mass of the active electrode material). Charging and discharging of a capacitor are fast electrostatic processes, and are only limited by the unavoidable series resistance  $R$  in the equivalent circuit of a real capacitor. In contrast, for a battery a constant potential is desirable, that is, as much charge as possible should be drawn from a battery at a constant rated voltage. A capacitor is optimized with respect to high power densities (high frequencies) whereas a battery is optimized for high energy densities.

These facts are illustrated in Figure 1.48 where the typical  $Q$  versus  $U$  curves for batteries and capacitors are compared. Two typical cyclic voltammograms for an



**Figure 1.48** Comparison of capacitor, supercapacitor and battery behavior. On the left side, two typical cyclic voltammograms for battery electrodes [ $\text{LiNiCo}$  oxide, top, and  $\text{Ni(OH)}_2$ , bottom] are shown. Integration of the voltammograms yields the S-shape  $Q(U)$ -curve shown, which is typical for a battery. On the right

bottom side, the voltammogram of the supercapacitor material  $\text{RuO}_2$  is shown with an almost rectangular profile, yielding an almost capacitor-like  $Q(U)$ -curve. For comparison the cyclic voltammogram of  $\text{Ti}$  oxide formation is also shown on top. This CV is completely irreversible whereas the other CVs are reversible.

$\text{Ni(OH)}_2$  cathode (used in Ni/MH batteries) and an LiNiCo oxide electrode (used in Li-ion batteries) are shown to illustrate the behavior of a typical battery. The corresponding  $Q(U)$ -curve can be derived from the potentiodynamic voltammograms by a simple mathematical integration and shows an S-shaped curve, confirming that most of the charge can be drawn from the battery without significantly changing  $U$ . In this figure, the cyclic voltammogram of  $\text{RuO}_2$ , which behaves as a so-called supercapacitor is also shown. In this instance a combination of double layer capacitance (electrostatic) and Faradaic processes occurs, resulting in an almost capacitor-type  $Q(U)$  curve. The frequency response of such a supercapacitor (1 Hz regime) is much faster than for a conventional battery, whereas it is still many orders of magnitude slower than a typical capacitor. Supercapacitors are typically used to back-up batteries when high power peaks are needed, for example, for the ignition of a car or for short-term UPS (uninterrupted power supply) circuits. In contrast to the cyclic voltammograms of valve metal oxide formation, which were discussed in great detail in the previous sections, charging and discharging of batteries and capacitors are highly reversible processes.

The capacitance  $C$  of a simple parallel plate capacitor is given by:

$$C = \epsilon_r \epsilon_o A/d \quad (1.27)$$

where  $A$  is the plate surface,  $d$  the distance between the plates and  $\epsilon_o = 8.86 \text{ pF m}^{-1}$  (permittivity of a vacuum). The complex dielectric constant  $\epsilon_r$  describes the dielectric material between the capacitor plates:

$$\epsilon_r = \epsilon_r - i \epsilon_{im} \quad (1.28)$$

The important part of this equation is the dielectric constant, which was used as such in the previous sections. It describes the increase in capacitance  $C$  in comparison with the case without a dielectric material ( $\epsilon_r$  of vacuum = 1)  $C_0$ , that is  $\epsilon_r = C/C_0$ . The physical reason behind the existence of the complex dielectric constant  $\epsilon_r$  is due to the induction and orientation of electrical dipoles within the dielectric material in an applied external field. This phenomenon is called 'polarization'. The imaginary part  $\epsilon_{im}$  describes the unavoidable polarization losses, which are caused by the energy dissipation (friction) during the orientation of the dipoles. Both the real and imaginary part depend on the frequency [ $\epsilon_r = \epsilon_r(\omega)$ ] of the AC signals. Four types of polarization can be distinguished:

1. *Electron polarization*, which is due to the deformation of the electron hull of the atoms constituting the dielectric material. Owing to the small mass of the particles involved (electrons), the rate of dipole induction is very fast (highest frequency part).
2. *Ionic polarization*, which is due to an induced shift of cations with respect to anions in the dielectric material.
3. *Orientation polarization*, which is due to the orientation of molecules that exhibit a permanent dipole momentum.
4. *Space charge polarization*, which is due to accumulation of charge carriers at isolating grain boundaries.

By means of the real (Re) and imaginary (Im) parts of  $\epsilon_r$  the so-called dissipation factor (DF) =  $\tan \delta_\epsilon$  can be defined as:

$$DF = \tan \delta_\epsilon = \frac{\text{Im } \epsilon}{\text{Re } \epsilon} \tag{1.29}$$

The angle  $\delta_\epsilon$  describes the deviation of the phase shift between current and applied potential from the ideal value of  $90^\circ$ . Its projection on the real part of the total impedance  $Z$  therefore describes the ohmic part of the capacitor characteristic corresponding to a series resistance in the equivalent circuit. In practice, this number is used to specify the polarization losses of a capacitor. Analogously, the total loss factor  $\tan \delta_C$  of a capacitor is defined by the ratio of the real and imaginary part of the total impedance  $Z$ . In addition to the polarization loss, this number considers unavoidable resistances due to lead wires and losses due to an imperfect insulation, plus the capacitive inductance  $L$ :

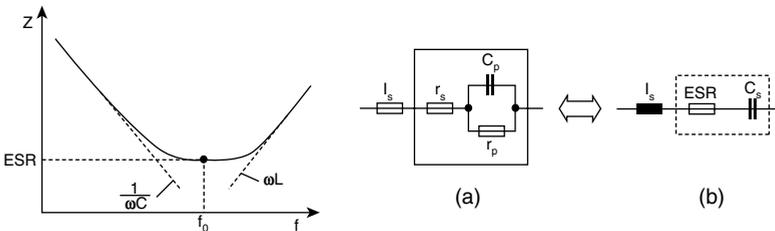
$$\tan \delta_C = \frac{\text{Re } Z}{\text{Im } Z} = \frac{1}{Q} \tag{1.30}$$

Through this equation the  $Q$ -factor is also defined, which, in addition, can be used to specify the losses or quality ( $Q$ ) of the capacitor. In Figure 1.49 the parallel and series equivalent circuits of a capacitor are shown, along with the frequency dependence of the impedance  $Z$ . Both the parallel and series circuit can be used synonymously, that is they describe an identical behavior. (The series circuit is normally preferred for high frequencies.) ESR stands for ‘equivalent series resistance’. The total impedance  $Z$  for the parallel circuit is:

$$Z = R_s + i\omega L_s + \frac{R_p}{1 + i\omega R_p C_p} \tag{1.31}$$

with

$$\text{Re } Z = R_s + \frac{R_p}{1 + \omega^2 R_p^2 C_p^2}$$



**Figure 1.49** Left: impedance  $Z$  of an electrolyte capacitor as a function of the signal frequency, where  $f_0$  is the resonance frequency. Right: identical equivalent circuits of a capacitor: (a) parallel circuit; (b) series circuit. The dashed boxes are identical according to the equations given in the text [236].

and

$$Im Z = -\frac{1}{\omega C_p} \left[ \frac{1}{1 + (\omega R_p C_p)^{-2}} - \omega^2 L_s C_p \right] \quad (1.32)$$

In order to describe an identical behavior, the dashed boxes of the equivalent circuit in Figure 1.49 have to be equal, resulting in the following relationship:

$$R_s + \frac{R_p}{1 + i\omega R_p C_p} = ESR + \frac{1}{i\omega C_s} \quad (1.33)$$

From this equation it follows that:

$$C_s = C_p + \frac{1}{\omega^2 R_p^2 C_p} \quad (1.34)$$

and

$$ESR = R_s + \frac{R_p}{1 + \omega^2 R_p^2 C_p^2} \quad (1.35)$$

Note that the relationship for  $ESR$  is identical to  $ReZ$  in the Equation 1.32. Using the definition

$$\frac{1}{R_p} = \omega C_p \tan \delta_\epsilon + \frac{1}{R_{is}} \quad (1.36)$$

and neglecting the isolation resistance  $R_{is}$  of the dielectric yields, the following relationship between the  $ESR$  and the  $DF$ ,  $\tan \delta_\epsilon$ , respectively, is obtained:

$$ESR = R_s + \frac{1}{2\pi C_p} \frac{\tan \delta_\epsilon}{1 + \tan^2 \delta_\epsilon} \cdot \frac{1}{f} \approx R_s + \frac{1}{2\pi C_N} \frac{\tan \delta_\epsilon}{f} \quad (1.37)$$

For the last approximation it was assumed that  $C_p$  corresponds to the nominal capacitance  $C_N$  and that there are only small polarization losses, that is,  $1 + \tan^2 \delta_\epsilon \approx 1$ . (Each capacitor is specified by the manufacturer with a nominal capacitance  $C_N$  and nominal or rated voltage  $V_R$ ). The quantity  $f_o$  is the 'resonance frequency'. At  $f_o$  a transition from a capacitive to an inductive behavior takes place. Further characteristic quantities for capacitors are:

- *Temperature coefficient*  $\alpha$  describing the variation of the nominal capacitance  $C_N$  (specified for 20 °C) with the temperature:  $C(T) = C_N [1 + \alpha(\text{temp} - 20^\circ\text{C})]$ .
- *Moisture coefficient*  $\beta$  describing the capacitance change with the relative change of air moisture  $F$  in % humidity:  $\beta = 1/C \, dC/dF$ .
- *Retention time* (self-discharge time) constant  $\tau$  describing the time needed for a potential drop of 37% after the capacitor was charged to the rated voltage  $V_R$ :  $\tau = R_{is}C$ , where  $R_{is}$  the isolation resistance. The associated power loss  $P$  is:  $P = U^2/R_{is} = 2W/\tau$ , where  $W$  is the energy stored in the capacitor.

**Table 1.3** Comparison of the three capacitor types, polymer foil, ceramic and electrolyte capacitor, with some examples of typical applications [263].

Polymer foil capacitors:	Ceramic capacitors:	Electrolyte capacitors:
<p><i>Dielectric material:</i> Polymer (PP, PS, PET, PC), paper</p> <ul style="list-style-type: none"> <li>• <math>\epsilon_r = 2-4</math></li> <li>• <math>d = 1-3 \mu\text{m}</math></li> <li>• C: 10 pF–10 <math>\mu\text{F}</math></li> <li>• <math>\tan \delta = 0.2 \times 10^{-3} - 5 \cdot 10^{-3}</math></li> </ul> <p>+: low cost</p> <p>–: temp. and moisture sensitive</p> <p><i>Applications:</i> Filter, high frequency, low loss, timing and tuning circuits, blocking</p>	<p><i>Dielectric material:</i> Ceramic (low K e.g. mica, high K BaTiO<sub>3</sub>)</p> <ul style="list-style-type: none"> <li>• <math>\epsilon_r = 10 - &gt;10^4</math></li> <li>• <math>d = 10-30 \mu\text{m}</math></li> <li>• C: 1 pF–10 <math>\mu\text{F}</math></li> <li>• <math>\tan \delta = 1 \cdot 10^{-3} - 50 \cdot 10^{-3}</math></li> </ul> <p>+: excellent multi-purpose capacitor</p> <p>–: aging, high temp. coeff.</p> <p><i>Applications:</i> Low K: blocking, filtering/smoothing High K: coupling/decoupling, filtering/smoothing, energy storage</p>	<p><i>Dielectric material:</i> Anodic valve metal oxides (Al<sub>2</sub>O<sub>3</sub>, Ta<sub>2</sub>O<sub>5</sub>)</p> <ul style="list-style-type: none"> <li>• <math>\epsilon_r = 2-27</math></li> <li>• <math>d = 20-500 \text{ nm}</math></li> <li>• C: 10 <math>\mu\text{F}</math>–F</li> <li>• <math>\tan \delta = 40 \cdot 10^{-3}</math></li> </ul> <p>+: highest volume efficiency</p> <p>–: high leakage current, low frequency, polar devices</p> <p><i>Typical applications:</i> Blocking, coupling, decoupling, interference suppression, energy storage, filtering smoothing, RC and timing circuits, RFI</p>

- *Ripple voltage*  $V_{\text{rip}}$  describes the maximum AC voltage that can be applied to a DC capacitor.
- *Break down voltage (BDV)* describes the highest voltage that can be applied to a capacitor without destroying the dielectric by a catastrophic breakdown.

#### 1.3.4.2 Capacitor Device Types and Production of Ta Capacitors

Three major types of capacitor devices are used as passive components for electrical circuits, that is, polymer foil capacitors, ceramic capacitors, for example, multi-layer ceramic capacitors (MLCC), and electrolytic capacitors. Each type has its merits and disadvantages. An overview of the basic features of these capacitor types is given in Table 1.3. Electrolyte capacitors are used especially for high volume efficiency applications at relatively low voltages and frequencies. In the following discussion, the electrolytic type of capacitors are dealt with specifically. Although all valve metals mentioned so far have attracted some interest, only Ta and Al have entered the market place so far. Ta capacitors show the highest volume efficiency for capacitance and have excellent reliability properties, for example, there is no aging effect. However, Ta is a rare material and thus the cost of Ta capacitors is relatively high. Therefore, increasing of the specific charge (CV product) per unit of volume or weight has been the main goal in research and development of Ta electrolytic capacitors since

their manufacturing began in the late 1950s. Higher CV provides smaller capacitor size and less consumption of the Ta powder for the same rating, which is attractive for both capacitor producers and customers. During this period of time the CV has increased more than ten times. This was mainly achieved by reducing the efficient size of the particles and by increasing of the porosity of the Ta powder used for sintering of the Ta anodes. The efficient particle size was reduced from tens of microns initially to about one micron at the present time. The reduction in the powder particle size and the adjustment of the porosity is achieved by a sophisticated chemical process. Two routes are possible. Both routes start with a 'Ta strip' solution, which is produced directly from ore concentrates by first dissolving the Ta and Nb contents of the ore in 70% HF solution and subsequently performing a solvent extraction in methyl isobutyl ketone (MIBK). The Ta remains in the MIBK solution, which is the Ta strip, whereas the Nb stays in the aqueous solution. The Ta strip can be processed in two ways, providing the two routes for Ta metal powder production:

1. A  $K_2TaF_7$  crystallization process is performed by adding KCl and HF to the Ta strip with subsequent drying and filtering. This  $K_2TaF_7$  salt is then reduced by Na in a hot salt melt (950 °C). This salt melt also contains deliberately chosen amounts of inert salts to achieve a certain dilution of the active compounds. The careful adjustment of the components in this salt mixture along with temperature and agitation speed allows the Ta nucleation process to be controlled and in turn the Ta particle morphology can be tailored. This primary powder morphology is then stabilized and further modified by downstream processing, including leaching, agglomeration, doping, consolidation and deoxidization steps.
2. A  $Ta_2O_5$  precipitation process is performed by adding  $NH_3$  to a Ta strip hydroxide solution. After subsequent calcination, a stable  $Ta_2O_5$  powder is obtained. The details of the precipitation process determine the morphology of the oxide powder. Subsequently an Mg–steam reduction of the oxide powder is performed resulting in the Ta metal powder. In contrast to the first route, here both the parameters of the precipitation and the conditions of the reduction determine the final morphology of the metal powder. Consequently, there is one additional free parameter allowing for an even better adjustment of the metal powder properties. The downstream process steps after reduction are similar to the first route.

There are many further important process details for Ta metal powder (TaMP) production that can not be disclosed here, and which are the object of continuing R&D work. It should be mentioned that Nb capacitor grade metal powder can be produced in a method similar to the second route using the aqueous Nb solution mentioned above. Some further information can be found in Ref. [237–247]. Once the TaMP is finished it can be used by the capacitor manufacturer to produce the capacitor devices. Briefly, the following process steps are used in a conventional production line:

1. Insertion of a Ta wire into the TaMP and dry pressing of the green body (anode).
2. Sintering of the anode for formation of a porous sponge-like Ta structure.

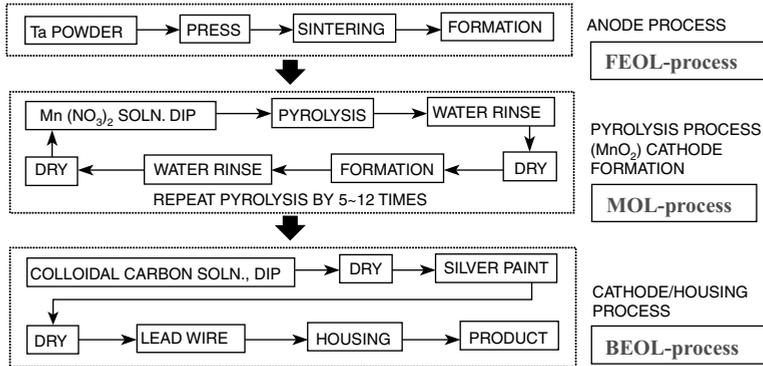
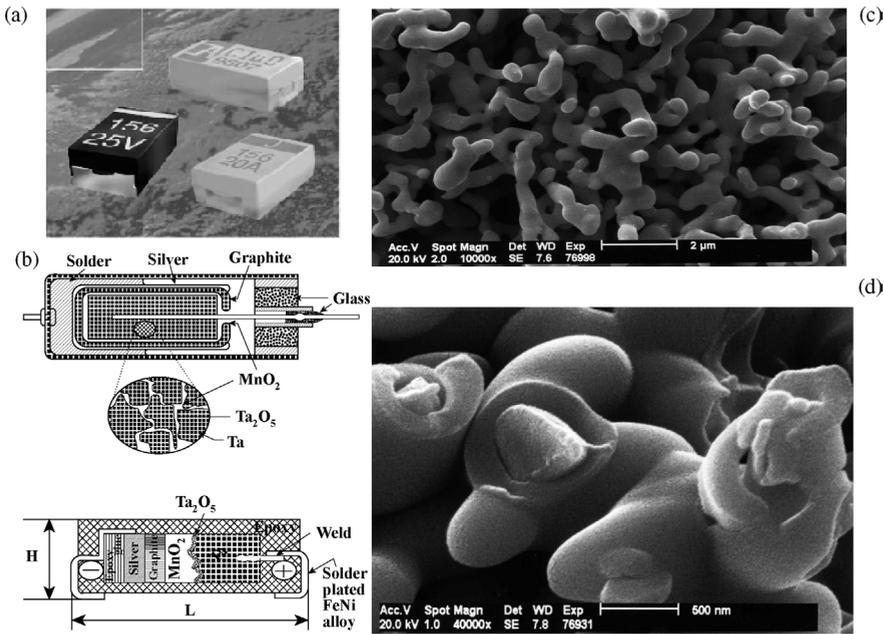


Figure 1.50 Ta capacitor production scheme.

- Anodizing of the anode in  $\text{H}_3\text{PO}_4$  for  $\text{Ta}_2\text{O}_5$  dielectric formation.
- Impregnation of the porous Ta anode with  $\text{Mn}(\text{NO}_3)_2$  solution and subsequent pyrolysis for formation of the conducting  $\text{MnO}_2$  counter electrode. This step is repeated several times in  $\text{Mn}(\text{NO}_3)_2$  solutions with increasing concentrations to accomplish a thick  $\text{MnO}_2$  layer.
- Applying of a graphite and Ag layer to improve electrical contacts.
- Encapsulation.

A detailed process flow is given in Figure 1.50. The resulting capacitor devices and the sponge-like capacitor structure are shown in Figure 1.51. In Figure 1.51d a scanning electron micrograph (SEM) of a cross-section through a broken particle is shown (analogous to Figure 1.43, which showed an Nb capacitor structure). The Ta metal core is covered by a homogeneous 100 nm thick  $\text{Ta}_2\text{O}_5$  film. The excellent lateral uniformity of the oxide confirms the texture independence of anodic oxide formation for the Ta/ $\text{Ta}_2\text{O}_5$  system. The oxide was formed in 0.1%  $\text{H}_2\text{PO}_3$  as the electrolyte.

For Al electrolyte capacitors a different process must be applied that uses an etched Al foil instead of a powder. In contrast to the sintered powder, which constitutes a three-dimensional structure, a foil principally is only two-dimensional. Consequently, the absolute surface area, that is the volume efficiency of an Al capacitor, is much lower than for the Ta types, yielding much larger device sizes for comparable capacitances. New processes for Al capacitor manufacturing make use of a solid electrolyte, which is a combination of  $\text{MnO}_2$  and a conductive polymer. However, in order to reduce the cost, most Al capacitors (98%) are still produced employing a wet electrolyte. These devices show a rather short lifetime (<5 years) as they are prone to drying out. Conversely, the lifetime of a solid Ta capacitor is literally unlimited, justifying their higher cost if better reliability is essential. The following treatment of current research issues in electrolyte capacitor development is limited to Ta exclusively.



**Figure 1.51** (a) Ta capacitors as surface mounted devices (SMD); (b) corresponding schemes; (c) SEM of sponge-like anode after oxide formation; (d) SEM with cross-section through a Ta/Ta<sub>2</sub>O<sub>5</sub> particle.

### 1.3.4.3 Current Development Trends for Ta Capacitors and Research Issues Involved

As reasoned above, the main development trend for electrolyte capacitors is the increase in capacitance volume efficiency to reduce the size and cost of the components. This goal is achieved mainly by reducing the particle size of the TaMP. With decreasing particle size of the TaMP, the sintering temperature has to be reduced from 1900–2000 °C in the past to about 1200–1350 °C at the present time. While the two physical parameters (particle size and sintering temperature) were reduced gradually, the physical situation in the Ta capacitors changed, fundamentally causing several important problems. There are two major effects:

1. *Dislocation formation:* The oxygen content in the bulk of the Ta anodes reaches the solubility limit resulting in an increased dislocation formation (crystallization) within the amorphous oxide layer. These dislocations act as leakage paths in the oxide increasing the direct leakage current (DCL) and causing defects in the dielectric. Normally the defects are not fatal but are isolated by a self-healing mechanism, that is, the reaction  $2\text{MnO}_2 \rightarrow \text{Mn}_2\text{O}_3 + \frac{1}{2}\text{O}_2$  takes place with the insulating Mn<sub>2</sub>O<sub>3</sub> covering the defect (an illustration of the self-healing mechanism is shown in Figure 1.52). However, when the temperatures involved are too high thermal runaway can occur.

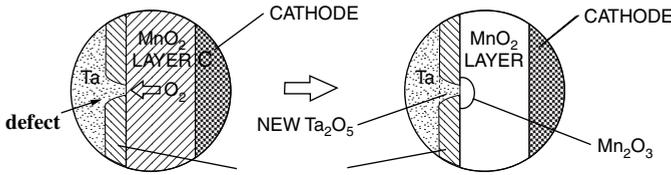


Figure 1.52 Self-healing mechanism of Ta capacitors.

2. *Thermal runaway:* With increasing volume efficiency more and more energy is stored at a constant volume, together with the increasing surface area and the presence of an oxygen source, that is  $\text{MnO}_2$  (see reaction above), a fatal combination is generated that can lead to catastrophic failures, that is, thermal runaway (explosion) of the devices. This problem is aggravated by the weaker links within the sinter body (reduced sinter temperature) causing a reduction of the thermal conductivity. Therefore, a critical amount of heat can accumulate at the defects generated by dislocation formation.

Both effects enhance each other, that is, the increased defect density due to the increased number of dislocations increases the chance for a fatal defect (thermal runaway). Moreover, the higher energy density leads to an increased thermal stress (heat accumulation) expediting the dislocation formation. Therefore, a vicious circle is created, as is illustrated in Figure 1.53. In the following both effects are described in more detail and several possible ways out of this vicious circle are presented. For completeness, a third problem, that is the increasing difficulty for impregnation of the finer and finer particles with a conductive counter electrode (e.g.  $\text{MnO}_2$ ) has to be mentioned here. This issue constitutes an important engineering problem but is only of minor scientific interest and will not be dealt with here.

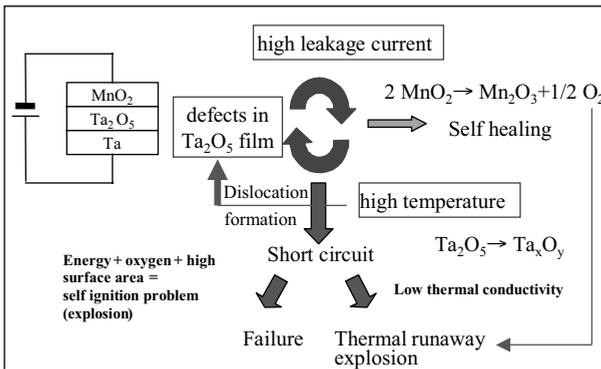


Figure 1.53 Thermal runaway vicious circle. Shrinking of TaMP leads to an increasing defect density due to a higher bulk oxygen concentration. The high associated leakage currents result in high temperatures, which induce further dislocations. Additionally, thermal runaway can occur due to the reduced thermal conductivity (lower sinter temperature leads to degradation of the interconnect structure, which reduces the thermal conductivity).

#### 1.3.4.4 Effect of Oxygen Content and Sinter Conditions on Dislocation Formation

The dielectric Ta<sub>2</sub>O<sub>5</sub> film thickness in the Ta capacitor typically varies between 30 and 300 nm depending on the formation voltage (ratio of rated- to formation-voltage is about 1:4). As a result of the low film thickness, the electrical field in the film at the rated voltage is about 10<sup>6</sup> V cm<sup>-1</sup>. To withstand the associated high electric fields for a long time the dielectric should have an *amorphous structure*. Amorphous dielectrics have a high density of electronic traps, that is, there is a continuum of localized states within the band gap, which now becomes a mobility gap. Owing to these traps, mobility of the charge carriers stays low in the high electrical field, preventing their accumulation and therefore reducing the chance of an electrical breakdown (electronic avalanche effects). *This is why the anodic Ta<sub>2</sub>O<sub>5</sub> film in a Ta capacitor is formed with conditions providing an amorphous structure. In fact, all successfully employed ultra-thin film dielectrics for electronic applications are amorphous (e.g. Si/SiO<sub>2</sub>).* Amorphous dielectrics are in principle not thermodynamically stable. They tend towards a spontaneous ordering and crystallization to reduce their internal energy. The crystallization process in amorphous Ta<sub>2</sub>O<sub>5</sub> film begins at nucleation sites located at the Ta/Ta<sub>2</sub>O<sub>5</sub> interface. These nucleation sites are related to defects on the Ta surface (impurity precipitates, crystalline grain boundaries, etc.) [248–251]. Growth of the crystalline inclusions induces mechanical stress in the amorphous matrix of the anodic oxide film and eventually causes damage to the dielectric. Figure 1.54 shows a crystalline ‘dislocation’ passing through the amorphous matrix of the Ta<sub>2</sub>O<sub>5</sub> film, resulting in its complete disruption (picture taken from Ref. [248]). Besides mechanical stress, the dislocations also act as a leakage path through the dielectric, which is one of the major reasons for catastrophic failures of Ta capacitors [252]. Consequently, the crystallization rate is a principal factor governing capacitor performance and reliability.

The bulk oxygen content in the Ta anode strongly affects this crystallization process in the dielectric oxide film [249, 250]. If the oxygen concentration in the bulk approaches the solubility limit (about 3.200 wt. ppm for Ta at room

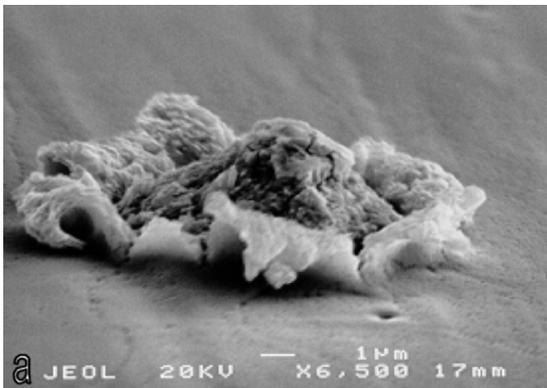
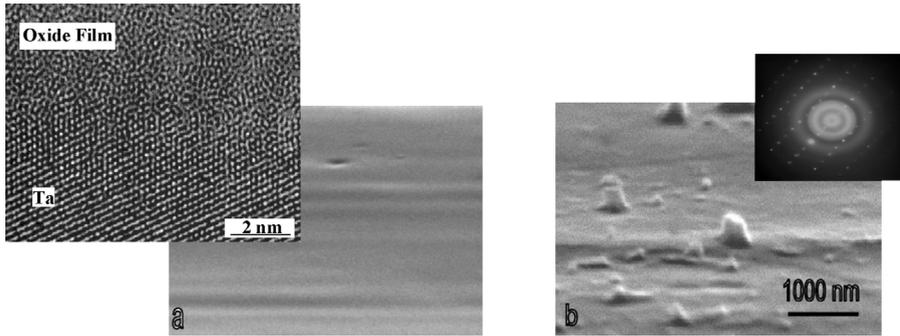


Figure 1.54 Dislocation in the Ta<sub>2</sub>O<sub>5</sub> matrix (source Ref. [248]).



**Figure 1.55** (a) Top view of the  $\text{Ta}_2\text{O}_5$  dielectric; (b) bottom view showing that the crystallization nuclei originate at the Ta/oxide interface. The inset in the left corner shows a high resolution TEM shot of the Ta/oxide interface without nuclei. The Ta shows a crystalline lattice whereas the  $\text{Ta}_2\text{O}_5$  is completely amorphous [248].

temperature), crystalline  $\text{Ta}_2\text{O}_5$  particles precipitate from the solid solution of oxygen in Ta. In the vicinity of the anode surface these crystalline particles serve as effective crystallization nuclei forcing crystallization of the anodic oxide film. As these crystalline dislocations serve as leakage paths in the dielectric film, an associated significant increase in the direct current leakage (DCL) is observed. Figure 1.55 shows the top (a) and bottom (b) of the anodic oxide film after formation of the crystalline nuclei. As one can see, the top surface of the film is smooth with some scattered pits or pores. The bottom of the  $\text{Ta}_2\text{O}_5$  film looks significantly different from the top. Peaks of various size and shape pass from the anode surface into the amorphous matrix. The diffraction pattern in the right corner of Figure 1.55b (TEM) shows that these peaks conform to the crystalline  $\text{Ta}_2\text{O}_5$  phase. This is the initial stage of the crystallization process. Both density and size of these nuclei increase gradually with increasing oxygen content in the anode and rise sharply when the oxygen content reaches the solubility limit. Regardless of the particle size, all Ta anodes exhibit the same behavior with respect to crystallization once they reach the critical oxygen content [255]. However, the smaller the particle size, the sooner this critical oxygen content is reached. This is simply due to the increasing surface to volume ratio of the smaller particles. Therefore, at a constant rate of oxygen diffusion from the native surface oxide into the bulk, higher oxygen concentrations build up in the smaller particles. The higher the bulk oxygen content, the greater is the rate of thermal oxide growth at elevated temperatures. Therefore, thicker thermal surface oxides are formed on smaller particles [256, 257]. This is because the oxygen atoms absorbed by the Ta surface cannot be dissolved into the Ta volume when it is already filled with oxygen. They stay on top of the surface building up a thick thermal oxide layer. The thickness of this thermal surface oxide prior to anodization plays an important role in crystallization. The reason for this is that at elevated temperatures micro-crystals can be formed in the thermal oxide, which serve as nuclei for a further crystallization in the subsequently formed anodic oxides.

**1.3.4.4.1 Impact of Sintering on Oxygen Concentration** For sintering temperatures  $>1750^{\circ}\text{C}$ , oxygen is evaporated out of the Ta anodes during the sintering process in vacuum. Additionally, most of other impurities, such as Fe, Ni and Cr, are also evaporated, providing a high purity of the final anodes. In this instance, crystallization of the anodic oxide film may only occur as a result of an eventual mis-processing. A few Ta capacitors, mostly for military applications, are still produced under such conditions. In contrast, at temperatures below this threshold temperature oxygen absorption by Ta takes place. The major source for the oxygen pick up during sintering is the native oxide on the top surface of the Ta particles [253], that is, heating in vacuum results in dissolving of the surface oxygen, which diffuses into the bulk of the Ta particles. As pointed out above, the finer the particles are (higher CV), the higher the absolute surface oxygen content, resulting in high oxygen contents of the sintered tantalum anodes. In fact, for very fine particles with a CV in excess of  $70\text{--}80\text{ k}\mu\text{F V g}^{-1}$ , the dissolving of the natural surface oxide into the bulk during powder sintering results in the bulk oxygen content already approaching the solubility limit. This is a major obstacle for capacitor manufacturers. For low voltages the anodic oxide film is thinner than in the high voltage regime, and therefore, it is less susceptible to crystallization. Several measures that can be taken to reduce the dislocation formation are considered next. These measures are of fundamental importance for the implementation of ultra-high CV powder into Ta capacitors. The results can also be transferred to other valve metal systems (e.g. Nb).

1. *Fixing the Oxygen Problem by Deoxidization after Sintering* To minimize the oxygen content in the Ta powder, a deoxidizing step using magnesium after sintering can be applied. As the magnesium–oxygen bonding energy is higher than that for tantalum–oxygen, the magnesium reacts with oxygen in the tantalum, forming magnesium oxide molecules, which in turn evaporate out of the powder [259]. However, this deoxidizing results in mechanically very weak junctions between the porous anode and the incorporated lead wire (the sintering between the lead wire and the anode body is triggered by the oxide). In [248] a new type of sintering was mentioned, which ultimately seems to fix this problem. No details were given on this very promising process (patent pending). By means of this new, so-called ‘Y-sintering’ (Yuri Freeman) process, the application of ultra-high CV powder seems to be possible.
2. *Prevention of Crystallization by Thermal Annealing after Anodizing* Random crystalline dislocations can begin to grow even in a completely amorphous matrix of the anodic oxide film. In this instance, crystallization can be minimized by a thermal annealing process subsequent to the anodizing process. The following physical model was suggested in Ref. [260] to explain this phenomenon. During thermal annealing the amorphous  $\text{Ta}_2\text{O}_5$  film undergoes high mechanical stress due to a large difference in the coefficient of thermal expansion between the Ta and  $\text{Ta}_2\text{O}_5$  phases ( $8 \times 10^{-7}$  and  $6.5 \times 10^{-5}\text{ K}^{-1}$ , respectively) [261]. These thermal stresses can relax by sliding (shear) of the  $\text{Ta}_2\text{O}_5$  film along the  $\text{Ta}_2\text{O}_5/\text{Ta}$  interface. Because the  $\text{Ta}_2\text{O}_5$  crystals are embedded into the Ta anode and sit inside the

Ta<sub>2</sub>O<sub>5</sub> film, this sliding will cause mechanical cutting of the crystals away from the metal surface. Loosing intimate contact with the metal surface undermines their further ability to grow. They are passively buried in the amorphous matrix of the anodic oxide film.

3. *Reduction of Thermal Budget after Anodizing* Heat has to be applied carefully as the opposite effect is also possible, that is, due to the increased film stress, nuclei, which were so far inactive, can be activated, initiating the growth of dislocations. Moreover, the activation energy for dislocation formation follows an Arrhenius law. Therefore, elevated temperatures can even induce dislocation formation. In this context, the conducting polymers should be mentioned. As will be pointed out below, conducting polymers have many advantages and can replace the MnO<sub>2</sub>. For impregnation with conducting polymers no pyrolysis is needed, therefore significantly reducing the thermal budget of the downstream process.
4. *Reduction of Crystallization by Purity Improvement* One root cause for crystallization even with a reduced oxygen content can be attributed to further impurities at the particle surface. The trivial fix for this would be an improvement in purity, which is actually difficult to achieve with the conventional K<sub>2</sub>-salt Na-reduction process described above (see p. 63). However, the second route, that is the Ta metal powder production by Mg reduction of the oxides, delivers purer metal powder grades (at least with respect to alkali elements). Therefore, this route may be superior for ultra-high CV powders. Moreover, higher purity is beneficial to achieve a higher BDV (break down voltage) as is known from E-beam melted powder.
5. *Reduction of Crystallization Rate by Adjustment of the Electrochemical Formation Conditions* As a last possibility for the reduction of dislocations in the amorphous oxide, the electrochemical formation conditions have to be mentioned. As was shown for the Ti/TiO<sub>2</sub> system in Figure 1.17, the formation conditions have a significant impact on the properties of the oxide films. The application of potentiostatic instead of potentiodynamic formation conditions allowed for a suppression of the texture dependence of oxide growth.

Moreover, from semiconductor manufacturing processes (e.g. the DRAM process as will be described later) it is known that doping of the film can also stabilize an amorphous matrix. Such a doping could potentially also be achieved electrochemically by a corresponding addition of the dopants to the electrolyte.

#### 1.3.4.5 Thermal Runaway

The root cause for the thermal runaway problem was identified to be due to the combination of high energy (high volume efficiency), large surface area and the presence of an oxygen source, that is the MnO<sub>2</sub> cathode. Initially the runaway is initiated by a defect in the dielectric layer causing high leakage and an associated temperature increase. Normally the defect is fixed inherently by the MnO<sub>2</sub> self-healing mechanism mentioned previously. When the defect density is too high, the self-healing fails and a permanent leakage path is generated leading to a short circuit in the component (device failure). This failure is fatal for the device and can destroy

the whole circuit (electrical malfunction). However, it is not catastrophic. For high CV powder, which has to be sintered at a relatively low temperature, the much more severe failure mode of thermal runaway occurs. In contrast to the normal short circuit failure mode described above, the heat now accumulates due to an insufficient thermal conductivity in the sinter body [weak sinter necks (bridges)]. As a result, the threshold temperature for ignition of the Ta powder is reached and a sudden, catastrophic ignition of the whole surface takes place, which is fed by the oxygen provided by the  $\text{MnO}_2$ . The device literally explodes constituting a severe safety problem for the surrounding environment. An incident such as this has to be prevented by any means. Therefore, expensive and time-consuming 'burn in' tests are necessary in order to make sure that poor devices are screened out before they are sold. This significantly reduces the process yield. It also prevents larger capacitor case sizes from being produced with high-CV powder (the energy content increases with increasing case size). Thus, fixing the thermal runaway problem is of paramount importance. In the following, several measures that can be taken to reduce the thermal runaway issue are presented. This includes one ultimate solution to the problem, namely the use of conductive polymers as a replacement of the  $\text{MnO}_2$  counter electrode that acts as the oxygen source.

**1.3.4.5.1 Reduction of Defects** Firstly, the defects in the dielectric film are responsible for the occurrence of a leakage path leading to a temperature increase. Therefore, reduction of defect number will reduce the chance for a thermal runaway significantly. For this, the exact measures already explained above can be taken (e.g. higher purity, adjusted formation conditions and doping). However, these measures can not eliminate the thermal runaway completely as some defects will always remain.

**1.3.4.5.2 Improvement of Thermal Conductivity of the Anode Sinter Body** For the initiation of a thermal runaway the threshold temperature  $T_{\text{crit}}$  for Ta powder ignition must be exceeded.  $T_{\text{crit}}$  itself is a function of the surface area, that is the larger the surface area the lower  $T_{\text{crit}}$  will be. In order to reach  $T_{\text{crit}}$  a minimum energy  $E_{\text{crit}}$  is required, which is of the order of some mJ for a  $50 \text{ k}\mu \text{ FVg}^{-1}$  Ta powder. Whether this critical energy can be accumulated depends on two major factors:

1. *The total energy stored in the device.* Therefore, the case size is critical. The larger the device, the more energy it contains. As an aside, the energy content also depends on the powder morphology: the larger the surface area the more energy can be stored per unit volume.
2. *Thermal conductivity of the sintered body.* If the thermal conductivity is high enough the critical temperature can not be reached locally but the energy is dissipated over the whole volume of the device.

The first factor leads to a simple measure, that is the use of smaller and smaller case sizes with increasing CV of the powder. It is fairly clear that this measure is not desirable as it strongly limits the design capabilities for capacitor devices. The second factor, that is improvement of the thermal conductivity, is much more interesting as

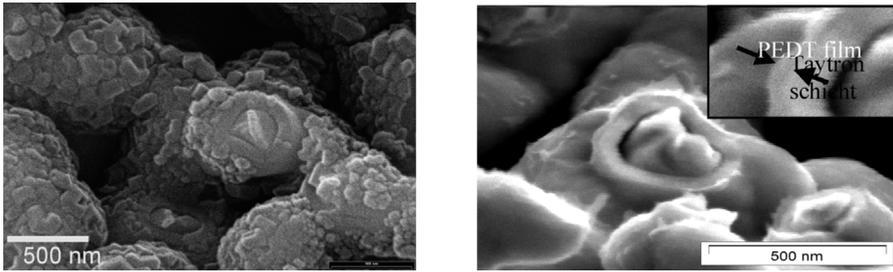
in principle it allows for a fundamental solution to the problem. However, it has to be kept in mind that the processing of increasingly finer powders requires the sinter temperature to be decreased in order to preserve the powder morphology (the high surface). Consequently, the interconnections between the particles become weaker. This even tends to reduce the thermal conductivity. Moreover, as worse comes to worst, the energy density also increases with increasing CV product. Therefore, both parameters aggravate the thermal runaway problem under standard conditions. Nevertheless, two promising approaches to improving the thermal conductivity of the sinter body are discussed below:

1. *Improvement of the green body uniformity* by using optimized binders. Owing to the range in the particle size distribution, the contact within and between the agglomerates can vary, that is there are density fluctuations within the green body that are transferred into the final sinter body (accumulation of fines). The thermal conductivity in low density areas is especially poor and thermal runaway is therefore likely to originate in such weak spots. These density fluctuations can be suppressed by using optimized binders (organic compounds), which provide for a uniform distribution of fines throughout the sinter body.
2. *Addition of a sinter aid* that strengthens the sinter bridges between the particles. These sinter bridges are the weakest part in the sinter body and therefore determine the thermal conductivity. An improvement of the sinter bridges can be accomplished by adding even finer particles to the mix, which fit into the spaces in between the particles.

**1.3.4.5.3 Conductive Polymers as the Cathode Material** The thermal runaway can ultimately be prevented by replacing the  $\text{MnO}_2$  cathode with conductive polymers (CP). This eliminates the oxygen source, which is essential to feed the reaction. Various conducting polymers are considered for application as a cathode material. Among them, polyaniline (PANI) and polypyrrole (PPY) were the first to attract interest. However, the long time and temperature stability of these polymers are significantly worse than the ones for a newer conducting polymer *poly-3,4-ethylene-dioxythiophene* (PEDT, tradename BAYTRON). For the application of PEDT two different process schemes are possible:

1. *Single step dipping* with a mixture of EDT (Baytron M)/polymerizer/organic solvent. Iron(III) *p*-toluene sulfonate (tradename Baytron C) can be used as the polymerizer.
2. *Multiple step process* with successive dipping of the anode into the EDT (Baytron M) and polymerizer (Baytron C) solution with intermediate drying steps.

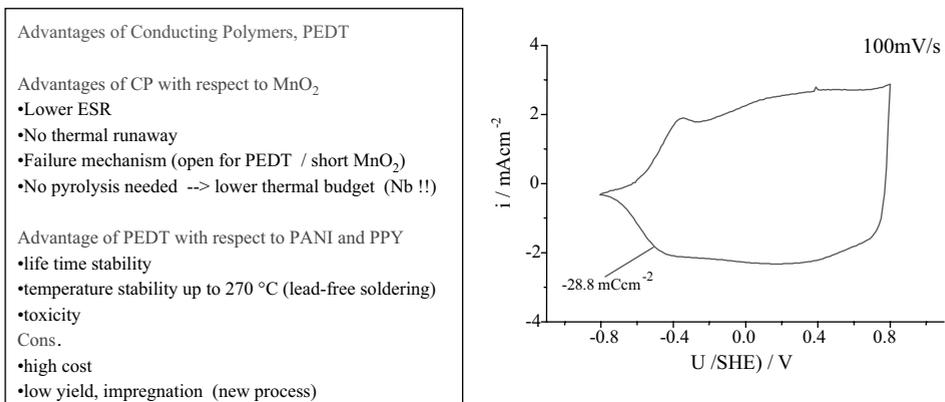
Both processes have their advantages and disadvantages with respect to the process yield (e.g. different pot life). Further fine tuning of the processes is required to identify the optimum sequence. In Figure 1.56 a direct comparison of a Ta anode impregnated with  $\text{MnO}_2$  and one impregnated with PEDT is shown. The thickness of the PEDT film is about 20 nm. Besides suppression of thermal runaway, the major advantage of CP is its better conductivity with respect to  $\text{MnO}_2$ . This significantly



**Figure 1.56** Left: Ta anode with  $\text{MnO}_2$  cathode; Right: PEDT cathode [262].

reduces the ESR and therefore improves the performance of the capacitors. However, the cost of the CPs is much higher than that for  $\text{MnO}_2$  and the integration process is less established, that is the yield is still low. Therefore, currently this new technology is only applied where an excellent ESR is needed and/or the thermal runaway problem is inherent. In the future the CPs that also can be applied to Al capacitors will significantly gain importance. Advantages and disadvantages of CPs are summarized in Figure 1.57 along with a cyclic voltammogram of a PEDT electrode. As is typical for most CPs the polymer is p-type semiconducting in the oxidized and insulating in the reduced state. PEDT shows an excellent reversibility with an almost rectangular profile over a potential range of 1.4 V. This is very similar to the corresponding voltammogram of  $\text{RuO}_2$  that was shown in Figure 1.48, therefore indicating another capacitor related application of PEDT, namely as a supercapacitor material.

**1.3.4.5.4 Alternative or Modified Anode Materials** In order to prevent or minimize thermal runaway, modified anode materials can also be considered. The minimum energy for a dust ignition in the case of pure Ta or Nb powder is below 3 mJ. Nitration of Ta and Nb (e.g.  $\text{Ta}_2\text{N}$  and  $\text{Ta}_2\text{N}_3$ ) increases the ignition energy to >10 J. Consequently, these materials are also less likely to be prone to ignition in solid capacitors. These



**Figure 1.57** Advantages and disadvantages of CPs, and a cyclic voltammogram of PEDT in aqueous solution.

nitrides are still metallic conductors, which can be anodized to form a good dielectric oxide layer. However, the dielectric constant of the corresponding oxides is significantly smaller by about a factor of two, reducing the possible capacitance volume efficiency. Even more severe are the changes in the mechanical properties of these materials. Nitrides are conventionally used for abrasive-proof tools. They are exceptionally hard, which results in severe handling problems of the powder. It is therefore difficult to form a green body without destroying the tools that are used for pressing. Moreover, the sinter activity of the nitrides is poor, resulting in the need for a high sinter temperature in excess of 1600 °C. This in turn further reduces the remaining CV efficiency. Therefore, currently no promising route for the production of a high CV nitrided powder exists. For Nb a more promising modification, namely the suboxide NbO, exists. NbO is a good metallic conductor, which is just a little harder than pure Nb. Therefore, handling of this powder is easier than for the nitrides. This material is currently been investigated together with Nb as a potential complement material for supplementation of both Ta and Al capacitors.

In the next section another important oxide system for electronic applications, namely the Si/SiO<sub>2</sub> system, will be discussed.

#### 1.4 Si/SiO<sub>2</sub> System

Without any exaggeration, Si/SiO<sub>2</sub> can be considered by far to be the most important system in electronics. This is true from a technological as well as from a scientific point of view. For no other system are so many publications available. Since the invention of the transistor in 1947 by Bardeen and Brattain [264] and Shockley [265], there has been a tremendous growth in semiconductor microelectronics. According to recent reports, Si still makes up about 98% of the world market share in microelectronics, with Ge, GaAs, InP, etc. covering the remaining 2%. (This does not include passive components as discussed in the previous sections.) However, the question is: why Si? Si is one of the most abundant elements, which can therefore be produced at low cost and the technology to grow large (currently 300 mm diameter) single crystals is well established. However, as shown in Table 1.4, the intrinsic carrier

**Table 1.4** Selected properties of common semiconductors.

Properties	Si	Ge	GaAs	InP
Energy gap	1.1 (indir.)	0.7 (direct)	1.4 (direct)	1.4 (direct)
Density of states (cm <sup>-3</sup> )				
Conduction band	3 · 10 <sup>19</sup>	1 · 10 <sup>19</sup>	5 · 10 <sup>17</sup>	
Valence band	1 · 10 <sup>19</sup>	6 · 10 <sup>18</sup>	7 · 10 <sup>18</sup>	
Intrinsic carrier mobility at 300 K (cm <sup>2</sup> V <sup>-1</sup> )				
Electrons	1500	3800	8500	4000
Holes	450	1800	400	150

mobility of Si is lower than for all the other important semiconductors. Consequently, in terms of carrier mobilities, Si is inferior to the others, resulting in a lower signal speed of the corresponding devices. In addition, Si is an indirect semiconductor, which limits its use for optical applications. Therefore, performance wise Si seems not to be the optimum choice. However, there is one crucial advantage of Si that comes into play when the passivated Si surface, that is the Si/SiO<sub>2</sub> interface, is considered. Passivation of the Si surface significantly improves the electrical characteristics of the Si device. This is due to the fact that at the termination of any crystalline lattice, there are non-saturated chemical bonds. For Si, there are about  $10^{15} \text{ cm}^{-2}$  of these 'dangling bonds' at the surface, which is in the order of the number of surface atoms. These dangling bonds give rise to energy states within the band gap. According to Deal [266] these defects are termed the interface trapped charge,  $Q_{it}$  ( $\text{C cm}^{-2}$ ), and are often reported as the interface trap density  $D_{it}$  (number  $\text{cm}^{-2} \text{ eV}^{-1}$ ). These states can affect and even prevent electronic conduction because under device operation, the electrons that are flowing in response to an external electric field will exchange charge with the surface states instead of exchanging charge with the conduction and valence bands of Si. This disastrous effect is termed *Fermi level pinning* as the Fermi level of the semiconductor cannot move in response to the applied electric field but the charge carriers are trapped in these interface energy states.

The passivation of the Si surface results in formation of an *amorphous SiO<sub>2</sub>* film, tying up the dangling bonds and reducing their number by the enormous amount of up to five orders of magnitude to about  $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ . No other semiconductor with a surface film has been able to achieve electronic surface passivation to the same extent that Si can with SiO<sub>2</sub>. This is the main reason why the Si/SiO<sub>2</sub> system dominates in microelectronics, that is Si and SiO<sub>2</sub> are the 'ideal couple' with SiO<sub>2</sub> being an excellent dielectric film, as will be pointed out below.

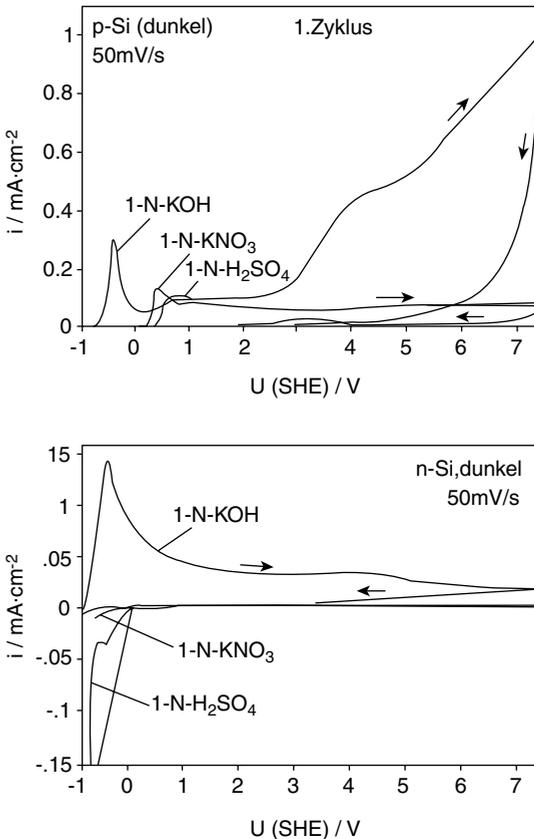
The passivation can be achieved in several manners. The most frequently used one is a thermal passivation [33–36], by the simple exposure of the Si surface to an O<sub>2</sub> ambience at elevated temperature. In contrast, an electrochemical passivation can be performed at room temperature, which is beneficial when a low thermal budget is desired. Both the thermal and the electrochemical treatment result in a consumption of Si from the surface, that is the SiO<sub>2</sub> grows into the surface (about 1/3). This can be critical for very large scale integration (VLSI) structures. If consumption of Si is not acceptable, a deposition of SiO<sub>2</sub> by chemical or physical vapor deposition (PVD/CVD) techniques is necessary.

A good overview on the various passivation and deposition processes can be found in Refs. [267–269]. In Table 1.5 the resulting  $D_{it}$  trap densities for the various possible passivation techniques are shown. Thermal passivation yields the highest interface quality, that is the lowest  $D_{it}$  can be achieved. Quality wise the electrochemical passivation is next. However, electrochemical reactions at a semiconductor surface are only possible in the accumulation mode. Therefore, anodic reactions only take place at p-type doped Si electrodes (accumulation of majority charge carriers, i.e. holes), whereas on n-Si only reduction reactions are possible. Consequently, only p-type doped Si can be anodically passivated. This can be changed by an illumination

**Table 1.5** Comparison of surface states  $D_{it}$  for various  $\text{SiO}_2$  preparation techniques.

$\text{SiO}_2$ formation	Approximate number of surface states $D_{it}$ ( $\text{cm}^{-2}$ )
Thermal oxidation	$10^{10}$
Anodic oxidation of p-Si	$10^{10}$ – $10^{11}$
CVD	$10^{10}$ – $10^{12}$
PVD	$10^{10}$ – $10^{13}$
No $\text{SiO}_2$ on Si	$10^{15}$

of the surface with photon energies above the band gap (1.1 eV for Si). Illumination generates a minority carrier even in the depletion mode (holes accumulate at the surface), that is under illumination n-type Si basically behaves as p-type Si and can be anodically oxidized. The corresponding formation cyclic voltammograms are shown in Figure 1.58 (from Ref. [32]).



**Figure 1.58** Anodic passivation of p-Si and n-Si in different electrolytes without illumination. In KOH corrosion takes place,  $50 \text{ mV s}^{-1}$  (source Ref. [32]).

Regarding oxide formation, this behavior relates to that of the valve metals treated earlier. Analogous to the valve metal oxides in the previous sections we now focus on the use of SiO<sub>2</sub> as a dielectric film for capacitors. In contrast to the prior sections, it is not the passive components but integrated circuits (IC) that are considered. There are two main applications of functional dielectrics in microelectronics, namely for MOSFET gate insulation and for storage capacitor nodes. Besides these applications, SiO<sub>2</sub> is used for many more purposes in integrated circuits, such as an ILD (inter layer dielectric between metal lines of a chip), STI (shallow trench isolation) fill, or LOCOS (local oxidation of silicon) isolation between active areas (also called field oxides), and for sacrificial hard-masks in lithography [267–269].

#### 1.4.1

### Application of the Si/SiO<sub>2</sub> System

#### 1.4.1.1 Si/SiO<sub>2</sub> in MOSFETs

In the same way that Si is at the heart of microelectronics, the metal oxide semiconductor field effect transistor, or MOSFET, is at the core of most IC devices. The MOSFET is a four-terminal device, which includes a metal gate electrode, heavily doped source and drain regions and a substrate electrode. The metal and Si substrate are separated by a dielectric, such as SiO<sub>2</sub>. For an n-channel or N-MOSFET, current conduction is via electron flow and not hole conduction. The N-MOSFET devices are fabricated on p-Si substrates and the source and drain regions are heavily doped (low resistance) with an n-type material, such as arsenic or phosphorus. When a negative voltage is applied to the metal gate electrode, the majority carriers, or holes, respond to the applied electric field and accumulate at the Si/SiO<sub>2</sub> interface. Consequently, the transistor is in the ‘off’ state, as current cannot flow from source to drain. Conversely, when a positive bias is applied to the metal gate, the minority carriers or electrons invert the Si/SiO<sub>2</sub> interface, generating a conducting channel between source and drain. The device is switched on. In Figure 1.59 a C-MOSFET, or complementary-MOSFET structure is shown for illustration. The CMOS design consists of consecutive MOSFETs of different polarities (N-MOSFET and P-MOSFET), which are integrated in series on one chip. This design minimizes leakage paths due to consecutive pn-junctions in reverse bias, resulting in low power consumption and high speed [272].

The requirements for higher density integrated circuits and faster switching and communication between the devices on a circuit have driven the microelectronics industry to *scaling*, which means a miniaturization of devices. The definition of scaling is: to reduce all parts of a device without affecting the electrical characteristics of the device. In current ULSI (ultra-large scale integration), a minimum lateral feature size well below 100 nm is targeted. Microelectronics have already therefore entered the realms of ‘*nanotechnology*’. The minimum feature size is defined by the gate length  $L$  (distance between source and drain, i.e. channel length) of the MOSFET. In order to keep the electrical MOSFET characteristic, that is the switching behavior, unchanged with shrinking device length, the capacitance of the MOS structure has to be kept constant. The MOS capacitor is part of the MOSFET structure consisting of

Note: Gate and source/drain contact metal not shown

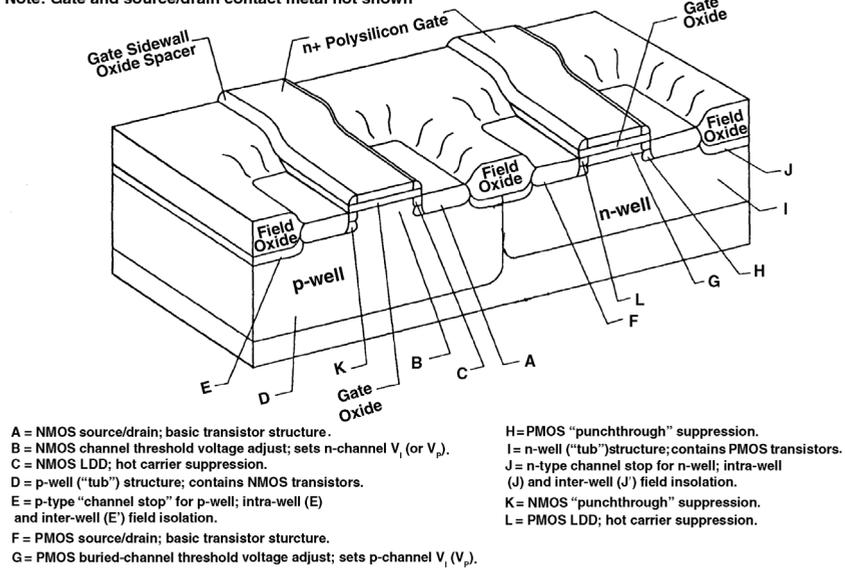


Figure 1.59 Schematic diagram of a C-MOSFET device.

the Si/SiO<sub>2</sub>/gate metal structure. The switching behavior of the MOSFET is described by the threshold voltage  $V_T$ . This is the minimum voltage that has to be applied to the gate in order to generate the conducting channel (ON-position of the MOSFET). The voltage  $V_G$  that is applied to the gate is distributed into two parts, the potential drop in the oxide  $\phi_{ox}$  and that in the Si (surface potential  $\phi_s$  due to the charge in the scl of the Si):

$$V_G = \phi_{ox} + \phi_s \quad (1.38)$$

The potential drop  $\phi_{ox}$  can be expressed by the capacitance of the MOS capacitor  $C_{ox}$  as:

$$\phi_{ox} = Q_C / C_{ox} = eN_A d_{scl} / C_{ox} \quad (1.39)$$

where  $Q_C$  is the charge on the gate. From the definition:

$$C_{ox} = \epsilon_0 \epsilon_{ox} / t_{ox} \quad (1.40)$$

Note that here  $C_{ox}$  is given in units of  $F\text{cm}^{-2}$  (capacitance density),  $t_{ox} = d_f$  (film thickness) of the oxide. Together with Equation 1.9 for the extension of the space charge layer, we get an expression for  $\phi_{ox}$  in terms of the charge  $N_A$  in the scl:

$$\phi_{ox} = \frac{1}{C_{ox}} \sqrt{2eN_A \epsilon \epsilon_{ox} (V_{GB} + 2V_F)} \quad (1.41)$$

where  $V_F$  is the Fermi potential.

The threshold potential  $V_T$  is defined as the point where inversion starts. For this point it is  $\phi_s = 2V_F$ , because the inverted surface has to have the same concentration of minority carriers as the concentration of the majority carriers had before

(when  $V_{GB} = 0$ ). In other words, the Fermi level now has to have the same distance from the valence band as the distance to the conduction band was before (vice versa for a p-type semiconductor). Therefore, for the threshold voltage we end up with the expression:

$$V_T = 2V_F + \frac{1}{C_{ox}} \sqrt{2eN_A \epsilon \epsilon_{ox} (V_{GB} + 2V_F)} \quad (1.42)$$

According to this equation the switching behavior of a MOSFET depends critically on the capacitance of the MOS-capacitor structure involved. For example, a decreasing  $C_{ox}$  would result in an increasing threshold voltage. Conversely, the clear tendency in microelectronics is to decrease  $V_T$  in order to reduce power consumption (less leakage at lower applied potentials). In order to keep  $C_{ox}$  constant with shrinking device dimensions (shrinking capacitor area) the SiO<sub>2</sub> film has to be made thinner. The scaling of the oxide film is one of the most critical issues facing the microelectronics industry. For the currently developed ULSI devices with gate lengths below 100 nm, an SiO<sub>2</sub> gate oxide thickness below 3.5 nm is necessary. At these dimensions the Si/SiO<sub>2</sub> interface region becomes a significant portion of the device dimensions. Interface properties such as interface roughness, charges at the interface (such as  $D_{it}$ ), interfacial stress and tunneling will all affect device performance and reliability. In particular, tunneling is a principal problem, that is, independent of the interface quality, Fowler–Nordheim (FN) and direct tunneling start to dominate the leakage currents [269–271]. For an oxide voltage  $\phi_{ox}$  below 3.2 V, the electron tunneling barrier changes from being triangular to trapezoidal (see Figure 1.60). Oxide tunneling then completely switches from FN to direct tunneling.

Logic CMOS technology may be able to tolerate the higher leakage currents due to the direct tunneling, but DRAM will not be able to tolerate them if  $t_{ox} < 3.5$  nm. Consequently, the Si/SiO<sub>2</sub> system approaches its limits [273–275] and new solutions that allow for a further scaling of devices have to be found. One approach would be the use of a material with a higher dielectric constant such as the valve metal oxides mentioned previously. This would allow the gate-capacitance of the MOSFET to be increased without reaching the tunnel region for the gate oxide thickness. Another

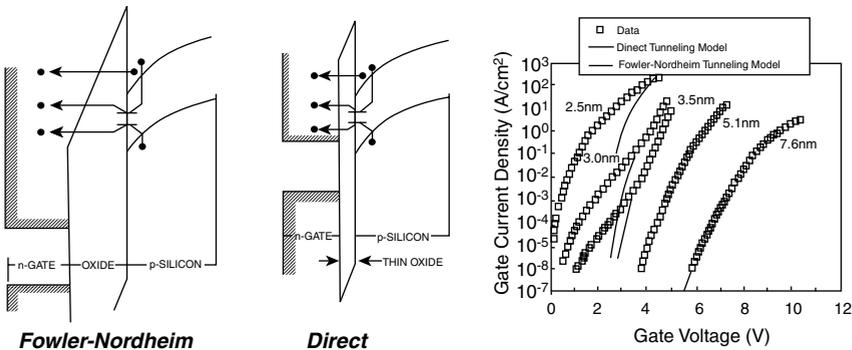


Figure 1.60 Comparison of FN and direct tunneling for shrinking gate oxide thicknesses.

approach is the use of a completely new design for the MOSFET structure. At present the MOSFET is printed laterally on top of the wafer surface. Alternatively, the MOSFET could be buried vertically into trenches that are dug in the wafer surface. This requires less space and therefore allows for higher densely packed structures without the need to shorten the gate length, and in turn allows the gate oxide thickness to be maintained. This option therefore allows keeping  $\text{SiO}_2$  as the gate dielectric material. New results on both options are presented below. However, firstly, another important capacitor structure on integrated circuits, namely the storage capacitor on DRAMs (dynamic random access memories), is introduced.

#### 1.4.1.2 Si/SiO<sub>2</sub> in DRAMs

DRAM is one of microelectronics industry's highest volume parts. Because of its emphasis on high density, low cost and longer retention times, the DRAM is ideal for setting a roadmap on minimum feature size, defect density and material quality. DRAM, therefore, can be considered the most important technology and research driver in electronics. It is thus ideally suited for deeper investigation into the details of current scientific issues regarding the use of dielectric materials, such as Si/SiO<sub>2</sub> and the valve metal oxides in electronics.

Random access memory, RAM, constitutes most semiconductor memory. Owing to its array type of structure, it allows any part of the memory to be read or written as fast as any other part. Conversely, serial access memories such as hard disks, floppy disks, magnetic tape, core memory or optical media (CD, DVD) can be very slow depending on the bit location that is being processed. The basic RAM storage element is the cell, which is duplicated once for every bit to achieve an array structure (two-dimensional lattices). Each cell can store one bit of information, '1' or '0'. Semiconductor RAMs can be categorized into roughly three groups: nonvolatile (NVRAM), static (SRAM) and dynamic (DRAM), each of which has several variants. All three types are typically used together. NVRAM is used for permanent storage of information that can be accessed in an ROM (read only memory) mode (e.g. BIOS chips for initialization of a computer). An SRAM cell stores data in a flipflop, consisting of several MOSFETs. It retains its information as long as power is applied to the cell, but loses it when power is removed. A DRAM cell is the smallest possible cell consisting of one MOSFET (access transistor) and one storage capacitor only (see Figure 1.61). The capacitor stores charge, which represents the bit, and the MOSFET transfers the

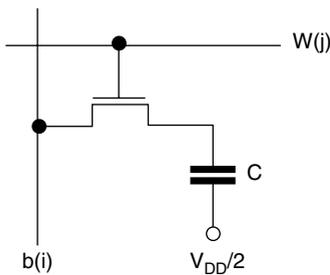
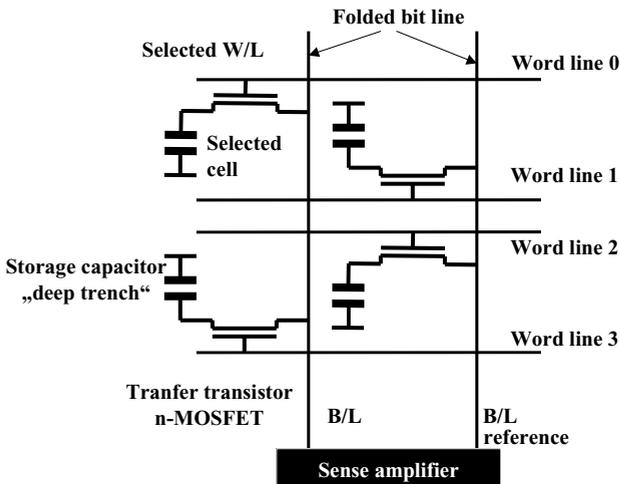


Figure 1.61 DRAM cell.

bit (charge) from and to the capacitor. Because the readout is destructive, the cell must be refreshed by immediately following every read operation with a write-back operation that re-writes the data which were just read. ‘Dynamic’ means that the cell must also be refreshed periodically, otherwise the cell would lose its information due to cell leakage. DRAMs are therefore optimized for low leakage currents. They are not optimized for speed as, for example, are the SRAMs. Owing to the more complicated cell structure the SRAMs are more expensive (one SRAM cell occupies 8–16 times more space than a DRAM cell) and are therefore used where speed is important, and DRAMs are used where cost efficient storage of large amounts of data is required. A faster DRAM or cheaper SRAM could eliminate the need to use both parts in one system [276] (mutual substitution).

**1.4.1.2.1 DRAM Operation** A DRAM cell consists of a storage capacitor and a transfer transistor (n-MOSFET) that acts as a switch. The presence of charge in the storage capacitor indicates a logical ‘1’ and its absence a logical ‘0’. Cells are arranged in arrays of rows (word line  $w_j$  or W/L) and columns (bit line  $b_j$  or B/L) that are orthogonal to each other. Multiple sub-arrays replace a single large array to shorten the word and bit lines and thereby reduce the time to access a cell. For example, a 256 Mbit array typically consists of  $16 \times 16$  Mbit sub-arrays. Word lines control the gate of the transfer transistor and the bit lines are connected to sense amplifiers. Adjacent bit line pairs can be considered as folded in the middle, broken and connected to a shared sense amplifier (folded bit-line design). Alternatively, amplifiers can be placed between two sub-arrays, thus connecting each sense amplifier to one bit-line in each array. This open bit-line design leads to more compact designs but offers less noise immunity than folded bit lines. When a word line is selected, all transfer transistors connected to that word-line are turned on and charge transfer occurs between the storage capacitors and the bit-lines crossing the word-line. In Figure 1.62



**Figure 1.62** DRAM folded bit-line layout and illustration of its operation.

one example is shown. Before a read operation, B/L and B/L are shortened and all bit-line pairs are pre-charged to a voltage  $V_b$ , halfway between the internal power supply voltage  $V_{DD}$  and ground. To read the cell the selected word line (W/L in this example) is raised to  $V_{DD}$  turning on all transfer transistors on that word-line. This does not affect any transistors on the other word lines. Each sense amplifier detects the polarity of charge transfer by measuring the voltage difference,  $\Delta V_b$ , between B/L and the reference B/L, and thus determines whether the cell stored a logic '1' or '0'. The signal is very small (100–200 mV) because when the transistor turns on, charge redistributes between the small storage capacitor and the capacitance of the bit-line. The latter can be more than ten-times higher due to the large number of devices connected to it and other stray capacitances. The magnitude of the bit-line signal  $\Delta V_b$  therefore depends on the ratio of the storage capacitance to the bit line capacitance, that is:

$$\Delta V_b = \frac{V_{DD}}{2} \frac{1}{1 + \frac{C_b}{C_s}} \quad (1.43)$$

where  $\Delta V_{DD}$  = internal power supply voltage,  $C_b$  = bit-line capacitance and  $C_s$  = storage node capacitance. As  $\Delta V_{DD}$  and  $C_b$  are reduced by about the same factor,  $C_s$  must be kept above a critical level, typically 30–40 fF. The stored charge decays away quickly because of the inherent leakage of the cell. The cell retention time typically ranges from ms to some 100 ms. A periodic refresh is therefore necessary to restore the charge before its level drops below a critical value where a '1' is indistinguishable from a '0'. An SEM micrograph of the word- and bit-lines of a DRAM cell (0.25  $\mu\text{m}$  pitch) is shown in Figure 1.63.

#### 1.4.1.3 DRAM Storage Capacitor (Deep Trench)

The construction of a DRAM cell in 'deep trench' (DT) technology is shown in Figure 1.64. The top shows schemes and the bottom of the figure shows the corresponding SEM micrographs of the DRAM cell. The storage capacitor is connected to an access n-MOSFET by the BuriEd STrap, therefore this layout is known as the 'BEST'-cell. When the MOSFET is turned on by applying a voltage to the gate, charge can flow from the source of the MOSFET to the drain that is connected to

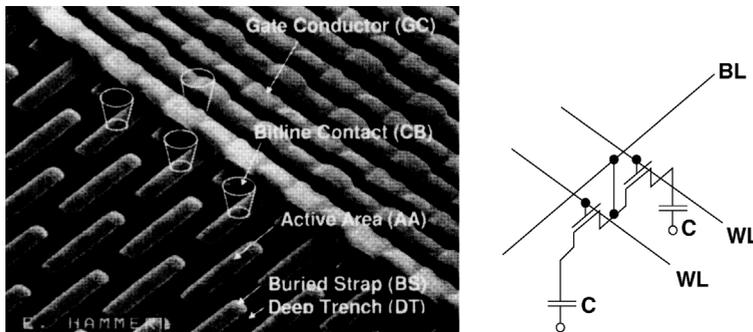


Figure 1.63 SEM and schematic representation of the DRAM word- and bit-line configuration.



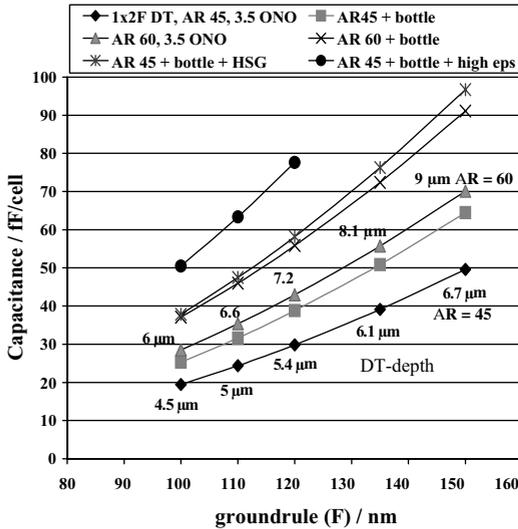
at the top portion of the DT. This thick oxide collar prevents the vertical transistor structure (see Figure 1.64) from turning on, which otherwise would result in a high vertical leakage (this vertical device is an undesired but unavoidable npn-transistor structure). Subsequently, the trench is filled with a conducting material such as highly doped Si and the buried strap is formed.

Note that there are always two DTs very close to each other. These DTs have to be isolated from each other by an STI (shallow trench isolation) process. There is also a ‘passing word-line’ right on top of the DT, which connects to a gate of a DT pair that is one plane deeper in the structure. A portion of the STI therefore also covers the top of the DT to generate insulation from this word-line conductor. The two DTs that are farther apart are connected by one active area containing two MOSFET structures, which share one bit-line contact (folded bit-line layout). In Figure 1.64 a cell of  $0.25\ \mu\text{m}$  feature size  $F$  is shown, that is, the channel length of the MOSFET access transistor is about that size as is the lateral top dimension of the DT. The depth of the DT is about  $6\ \mu\text{m}$  yielding an aspect ratio of 24 in this instance.

As already mentioned above, the minimum lateral feature size of future gigabit DRAM generations has to be shrunk well below  $0.1\ \mu\text{m}$  to keep pace with productivity demands. However, the bit storage capacitance does not scale but has to be kept constant or even increased to compensate for higher charge leakage if reduced dielectric layer thickness or new node materials are applied. A storage capacitance of up to  $40\ \text{fF}$  per cell will be necessary for future DRAM generations. Future DRAMs can only meet this target when several new measures are taken. With conventional materials and new processes a minimum feature size  $F$  of  $0.10\ \mu\text{m}$  in the best case can be achieved.

For even smaller feature sizes high  $\epsilon_r$  materials for the storage capacitor dielectric become essential. Figure 1.65 shows the calculated capacitance per cell as a function of  $F$  for a DT with  $1F$  by  $2F$  lateral top-down dimensions. These dimensions are typical for current  $8F^2$  and  $6F^2$  array layouts (one DRAM cell laterally covers a space of  $\times F^2$ ). For the calculations, an oxy-nitride (ONO) dielectric layer with an oxide ( $\text{SiO}_2$ ) equivalent thickness  $t_{\text{eq}}$  of  $3.5\ \text{nm}$  ( $\epsilon = 3.8$ ) was assumed. The process for formation of such an ONO film is described below. The depth of the vertical trench top isolation oxide (DT-collar) that reduces the active capacitor area was assumed to be  $1.3\ \mu\text{m}$ . Six different possibilities (curves) to achieve a capacitance increase are specified in Figure 1.65. These possibilities are discussed in some detail below.  $\text{TiO}_2$  and  $\text{Ta}_2\text{O}_5$  are considered as the high  $\epsilon_r$  node materials.

**1.4.1.3.1 Increase of Aspect Ratio for DT Si Etch up to 60** The maximum achievable DT depth is not limited by an Si Reactive Ion Etch (RIE) stop, but by hard mask erosion [277–279]. A boron doped silicon oxide (BSG) is used as the hard mask material (CVD deposition). The BSG is patterned by conventional photoresist technology. A photoresist to BSG RIE selectivity of above 4:1 is possible. In turn, the BSG hard mask to Si RIE selectivity was found to depend on the DT top dimension (lateral DT perimeter). The corresponding experimental relationship is shown in Figure 1.66 for a conventional Si RIE tool set. For each data point the required BSG

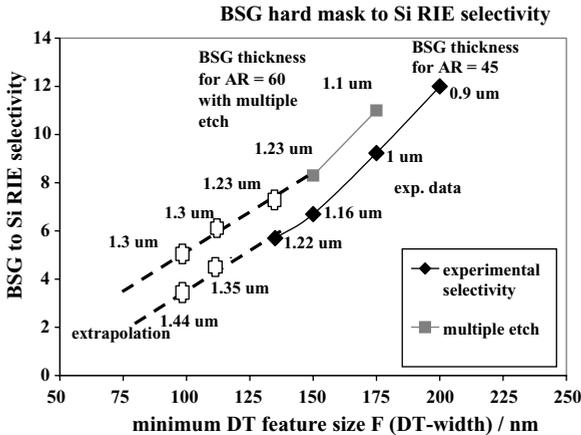


**Figure 1.65** DT capacitance roadmap. The six curves represent different options: 1, Si-etch with an aspect ratio (AR) of 45, straight DT profile; 2, AR = 45 + bottle shape DT profile; 3, AR = 60; 4, AR = 60 + bottle; 5, AR = 45 + bottle + HSG (hemispherical silicon grains); 6, AR = 45 + bottle + high  $\epsilon$  dielectric materials such as TiO<sub>2</sub>, Ta<sub>2</sub>O<sub>5</sub> and Al<sub>2</sub>O<sub>3</sub>.

layer thickness is given, assuming a DT Si RIE aspect ratio of 45 and a required remaining BSG thickness of 150 nm after Si RIE (process window).

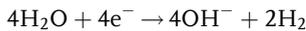
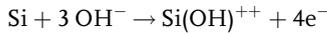
Figure 1.67 shows, as an example, cross-sections of DT structures with 6  $\mu\text{m}$  depth and a trench width of 0.135  $\mu\text{m}$  (AR = 45). For this a 1.2  $\mu\text{m}$  thick BSG hard mask stack was used, which is well below the capabilities of current tool sets. In order to ensure a clean DT profile a sidewall passivation layer has to be formed during Si RIE, requiring a well controlled ratio between etchant (e.g. HBr) and passivating (O<sub>2</sub>) gases. We found the passive layer formation to be vertically inhomogeneous with thicker films formed in the upper DT portion. This results in a decreasing trench open area with increasing etch time (DT clogging) reducing the BSG to Si etch selectivity and the differential etch rate. Therefore, a multiple step RIE process (see patent Ref. [280]) was applied with an integrated removal of the passivation layer at certain times. With this scheme the differential etch rate and RIE selectivity were significantly enhanced. The corresponding data are also shown in Figure 1.68. An AR of up to 60 could be achieved. Figure 1.67 (right) shows a corresponding cross-section with 8.6  $\mu\text{m}$  DT depth and 0.15  $\mu\text{m}$  width. As the DT profile is less controlled for this process, post-engineering of the DT-sidewall profile is needed. For this, an inexpensive wet-clean is applied, as is explained next.

**1.4.1.3.2 Bottle-shaped DT** For well controlled engineering of the lateral DT profile a new wet etch process employing diluted NH<sub>4</sub>OH chemistry was developed

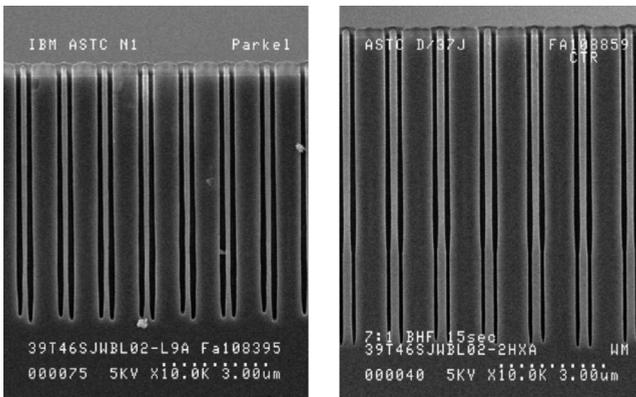


**Figure 1.66** Measured hard mask (BSG) to DT Si RIE selectivity as a function of feature size for different etch processes (single and multiple etch). The hard mask thickness required to achieve a DT aspect ratio (AR) of 45 (single etch) or 60 (multiple etch) is given for each data point.

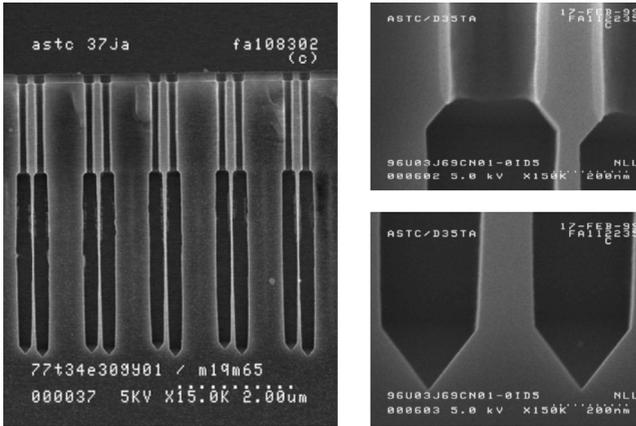
(see patent in Ref. [281]). In a first step the thin native oxide is removed from the surface and an H-terminated Si surface is generated applying diluted HF (200:1) for 60 s at RT (25 °C). Subsequently, the anisotropic etch is performed using 40:1 NH<sub>4</sub>OH ( $T = 25\text{--}45\text{ }^{\circ}\text{C}$ ; time = 60–120 s). The following reactions take place:



Besides the formation of a smooth single crystalline DT sidewall, this process increases the DT area (bottle-shaped DT) in the bottom portion, therefore significantly



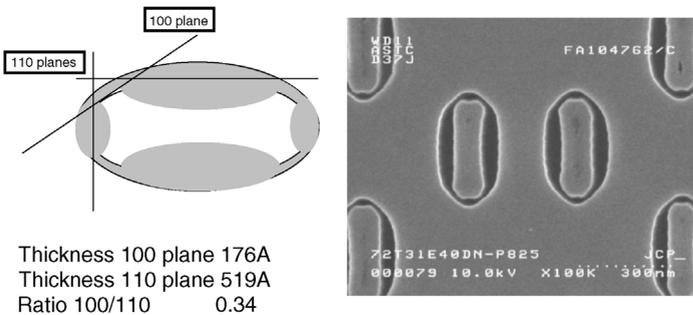
**Figure 1.67** Left: DT Si etch with an aspect ratio AR of 45 (single step DT etch); DT depth 6 μm, DT width 0.135 μm. Right: two-step DT Si etch with AR = 60; DT depth 8.6 μm, width 0.15 μm.



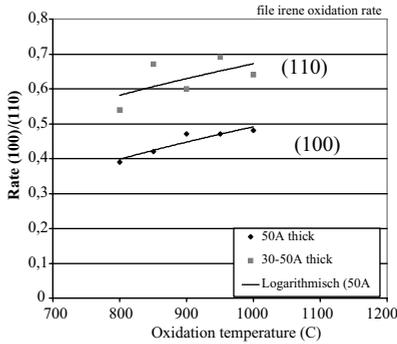
**Figure 1.68** SEM of a bottle-shaped DT. The corresponding etch leaves a single crystalline high-quality surface.

increasing the capacitance. The process is self-aligned to the DT-collar oxide, that is protected by a thin nitride layer which is formed in advance, that is, the reactions in both steps are highly selective with respect to Si<sub>3</sub>N<sub>4</sub>. Depending on the array layout (DT to DT distance) a capacitance increase of up to 80% can be achieved (e.g. in an 8 F<sup>2</sup> layout). The corresponding curve in the roadmap of Figure 1.65 is based on a 6 F<sup>2</sup> layout. For this specific example, a capacitance increase of 30% was achieved. Figure 1.68 shows cross-sections of DT bottle profiles. Owing to its anisotropy this etch simultaneously takes care of another important problem that is associated with the texture dependence of Si/SiO<sub>2</sub> growth.

In Figure 1.69 an example of a conventional DT top-view is shown (oval shape) after collar oxide formation (black region) and DT fill with a highly doped poly-Si. The thermal oxide formed shows a strong dependence on the crystal orientation of the Si surface. This holds true for all oxidation modes, for example, dry and wet oxidation (in the 'wet'-oxidation mode there is a carefully adjusted addition of H<sub>2</sub>O as steam to the oxidation chamber resulting in an increased oxidation rate). This also holds true for



**Figure 1.69** Top-down view of a DT structure without applying the anisotropic etch. The oxide collar (dark region) and the DT fill can be seen.

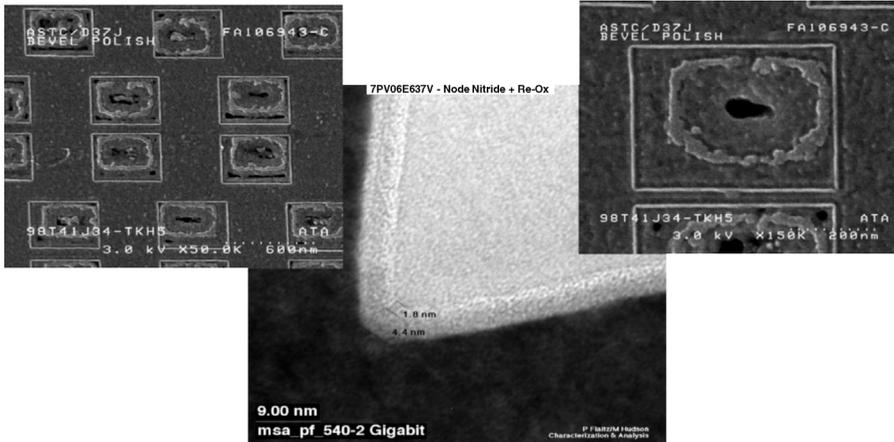


**Figure 1.70** SiO<sub>2</sub> oxidation rates on different Si surfaces.

an electrochemical oxide formation. The film thickness ratio between the oxides grown on the (100) and (110) surfaces can not be suppressed completely.

As an example, Figure 1.70 shows the oxide thickness on different Si surfaces for various formation modes, different forming temperatures, respectively. It is understandable that this non-uniformity constitutes a significant reliability problem for the SiO<sub>2</sub> films. For the aforementioned gate oxides, this problem was not addressed as the corresponding oxidation is performed on planar single crystalline wafer surfaces. In fact, the strong texture dependence of Si/SiO<sub>2</sub> oxide formation is one of the main reasons why single crystalline wafer surfaces are used in microelectronics. As soon as vertical structures such as the DT are used, this issue returns. For instance, for the dielectric node formation within the DT mentioned previously, this phenomenon must be considered. The minimum node thickness therefore is determined by the (110) planes where the thinnest oxide grows. A varying node oxide thickness inside the DT therefore has to be tolerated and, fortunately, for capacitor application it can be. However, for a potential vertical MOSFET it can not be accepted as the  $V_T$  depends on the oxide thickness, as shown above. A varying oxide thickness therefore means an uncontrolled threshold voltage, which in principle opposes MOSFET operation.

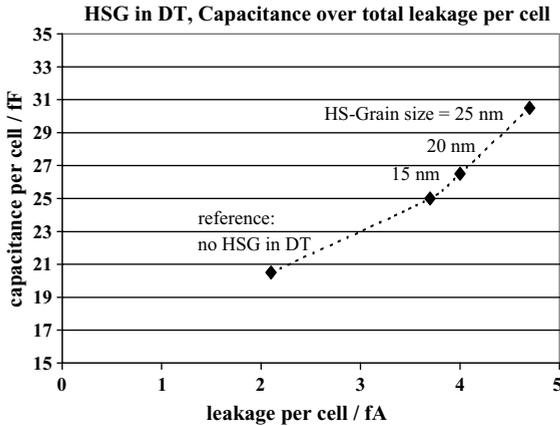
Nevertheless, such exact types of structures, that is vertical MOSFET within a DT, are currently being developed [308]. The key solution to overcome this problem lies in the anisotropic etch, as presented here. The top-down view of a DT after anisotropic etch and subsequent oxide formation and fill is shown in Figure 1.71. The DT shows a perfect rectangular shape, that is, the (100) plane is etched faster than the (110) plane and therefore is completely eliminated eventually, thus leaving a single crystalline (110) surface everywhere in the DT. The void inside of the poly-fill does not cause any problems (e.g. no resistance increase of the poly-fill), but Weibull slope reliability measurements actually showed a significantly improved node reliability for the anisotropically etched DTs. Accordingly, the center picture in Figure 1.71, showing a TEM high resolution zoom of the SiO<sub>2</sub> dielectric film, indicates an excellent uniformity of the film, even at critical sites such as the tip of the DT. The anisotropic etch therefore not only establishes an important means of increasing the DT capacitance, but more importantly, a high quality, single crystal surface is provided, which increases the reliability of the oxides formed upon it.



**Figure 1.71** Top-down view of anisotropically etched DT showing a perfect rectangular shape with (110) surfaces only. In the center, a high resolution TEM of the DT tip is shown with a perfectly uniform SiO<sub>2</sub> node dielectric inside.

**1.4.1.3.3 Hemispherical Silicon Grain HSG Formation** A further DT capacitance increase can be achieved by introducing a surface roughness on the trench sidewalls. For this, the well known hemispherical silicon grain (HSG) formation process can be used. This process requires deposition of a thin doped amorphous Si layer on top of the vertical trench walls. After lining, the structure is heated to initiate a nucleation (or seeding) process. In a subsequent annealing step the nuclei are grown to yield grains of the desired size (nuclei grow by mass transport of high mobility Si atoms), thus creating a rugged surface. For the DT, an exact and uniform growth of very small grains (below 25 nm) is essential to prevent any DT clogging. This requires a strict control of the process parameters therefore reducing the process windows.

Another principal problem with the use of rough surfaces such as HSG lies in the polycrystalline texture of the surface. Thus the texture dependence of oxide growth has to be considered again, causing the reliability problems mentioned. The only means to circumvent this problem is the use of deposition processes instead, or in addition to thermal or electrochemical dielectric film formation. Normally deposition rates do not depend on the texture. At present, a combination of thermal SiO<sub>2</sub> ( $\epsilon_r = 3.9$ ) and CVD deposited Si<sub>3</sub>N<sub>4</sub> ( $\epsilon_r = 7.2$ ) is one of the most commonly used dielectrics when combined with a rugged electrode such as HSG and/or three-dimensional capacitor structures. This dielectric multi-layer stack is termed ONO (SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub>) (oxide/nitride/oxide) or ON (SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>) (oxide/nitride). The ONO stack is prepared by successive thermal oxidation of the bottom polysilicon electrode, low-pressure chemical vapor deposition (CVD) of Si<sub>3</sub>N<sub>4</sub>, and thermal oxidation of the Si<sub>3</sub>N<sub>4</sub> film. In order to reduce the SiO<sub>2</sub> equivalent thickness, the bottom oxide layer can be removed from the film structure to form the ON structure. According to studies, the leakage current properties of these ONO and ON films are dominated by the Poole–Frenkel current [282, 283]. However, when the oxide



**Figure 1.72** DT capacitance as a function of node leakage for a reference process without HSG, and three different HSG processes with three different HSG grain sizes, respectively. For the measurements DT test structures with  $1F \times 1.5F$  top-down dimension ( $F = 0.15 \mu\text{m}$ , DT depth  $5 \mu\text{m}$ ) were used.

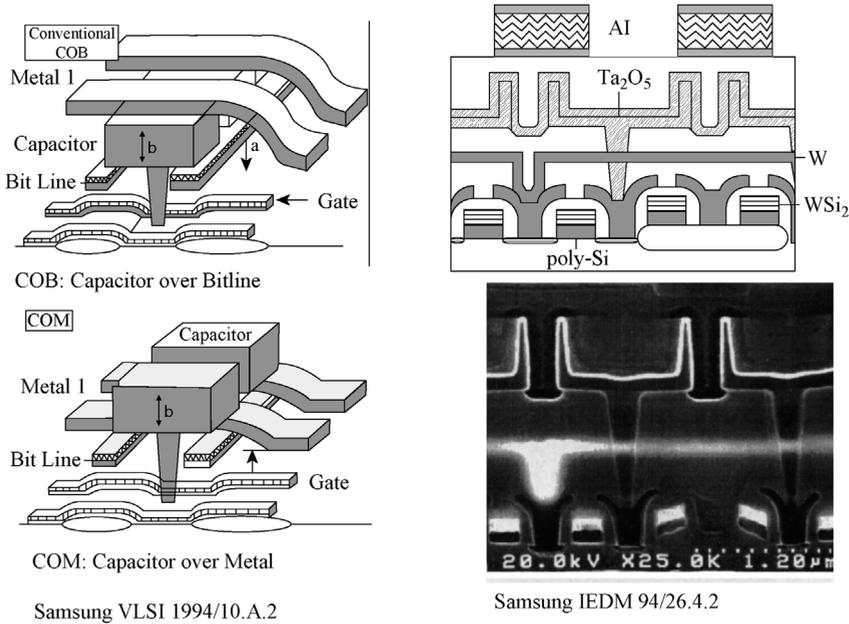
equivalent thickness becomes less than 5 nm, the leakage current properties become dominated by direct tunneling current. This is undesirable as the direct tunneling current can only be suppressed by increasing the physical thickness of the capacitor dielectrics [284]. This limits the equivalent thickness of ON films to 5 nm.

Furthermore, a transition layer exists between the polysilicon electrode and the bulk  $\text{Si}_3\text{N}_4$  film. This transition layer is formed when an initial layer of  $\text{Si}_3\text{N}_4$  is deposited on the native oxide and the mixture of  $\text{Si}_3\text{N}_4$ , native oxide, and Si nuclei form an Si-rich and defective layer. As the  $\text{Si}_3\text{N}_4$  film becomes ultra-thin, the oxide equivalent thickness of  $\text{Si}_3\text{N}_4$  rapidly decreases due to the density reduction in the defective layer. In addition, the tunneling leakage current rapidly increases [285]. To overcome this problem, the native oxide can be changed to a nitrided layer by performing rapid thermal nitridation (RTN) on the polysilicon electrode surface before CVD of  $\text{Si}_3\text{N}_4$  [284]. Figure 1.72 shows the effect of the HSG grain size on the capacitance and leakage currents of a DT using this type of ON film. With such a process, a capacitance gain of up to 50%, with node to buried plate leakage currents still meeting the specifications, can be achieved.

#### 1.4.2

##### Alternative Dielectric Materials

As the downscaling limits of conventional  $\text{SiO}_2$  and ONO dielectrics are reached, alternative dielectric films with higher dielectric constants  $\epsilon_r$  are needed. The valve metal oxides  $\text{TiO}_2$  ( $\epsilon_r$  up to 170) and  $\text{Ta}_2\text{O}_5$  ( $\epsilon_r = 25$ ) are among the candidates for the next generation of DRAMs. However, even high  $\epsilon_r$  ferroelectric materials such as (Ba, Sr) $\text{TiO}_3$  have been investigated for this purpose. The integration of  $\text{Ta}_2\text{O}_5$  has already been successfully realized within the 'stack capacitor' DRAM technology. In contrast



**Figure 1.73** Examples for 'stack-capacitor' DRAMS. In contrast to the 'deep trench' capacitor that is etched into the Si below the access transistor, the stack capacitor is deposited on top of the access transistor. Ta<sub>2</sub>O<sub>5</sub> is used as the dielectric film.

to the DT-DRAM technology, the stack storage capacitor is formed on top of the MOSFET access transistor and not below it. Consequently, the stack capacitor structure is not formed by an etch process but by deposition techniques. This limits the aspect ratio to about ten, whereas for the DT structures aspect ratios up to 100 were discussed above. Correspondingly, the active capacitor surface area of a stack capacitor is in principle smaller than for a DT capacitor and downscaling limits are reached earlier in stack capacitor technology.

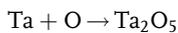
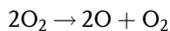
Thus, it is no surprise that Ta<sub>2</sub>O<sub>5</sub> was first introduced into the stack technology and that this technology has mainly driven alternative dielectric development in the past. In Figure 1.73 a typical stack storage capacitor structure using Ta<sub>2</sub>O<sub>5</sub> as the dielectric material is shown. For formation of alternative dielectric layers, principally it is deposition techniques such as PVD/CVD that have to be applied. Usually the resulting Si/dielectric film interfaces are more disturbed than the thermally or electrochemically formed ones (more interface defects). Moreover, the adhesion of the deposited films or/and an interface diffusion of atoms from the dielectric into the bulk can be critical. In order to improve the quality of the Si/dielectric interface, often barrier layers have to be used between the Si and the dielectric film. One example for such a stack has already been presented above, namely the ONO or ON stack. In the following sections the most important options for alternative dielectric materials, namely Ta<sub>2</sub>O<sub>5</sub>, TiO<sub>2</sub> and the ferroelectrics, are introduced.

#### 1.4.2.1 Ta<sub>2</sub>O<sub>5</sub>

Ta<sub>2</sub>O<sub>5</sub> can replace SiO<sub>2</sub> or ONO dielectric films without major process integration changes. Many methods for depositing Ta<sub>2</sub>O<sub>5</sub> films have been proposed. Among them, CVD methods such as LPCVD [286, 287], plasma-enhanced CVD (PECVD) [288, 289] and electron cyclotron resonance plasma-enhanced CVD (ECR PECVD) [292] are the most effective in depositing Ta<sub>2</sub>O<sub>5</sub> films. CVD methods are desirable because Ta<sub>2</sub>O<sub>5</sub> exhibits good step coverage [293]. High-temperature annealing is usually necessary to improve the quality of as-deposited tantalum oxide films prepared by all types of deposition methods, except for advanced methods such as PECVD and ECR PECVD [290, 291].

PECVD processes are based on the activation of a precursor by a high-energy plasma. The advantage of PECVD is that it provides both a high deposition rate and good step coverage [291]. The ECR PECVD process uses both microwave and a high magnetic field to create the plasma at low operating pressures. An ECR plasma decomposes the precursor so powerfully that high-quality films can be deposited at a low temperature. Furthermore, the low process pressure (down to 10<sup>-4</sup> Torr) inhibits the homogeneous gas-phase reactions, and the low ion energy offers the benefit of greatly reduced damage to the device [290]. Unlike other CVD processes, the electrical properties of the ECR PECVD film do not need to be improved by annealing in an oxygen ambience at high temperatures, due to the crystallization of the tantalum oxide film and the growth of the interfacial silicon oxide layer [290]. RTN, which forms an Si<sub>3</sub>N<sub>4</sub> barrier layer, is effective in preventing the formation of an interfacial SiO<sub>2</sub> layer for the LPCVD deposition of Ta<sub>2</sub>O<sub>5</sub> but is ineffective for the ECR PECVD system. This is because the Si<sub>3</sub>N<sub>4</sub> buffer layers are transformed into silicon dioxide during tantalum oxide deposition, due to the strong oxidation power of the ECR oxygen plasma [294].

Currently, titanium nitride (TiN) and tungsten (W) are being studied as buffer layers as they are expected to yield an interfacial oxide with higher dielectric constant in the ECR oxygen plasma [294]. As typical precursor materials for Ta and Ta<sub>2</sub>O<sub>5</sub> CVD deposition, liquids such as Ta(OCH<sub>3</sub>)<sub>5</sub>, Ta(OC<sub>2</sub>H<sub>5</sub>)<sub>5</sub> and related alkoxides, and solid materials, such as TaCl<sub>5</sub> and related halides, are usually used. The advantage of liquid sources is the good controllability of flow rate over a wide range. However, the Ta<sub>2</sub>O<sub>5</sub> deposited using liquid sources by thermal CVD or photo-CVD are subject to carbon contamination, which leads to poor electrical properties. On the other hand, the use of plasma-enhanced CVD and ECR CVD oxidizes the Ta(OC<sub>2</sub>H<sub>5</sub>)<sub>5</sub> so strongly that it dissociates under the applied electric field in the plasma and reacts with ionized oxygen molecules in the following chain reaction that forms Ta<sub>2</sub>O<sub>5</sub>:



Thus Ta<sub>2</sub>O<sub>5</sub> is deposited and the carbon compounds are evacuated [288]. The only disadvantage is that a thick interfacial SiO<sub>2</sub> layer with a low dielectric constant will be formed during PECVD.

Solids such as TaCl<sub>5</sub> can also be used as source material for Ta<sub>2</sub>O<sub>5</sub> deposition but have the disadvantage of poor controllability of the flow rate. One concern about as-deposited CVD Ta<sub>2</sub>O<sub>5</sub> capacitors is the excessive leakage current that is exhibited, which is believed to be caused by a deficiency of oxygen in the as-deposited film. To fill the vacancies with oxygen to reduce leakage current and to improve the electrical properties of CVD Ta<sub>2</sub>O<sub>5</sub> capacitors, various post deposition annealing techniques have been proposed, for example: annealing in O<sub>2</sub> [296], UV-O<sub>3</sub> [297] and dry O<sub>2</sub> [297, 298]; rapid thermal O<sub>2</sub> annealing (RTO) [293]; and rapid thermal annealing in N<sub>2</sub>O (RTN<sub>2</sub>O) [299, 300]. Among these annealing techniques, rapid thermal annealing (RTA) in N<sub>2</sub>O is the most effective in suppressing leakage current [300]. However, the oxygen atoms from N<sub>2</sub>O produce a thicker interfacial SiO<sub>2</sub> layer than conventional techniques with oxygen, because N<sub>2</sub>O is a better oxidizing agent [301]. The formation of an interfacial oxide reduces the effective dielectric constant, which is a serious disadvantage for high dielectric capacitor applications. Thus, RTN treatment is required to suppress the oxidation during annealing [285].

During the dry-O<sub>2</sub> annealing, the densification of the Ta<sub>2</sub>O<sub>5</sub> film due to hydrocarbon desorption decreases the equivalent thickness. At higher annealing temperatures, the growth of an SiO<sub>2</sub> layer at the interface between Ta<sub>2</sub>O<sub>5</sub> and Si leads to an increase in the SiO<sub>2</sub> equivalent thickness. When no-RTN treatment is performed prior to Ta<sub>2</sub>O<sub>5</sub> deposition, the oxide equivalent thickness is monotonously increased because of the oxidation of the Si surface.

An additional serious problem of Ta<sub>2</sub>O<sub>5</sub> capacitors is caused by their exposure to high temperature, which unavoidably occurs in subsequent process steps. One example is the boro-phospho-silicate glass (BPSG) reflow process after capacitor formation in the stack technology. Here temperatures up to 600 °C occur. In DT technology this problem is even more severe as here several process steps with temperatures up to 1050 °C are applied. The Ta<sub>2</sub>O<sub>5</sub> degradation in BPSG reflow with a top TiN electrode was shown to be due to TiN oxidation at the TiN/BPSG interface [302, 303]. The TiN oxidation leads to a volume expansion and build-up of compressive stress, which eventually leads to cracks in the Ta<sub>2</sub>O<sub>5</sub> film. As a result, the leakage current is increased. This problem could be fixed by placing a thin layer of poly-Si between TiN and BPSG thus suppressing the TiN oxidation and therefore reducing the leakage current [303]. The Ta<sub>2</sub>O<sub>5</sub> dielectric with the bi-layered TiN/poly-Si top electrode was applied successfully to the full process for 256-Mbit stack-DRAM devices. Degradation free Ta<sub>2</sub>O<sub>5</sub> capacitors can be produced. As mentioned earlier, an interfacial oxide layer that has a low dielectric constant is inevitably grown during Ta<sub>2</sub>O<sub>5</sub> deposition and the post-deposition annealing process. The bottom electrode also affects the interfacial oxide layers and the capacitance of the dielectric film.

It was found that for ECR PECVDA, different electrode materials have different incubation periods, which is the time required to cover up the substrate surfaces completely with Ta<sub>2</sub>O<sub>5</sub>. Furthermore, the incubation period for the Ta<sub>2</sub>O<sub>5</sub> film

deposition was related to the oxidation of the electrodes [304]. The effect of the interfacial oxide layer on the capacitance of the dielectric film is:

$$C = \epsilon_0 \epsilon_r \frac{A}{d_{\text{Ta}_2\text{O}_5}^* + d_{\text{io}}^*} \quad (1.44)$$

$$d_{\text{Ta}_2\text{O}_5}^* = d_{\text{Ta}_2\text{O}_5} \cdot \epsilon_{\text{SiO}_2} / \epsilon_{\text{Ta}_2\text{O}_5} \quad (1.45)$$

$$d_{\text{io}}^* = d_{\text{io}} \cdot \epsilon_{\text{SiO}_2} / \epsilon_{\text{io}} \quad (1.46)$$

where  $A$  is the capacitor area,  $\epsilon_0$  is the permittivity of empty space and  $\epsilon_{\text{SiO}_2}$ ,  $\epsilon_{\text{Ta}_2\text{O}_5}$  and  $\epsilon_{\text{io}}$  are the relative dielectric constants of  $\text{SiO}_2$ ,  $\text{Ta}_2\text{O}_5$  and the interfacial oxide (io), respectively;  $d_{\text{Ta}_2\text{O}_5}$  and  $d_{\text{io}}$  are the thickness of the  $\text{Ta}_2\text{O}_5$  film and the interfacial oxide layer, respectively. Therefore, when  $\text{Ta}_2\text{O}_5$  is used as a capacitor material, the capacitance is actually determined by  $(d_{\text{Ta}_2\text{O}_5}^* + d_{\text{io}}^*)$ . Thus,  $d_{\text{io}}$  should be reduced to a value as small as possible.

According to the literature, a platinum (Pt) bottom electrode does not form any interfacial oxide ( $d_{\text{io}}^* = 0$ ) and thus offers the highest capacitance. However, at present it can only be deposited by physical vapor deposition (PVD) methods, which give poor step coverage, and therefore is excluded for an eventual DT process (high aspect ratio). On TiN and W bottom electrodes, interfacial oxide is formed with thicknesses of 0.9 and 2.1 nm, respectively, which are less than the ones formed on a pure Si electrode ( $d_{\text{SiO}_2}^* = 4$  nm). Both TiN and W can be deposited by CVD, which gives good step coverage, and are currently already used in other DRAM process steps. Between the two, TiN has a lower  $d_{\text{io}}^*$  value and is very stable with  $\text{Ta}_2\text{O}_5$  at high temperatures (700–900 °C). Thus, TiN is the most promising material as a bottom electrode when used for  $\text{Ta}_2\text{O}_5$  dielectric films [304].

The electrode material also affects the leakage current of the  $\text{Ta}_2\text{O}_5$  capacitors. It was found that among some common metal and nitride electrodes (W, Mo, Ti, WN, MoN, TiN and TaN), the voltage that induces a leakage current of  $1 \mu\text{A cm}^{-2}$  ( $V_{\text{crit}}$ ) increases with the work function of the electrode immediately after electrode formation and after annealing at 400 °C [305]. Thus, for a low-temperature annealing process, the leakage current in the  $\text{Ta}_2\text{O}_5$  film at a given voltage decreases with increasing work function of the top electrode. This result indicates that the conduction mechanism is an electrode-limited type, and that the barrier height for the electrons at the top electrode/ $\text{Ta}_2\text{O}_5$  interface limits the leakage current. For high-temperature annealing (800 °C), there is almost no correlation between the work function and the leakage current. It is assumed that after high-temperature annealing, the current is affected by the reaction between  $\text{Ta}_2\text{O}_5$  and the electrode. It was found that TiN is the optimum electrode for low temperature processes (about 400 °C) while Mo or MoN are the optimum electrodes for high-temperature processes (about 800 °C) because they exhibit the smallest leakage current [305].

The downscaling limit of  $\text{Ta}_2\text{O}_5$  capacitors is estimated to be around an equivalent oxide thickness of 1.5 nm [284]. Combined with polysilicon electrode techniques, such as HSG,  $\text{Ta}_2\text{O}_5$  capacitors will be available for 1 Gb DRAMs and beyond.

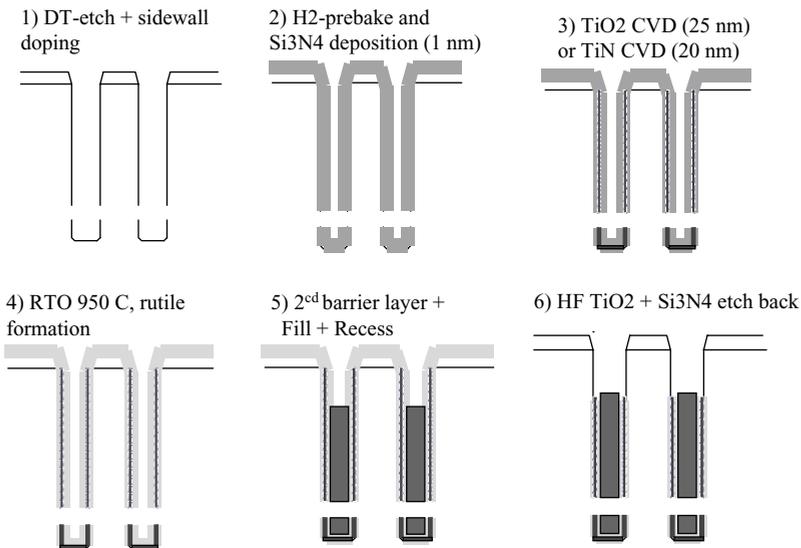
Currently, Ta<sub>2</sub>O<sub>5</sub> has already reached the stage of practical use and is the most likely choice for replacement of ONO/ON dielectrics after the 256 Mbit generation.

#### 1.4.2.2 Ti/TiO<sub>2</sub>

Another possible candidate as an alternative dielectric for DT technology is TiO<sub>2</sub> (see patent Ref. [306]). The dielectric constant of crystalline rutile is between 86 for a crystal orientation with the optical axis (c-axis) perpendicular to the surface and 170 for the c-axis parallel to the surface. This exceptionally high  $\epsilon_r$  allows relatively thick dielectric layers (>30 nm) with an SiO<sub>2</sub> equivalent thickness  $t_{eq}$  still below that of pure SiO<sub>2</sub> or ONO to be employed. Therefore, in contrast to the previously described dielectrics, for TiO<sub>2</sub> a crystalline layer might be acceptable. (As explained in Section 1.3, ultra-thin dielectric, amorphous films must be used in order to keep the leakage current low.) The use of a crystalline film is beneficial in DT technology due to its better stability with respect to high temperatures. In DT technology several high temperature steps (up to 1050 °C) are required after node dielectric deposition.

The temperature stability is therefore a decisive advantage of rutile TiO<sub>2</sub> in comparison with the other mentioned dielectrics. In order to generate the required rutile phase high temperatures up to 1050 °C are necessary. In contrast to the stack capacitor technology, these temperatures are no problem in DT technology (which explains why TiO<sub>2</sub> is not used for stacked capacitors). With TiO<sub>2</sub> dielectrics, leakage currents below  $10^{-10}$  A cm<sup>-2</sup> have been reported in the literature [307]. For TiO<sub>2</sub> deposition, the following process scheme, illustrated in Figure 1.74, could be possible:

1. DT etch and buried plate formation as usual.
2. Si<sub>3</sub>N<sub>4</sub> barrier layer formation by nitridation (thickness below 1 nm).



**Figure 1.74** Possible process steps for forming a TiO<sub>2</sub> dielectric layer in a DT storage capacitor. Details are described in the text.

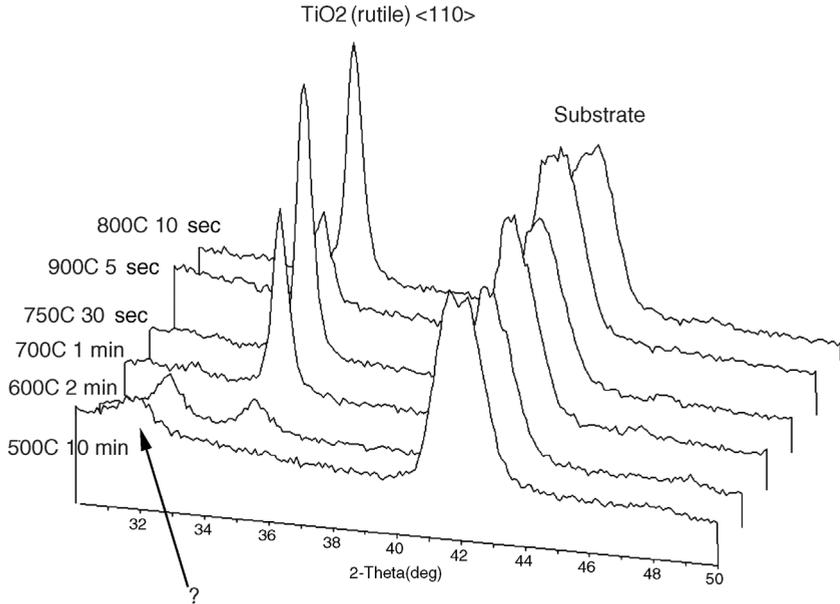


Figure 1.75 XRD-spectra. Temperature dependence of  $\text{TiO}_2$  rutile formation.

3. CVD-TiN-deposition. Alternatively, a direct PECVD  $\text{TiO}_2$  deposition is possible. However, the conformity of the TiN deposition is superior.
4. Oxidation above  $950^\circ\text{C}$  to form the rutile phase. For this, a complete oxidation of the TiN has to be achieved. This can, for example, be checked by optical *in situ* methods such as SAME, which allows for the determination of the crystallographic orientation, as was explained in Section 1.3.
5. Second barrier layer ( $\text{Si}_3\text{N}_4$ ) + DT fill with highly doped polysilicon + planarization by CMP (chemical mechanical polishing) + oxide collar recess as usual.
6. Etchback of  $\text{TiO}_2$  in the collar portion using HF/glycerol.

The temperature dependence of rutile formation from such a TiN was measured by X-ray diffraction. The results are shown in Figure 1.75.

## 1.5

### Summary and Conclusions

A whole variety of technologies exist for passive and integrated circuit (IC) capacitor fabrication. There is however one common denominator for all these different technologies: they all make use of deliberately chosen *valve metal*, *Si* and *ceramic oxides* as the dielectric thin films, which therefore *play a key role in electronics*. The reasons for this and the underlying research issues were discussed in this chapter.

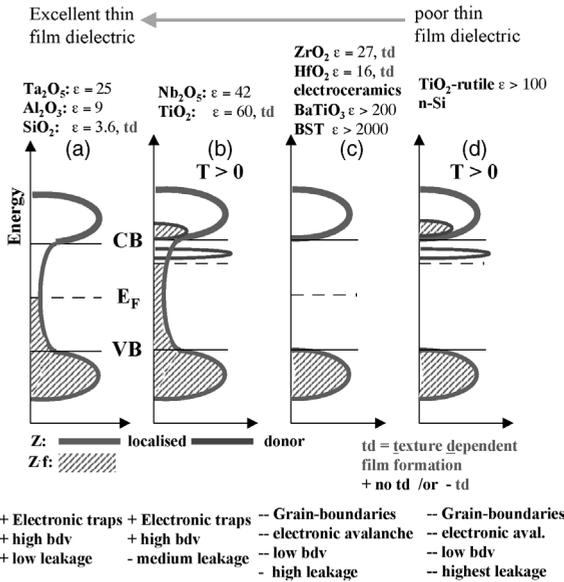
In order to maximize the capacitance  $C$ , generally an increase of the capacitor plate surface area  $A$ , the use of higher dielectric constant  $\epsilon_r$  materials and decreasing dielectric film thickness  $d_f$  is pursued (simple capacitor equation  $C = \epsilon_r A / d_f$ ). However, there is no single, cost effective technology available yet that simultaneously combines an optimum of all these parameters. The highest capacitance volume efficiency is achieved with electrolytic capacitors such as Ta capacitors. It was shown that the major reason for this is due to the application of a sinter process, which allows the formation of a three-dimensional, sponge-like capacitor plate structure with extremely large surface area (several  $\text{m}^2 \text{g}^{-1}$ ). A thin dielectric film (15 to 200 nm) is formed directly on top of this porous substrate by electrochemical anodization.

For integration of capacitors into ICs, 'deep trench' structures can be used. The dielectric oxides have to be compatible with the integration process. The integration scheme of IC fabrication was described using DRAM technology as an example. The extremely sophisticated IC integration schemes usually exclude the application of fancy high  $\epsilon_r$  materials, such as the ceramic perovskites. In order to keep the capacitance high, ultra-thin (nano) dielectric films must be employed. For  $\text{SiO}_2$  or  $\text{Si}_3\text{N}_4$ , the film thickness rapidly approaches the minimum tunnel limit of  $<3$  nm. Owing to the thin dielectric film thickness for IC and electrolytic capacitors, the oxides have to withstand extremely high electric fields even at moderate applied voltages (e.g.  $E = 10^8 \text{ V m}^{-1}$  for  $d_f = 100$  nm and  $U_{\text{applied}} = 10$  V). Moreover, they reliably have to endure thermal (typically  $-40$  up to  $125$  °C) and mechanical stresses over a minimum device lifetime of between 5 and 20 years. The demands are thus for an optimized combination of material properties, which have been discussed and studied.

Some of the key properties of the various oxide systems are summarized and compared in the band models of Figure 1.76. In order to tolerate high electric field strengths for a long time, the dielectric film has to have an amorphous structure. This is due to the continuum of localized states within the mobility gap, which act as traps for the electrons and therefore prevent critical electron acceleration up to a level where dielectric breakdown (avalanche ionization) occurs. Therefore, all established ultra-thin film dielectrics, namely  $\text{SiO}_2$ ,  $\text{Al}_2\text{O}_3$  and  $\text{Ta}_2\text{O}_5$  show uniform amorphous structures. This 'knock out' criterion for ultra-thin film application is also fulfilled by  $\text{Nb}_2\text{O}_5$  and  $\text{TiO}_2$ . However, the latter systems tend to form sub-oxides (e.g.  $\text{NbO}$ ,  $\text{Nb}_2\text{O}$  and the Magnéli phases in the case of  $\text{TiO}_2$ ) resulting in non-uniform oxide properties. The oxygen vacancies act as donors in the mobility gap. Consequently, these oxides show a pronounced n-type semiconducting behavior.

By Schottky–Mott analysis of the bias dependent capacitance measurements a quantitative determination of the donor defect state concentration  $N_D$  is possible. For the anodically formed  $\text{Nb}_2\text{O}_5$  and  $\text{TiO}_2$  films,  $N_D$  is typically in the order of  $10^{20} \text{ cm}^{-3}$ . These systems therefore show higher leakage currents than the insulating  $\text{Ta}_2\text{O}_5$ ,  $\text{SiO}_2$  and  $\text{Al}_2\text{O}_3$  films. Moreover,  $\text{Nb}_2\text{O}_5$  and  $\text{TiO}_2$  are prone to dislocation formation (local crystallization), which further increases the leakage current. In the case of  $\text{TiO}_2$  even crystallization to the rutile or anatase phase can occur at high formation potentials above 50 V.

The valve metal oxide systems  $\text{ZrO}_2$  and  $\text{HfO}_2$  and most of the typical electro-ceramic perovskite compounds such as  $\text{BaTiO}_3$  and  $(\text{Ba,Sr})\text{TiO}_3$  (BST) show an



**Figure 1.76** Band models of the various oxide systems. The oxides can be placed into four groups regarding their suitability as ultra-thin dielectric film. Performance degrades from left to right. (a)  $\text{Ta}_2\text{O}_5$ ,  $\text{Al}_2\text{O}_3$  and  $\text{SiO}_2$  show an amorphous structure. This is essential for ultra-thin dielectric films, as the continuum of localized states in the mobility gap act as electron traps. This prevents electron avalanche breakdown resulting in highest bdv (breakdown voltage). (b)  $\text{Nb}_2\text{O}_5$  and  $\text{TiO}_2$  are also amorphous, but show a high donor concentration due to oxygen vacancies. These oxides therefore show n-type

semiconducting behavior with an increased leakage. (c)  $\text{ZrO}_2$ ,  $\text{HfO}_2$  and perovskite electroceramics usually show crystalline structures with a high density of grain boundaries that act as high leakage paths. Owing to the reduced bdv, these materials are preferentially used for thicker film applications ( $>1 \mu\text{m}$ ), e.g. MLCC technology. (d) Rutile  $\text{TiO}_2$  with oxygen vacancies shows the worst combination of electronic properties for dielectric applications. It behaves as n-type Si. Z, density of states; Zf, occupied states; CB and VB, conduction and valence band edge;  $E_F$ , Fermi energy.

excellent insulating behavior with no bias dependence of capacitance at all. However, as illustrated in the band model of Figure 1.76, they usually form crystalline oxides, which are prone to dielectric breakdown at high field strengths. Therefore, it is difficult to integrate these systems into technologies such as integrated circuits where single digit nm thick films are needed. However, they are widely used for multilayer ceramic capacitors (MLCC) where thicker dielectric films ( $>1 \mu\text{m}$ ) are acceptable.

The presented electrochemical measurements prove that formation conditions sensitively affect the electronic film properties. Consequently, the formation conditions can be used for an adjustment and control of electronic properties to a certain extent. For instance, in the case of  $\text{Ti}/\text{TiO}_2$  changing from potentiodynamic to potentiostatic formation, conditions allows for significant reduction of the donor defect state concentration. Moreover, under potentiodynamic conditions, a pronounced texture dependence of oxide growth is observed, which can be significantly suppressed by potentiostatic formation. The texture dependence itself

was investigated by means of the new nl-photoresist droplet method, which allows all types of electrochemical measurements to be performed at high lateral resolution, for example, on single substrate grains. Simultaneously, optical methods were applied to the same single substrate grains. With the new 'Spectroscopic Anisotropy Micro-Ellipsometry' method (SAME) crystallographic properties such as the surface orientation of substrate grains and crystallization of anodically formed films and their epitaxial relationship to the substrate grains could be determined. It was shown that SAME, along with the new nl-photoresist method, is a powerful tool for studying of texture dependent anodic oxide growth.

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