1
Carbon Nanotubes in Microelectronic Applications

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1.1
Introduction

Carbon nanotubes (CNTs) are the hottest topic in physics, according to a 2006 ranking of different scientific fields in the published literature [1]. The interest in these objects has been sparked by the exceptional properties of those nano-sized objects combined with the ease of theoretical investigations due to the relatively limited number of atoms in CNTs, facilitating *ab initio* calculations [2]. The first investigations of CNT properties reveal many interesting features which are very attractive for solving the technological hurdles that the semiconductor industry is

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facing if scaling of circuits continues for another decade [3, 4]. The high current-carrying capacity, high thermal conductivity and reduced charge carrier scattering combined with the huge resilience of CNTs promise to solve challenges in the interconnect area, whereas the low effective electron and hole mass, the attractive band gap and the absence of dangling bonds address the needs of a fast, energy-efficient and high-k dielectric-compatible device of the future.

However, the step from a hand-crafted, proof-of-concept device example to a highly integrated, reliable technology is huge and hardly achievable within a few years. Therefore, this chapter summarizes some critical aspects of a microelectronic-compatible integration of CNTs and highlights the recent progress that has been achieved in terms of possible applications.

1.2 Carbon Nanotube Basics

Carbon nanotubes may be considered to be graphene cylinders. Graphene is a single planar sheet of sp^2-bonded carbon atoms, as shown in Figure 1.1. Graphite consists entirely of individual graphene layers, which are stacked on each other. The properties of graphite already give a first hint towards the remarkable properties of carbon nanotubes. The charge carrier densities in graphite are almost equal for electrons and holes ($n_e \approx n_h \approx 7 \times 10^{18}\,cm^{-3}$) and routinely measured mobilities are of the order of $10^4\,cm^2\,V^{-1}\,s^{-1}$ at room temperature and $10^6\,cm^2\,V^{-1}\,s^{-1}$ at 4.2 K [5]. The in-plane resistivity is as low as $50\,\mu\Omega\,cm$ and can be engineered down to $1\,\mu\Omega\,cm$, which is half of the value of copper by doping and intercalation [5]. The thermal conductivity of graphite is also very high, ranging between 24 and $470\,W\,m^{-1}\,K^{-1}$. Recent experiments have verified these remarkable properties also in individual graphene layers and even field effect modulation of the conductivity has been demonstrated in these samples, leading to a first verification of a recently proposed metallic field effect transistor [6, 7]. However, the viability of graphene-based microelectronic devices and interconnects is limited by the high temperatures of 1400–2000 °C which are required to fabricate graphite or graphene.

1.2.1 Band Structure of Carbon Nanotubes

The basic structure of CNTs is shown in Figure 1.1. A single-walled CNT (SWCNT) can be thought of as a rolled-up graphene sheet in which the edges of the sheet are joined together to form a seamless tube. By changing the direction in the roll-up, different chiralities can be created. Further, several tubes of different diameter can be fitted into each other to make a multi-walled carbon nanotube (MWCNT), as shown in Figure 1.1.

The band structure of graphene is the basis for understanding the electronic behavior of carbon nanotubes. Graphene has a honeycomb lattice structure of carbon atoms in the sp^2 hybridization state. Every lattice point of the two-

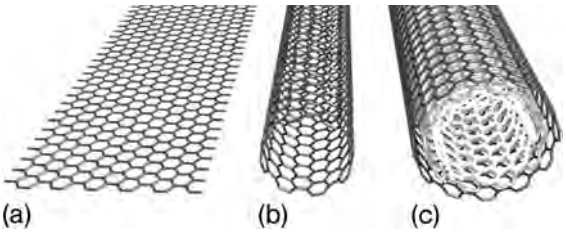


Figure 1.1 Structure of a single layer of graphite (graphene) (a), single-walled carbon nanotube (b) and a multi-walled carbon nanotube with three shells (c).

dimensional graphene point can be described by multiples (n,m) of two unit vectors a_1 and a_2, as shown in Figure 1.2a. The multiples are also used to describe the chirality of the CNT by defining the chiral vector $C_h = n \cdot a_1 + m \cdot a_2$. The length of C_h is just the circumference of the CNT. Every CNT is then characterized by the two indices (n,m). There are two carbon atoms in a unit cell and each atom contributes a free electron. The Brillouin zone of graphene is shown in Figure 1.2 and has been calculated by a simple tight-binding approach. The Brillouin zone is also hexagonal in shape and the unhybridized orbitals give rise to valence and conduction bands. The band structure of graphene is unique in the sense that at the six corners of the Brillouin zone, the valence and the conduction bands meet exactly at a point where the Fermi energy lies.

The cones in Figure 1.2b represent the electron energy dispersion of graphene close to the Fermi energy and the parallel lines indicate the allowed states of a nanotube with the periodicity around the circumference in reciprocal space. By imposing the quantization condition, $C_h \cdot k = 2\pi q$, of the wavevector k around the circumference C_h, the energy landscape is cut into slices of allowed states as indicated in Figure 1.2b by the thick solid lines. The slices are separated by $2/d$, where d is the diameter of the tube. The spacing of the lines is inversely proportional to the CNT diameter and their angle depends on the nanotube chirality or index (n,m). For specific tube diameter and chirality the lines intersect with the apex of the cones, as shown in Figure 1.2d, and the nanotubes are metallic, i.e. there is an allowed state at the Fermi energy. If, as shown in Figure 1.2c, the lines intersect elsewhere on the cones, there is a band gap around the Fermi energy and the tubes are semiconducting. For larger diameter CNTs the spacing between the lines is reduced and the maximum possible band gap decreases. The condition for achieving metallic tubes can be expressed by $n - m = 3q$, with q being an integer [8]. The electrical properties of CNTs are strongly dependent on the chirality and the tube diameter.

Every possible nanotube configuration (n,m) can be mapped by symmetry operations on the blue and red colored dots in Figure 1.2e. From a statistical point of view, one-third of the possible nanotube conformations are metallic whereas the remaining two-thirds are semiconducting. This can be deduced by analysis of the index map shown in Figure 1.2e. This has severe implications as no specific chirality can be grown to date and one always obtains a mixture of chiralities of

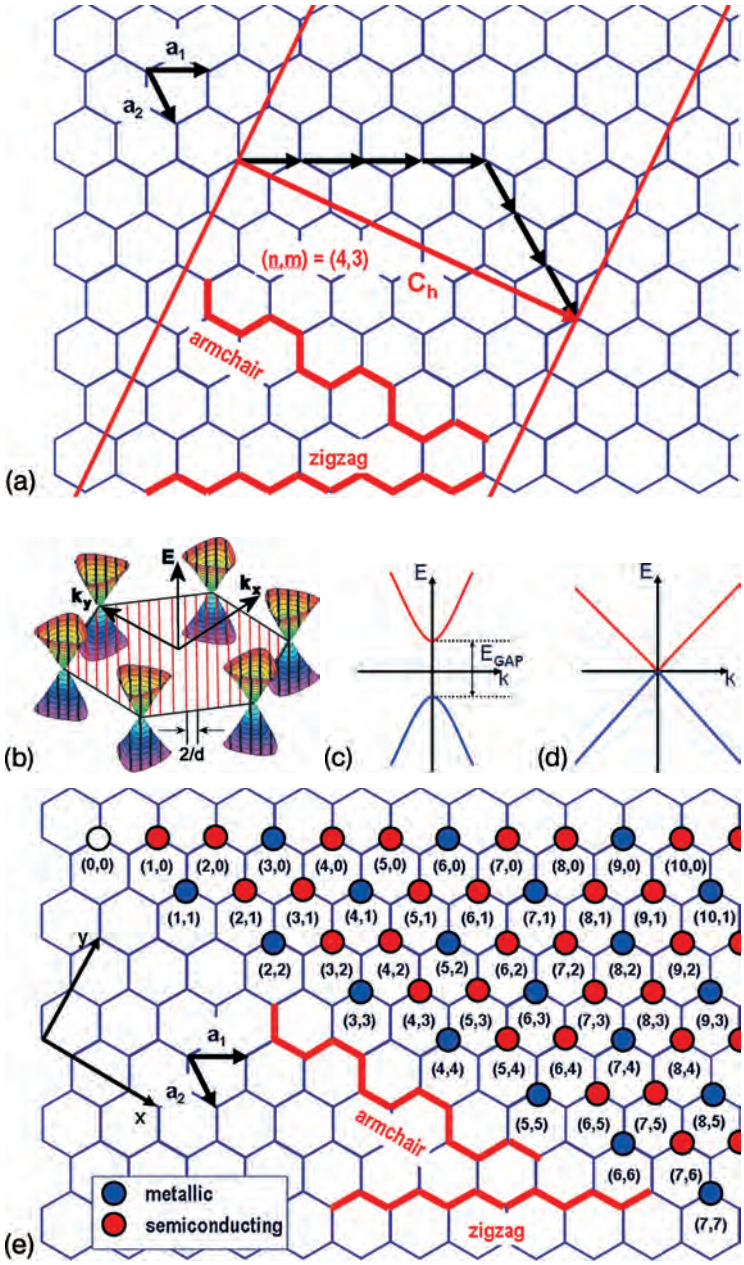


Figure 1.2 (a) The index (*n*,*m*) determines the chirality of the CNT and the circumference C_h. To make a CNT with index (4,3), the graphene layer needs to be cut out along the two parallel gray lines and rolled up to from a seamless cylinder. (b) The band structure of graphene form hexagonal cones in the vicinity of the Fermi energy. The formation of a nanotube cuts the energy landscape into slices of allowed states. The location of the conic section determines whether the resulting band structure is semiconducting (c) or metallic (d). (e) A map showing which (*n*,*m*) gives semiconducting and metallic tubes can be drawn. Only armchair CNTs (*n* = *m*) are strictly metallic.

predominantly semiconducting CNTs. The band gap of semiconducting SWCNTs is inversely proportional to the diameter and corresponds to 0.8 eV for a tube with a diameter of 1 nm. Single-walled tubes with diameters up to 5 nm and as small as 0.4 nm have been observed, but the diameter is typically between 0.7 and 2 nm, providing band gaps in a range that is interesting for transistor and diode applications [3, 8]. Multi-walled nanotubes with diameters up to 100 nm have been observed although their diameters are usually around 10–20 nm. The separation of the layers in an MWCNT is about the same as in graphite and corresponds to 0.34 nm. The curvature of the nanotube, especially at small diameters, leads to some modifications which are not incorporated in a simple tight-binding approximation [8]. Even CNTs which satisfy the condition $n - m = 3q$, with q being an integer, develop a small band gap due to the distortion of the bonds and are so-called small band gap CNTs. Only CNTs with $n = m$ are genuine metallic tubes due to their special symmetry. The effect is only important at very small diameters, because the distortion induced band gap scales inversely with the square of the diameter [8]. For example, while a semiconducting nanotube with a diameter of 1 nm has a band gap of 0.8 eV, a semimetallic nanotube with a comparable diameter has a band gap of only 40 meV.

1.2.2 Fabrication of Carbon Nanotubes

There are three main methods to produce CNTs: arc discharge, laser ablation and catalyst-enhanced chemical vapor deposition (CCVD). Each of these techniques has its advantages and disadvantages, which are only briefly discussed below due to the extensive literature available on this topic [3, 4, 9, 10].

Arc discharge and *laser ablation* rely on the evaporation of a graphite target to create gas-phase carbon fragments that recombine to form CNTs. The temperatures reached in these processes are in the range 2000–3000 °C, more than sufficient for the carbon atoms to rearrange into the tube structure. In order to increase the yield of nanotubes in the carbon material created, several different metals in concentrations of the order of 1% are incorporated into the target material that is evaporated. The metals evaporate with the carbon and coalesce into clusters that form a base from which the nanotubes can grow.

Under optimized conditions, both of these processes produce nanotubes with the highest achievable crystallinity due to the high temperature during formation. Unfortunately, a large amount of unwanted non-nanotube graphitic and amorphous carbon material is also produced, and a cleaning process is necessary before the nanotubes can be used. Further, the purified nanotubes are dispersed in a solvent and are typically deposited in a random manner on the substrate by dipping, spraying or spin-on. This is useful for investigations of the physical properties of CNTs in individual "hand-crafted" devices or for large-size applications, such as conductive transparent coatings or conductive plastic material, but is not suitable for the reproducible, parallel integration of CNTs into microelectronic systems. On the other hand, preparation of the nanotubes in solution allows

the application of various processes to separate the semiconducting and metallic CNTs and chemically functionalize the CNTs.

Catalyst-enhanced chemical vapor deposition utilizes small metal catalyst clusters in the gas phase or on surfaces to decompose a carbon containing feedstock gas, such as methane or acetylene. The resulting carbon dissolves in, or is adsorbed on, the catalyst particle and is released in the form of a nanotube starting with a buckyball-type cap when the concentration exceeds the maximum solubility. The nanotube continues to grow as long as carbon continues to be delivered at the right rate and the form of the catalyst does not change. The growth temperature depends on the type of nanotube to be grown and the catalyst composition and lies in the range 400–1100 °C, lower than the temperatures in the arc discharge or laser ablation processes. For this reason, it is believed that CCVD tubes have a higher density of defects.

The advantage of CCVD nanotube production is the possibility of structuring the catalyst particles and, hence, selectively growing the nanotubes where they are required. Further, under the right conditions only nanotubes are produced and no unwanted graphitic material. Using this CCVD method, SWCNTs and MWCNTs can be grown on semiconductor wafers with semiconductor production equipment without almost any equipment modifications using carbon-containing gases such as methane or acetylene.

1.2.3 Density of States, Resistance and Resistivity

The density of states (DOS) without small band gap effects can be easily calculated for different CNTs following an approach of Mintmire and White [11] or using the online simulation facilities of www.nanohub.org [12], both of which are based on the tight-binding approach. The result for two metallic CNTs with diameters of 1 and 20 nm are shown in Figure 1.3. The DOS is constant in an energy window of 2 eV for the 1-nm diameter CNT and additional van Hoove states are energetically far away from the Fermi energy. In contrast, the 20-nm thick CNT, which might constitute the outer shell of an MWCNT, has additional states available in an energy window of ~0.2 eV and can be much easier manipulated by charge transfer doping. In Figure 1.3, a small p-doping of the 20-nm diameter CNT is assumed, which shifts the Fermi level below the charge neutrality point of the undoped CNT.

The DOS of CNTs is four orders of magnitude smaller than that of metals and this would normally result in bad conductivity. However, the one-dimensional nature of the nanotubes leads to a huge mean free path of the order of 1–10 μm of the charge carriers, in contrast to that of metals, which is around 40 nm for copper. Additional states have to be available for the scattered carriers, to where the charge state can be scattered. However, additional states for small-angle scattering events are energetically far away due to the circumferential quantization. The only allowed states are in the direction along the CNT. The phase space for scattering is therefore strongly restricted, even at room temperature. At low bias voltage the only energetically allowed state to be scattered to is just backwards in the opposite direction.

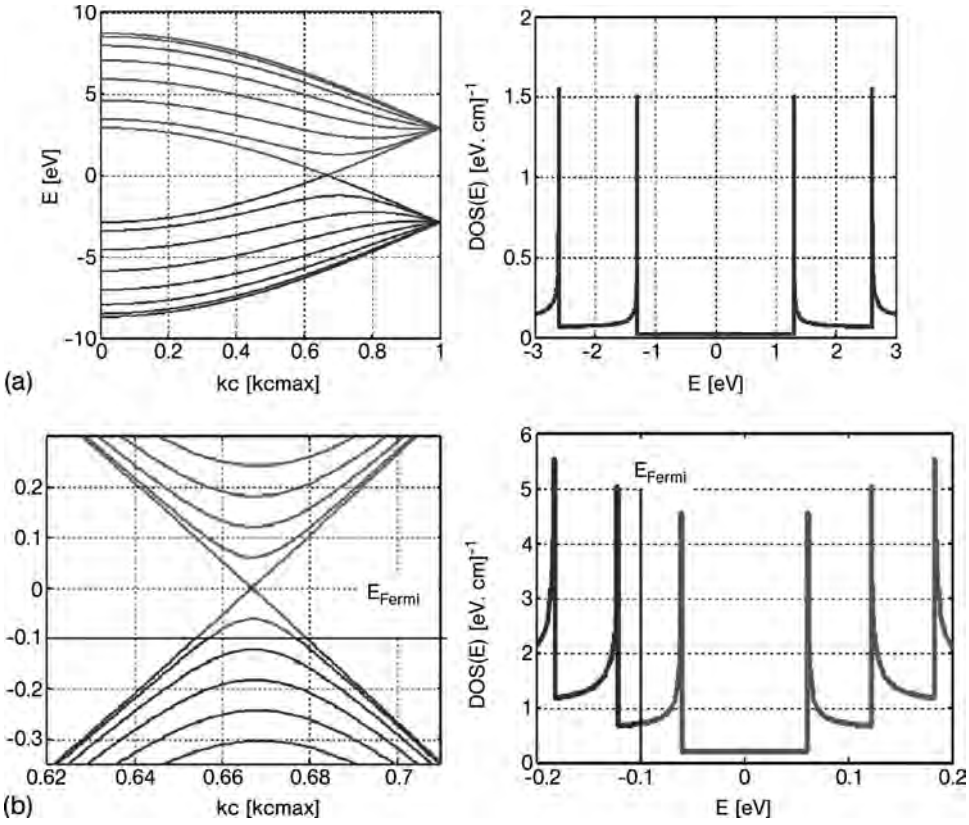


Figure 1.3 (a) The band structure of an $(n,m) = (7,7)$ metallic CNT of diameter 1 nm with the corresponding density of states. (b) The band structure of an $(n,m) = (150,150)$ metallic CNT of diameter ~20 nm with the corresponding density of states. Due to charge transfer doping the CNT is p-doped with additional density of states.

From the Landauer approach, the conductance G can be modeled by $G = 2e^2/hMT$, where M is the number of the allowed channels for the transport and T is the quantum mechanical transmission coefficient, which models the transmission probability. The factor 2 in the Landauer expression accounts for spin degeneracy and e^2/h is the fundamental Klitzing conductance of a single eigenstate. The transmission T can be influenced by defects in the CNT, nearby located trapped charges, and bending-induced strain. The transport channels are related to the k-value with which every electron is characterized in the band structure. Two bands cross at the Fermi level in the band structure of the metallic CNT, an example of which can be seen for an $(n,m) = (7,7)$ CNT in Figure 1.3.

The lowest possible resistance for an SWCNT including the contact resistance is ~6.5 kΩ because there are two bands with spin degeneracy and therefore $M = 2$. In a perfectly contacted, ballistic nanotube, half of the 6.5 kΩ resistance drops just at each of the two contacts to the nanotube. Additional contact resistance can occur

which is dependent on the nature of the contacts. The kind of metal and the way it is deposited are equally important as the size and the diameter of the contacts, but resistances close to the theoretical value can be obtained on a routine basis [8, 55].

For MWCNTs, each shell contributes according to its diameter and chirality to the density of states and therefore to the conductivity. In thicker shells, additional states may become populated by thermally activated carriers, because more energy levels are accessible, as can be seen in Figure 1.3b for the 20-nm diameter tube. The 20-nm CNT would even conduct well in the case of a semiconducting CNT because the band gap is small compared with the thermal energy.

MWCNTs almost always show metallic behavior and can be easily used in interconnect applications because of the guarantee of a metallic behavior. The number of participating channels in an MWCNT can be calculated for each case and an approximate method is discussed by Naeemi and Meindl [13].

For interconnect applications, the maximum conductivity should be achieved, which means that the number of conducting channels per unit cross-sectional area should be maximized. It is worth looking at the specific resistivity of SWCNT and MWCNTs, because this will indicate the quality of the various materials for interconnect applications. The low bias resistivity for SWCNTs and MWCNTs is depicted in Figure 1.4 and shows a peculiar dependence on the length of the nanotubes. For SWCNTs, the experimental values are plotted and calculated values are given for MWCNTs with two different diameters. The resistivity of the SWCNTs is calculated by the measured resistance at a given length for an effective area cross-section of $1\,nm^2$. The length dependence of the resistivity stems from the very large mean free path of the charge carriers, which is typically around 1 µm for SWCNTs. Making the SWCNT shorter than 1 µm does not reduce its overall resistance any further. Therefore, the resistivity increases sharply at short lengths of a few nanometers. SWCNTs exceeding 1 µm have an almost one order of magnitude better resistivity than copper and an SWCNT of length 100 nm still outpaces the resistivity

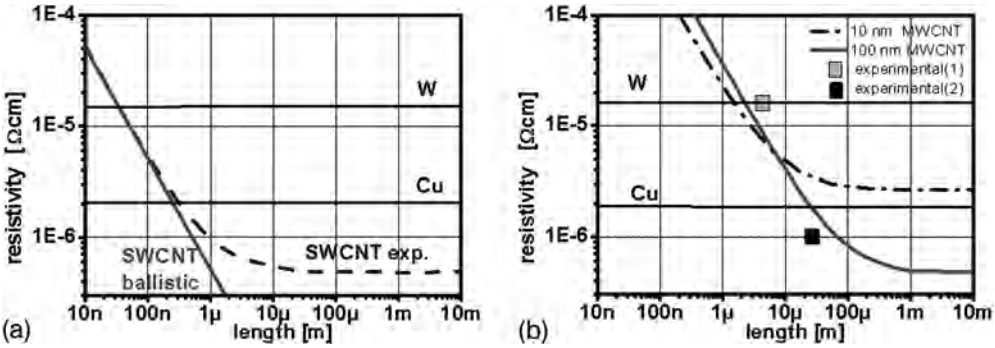


Figure 1.4 (a) The length dependent resistivity of SWCNTs based on experimental data compared with a pure ballistic SWCNT. As a reference, the values without size effects for W and Cu are indicated. (b) The resistivities of two different MWCNTs which differ in diameter are calculated according to Reference [13] for a shell filling factor of 0.5 and two experimental findings are incorporated, which demonstrate the achievable resistivities.

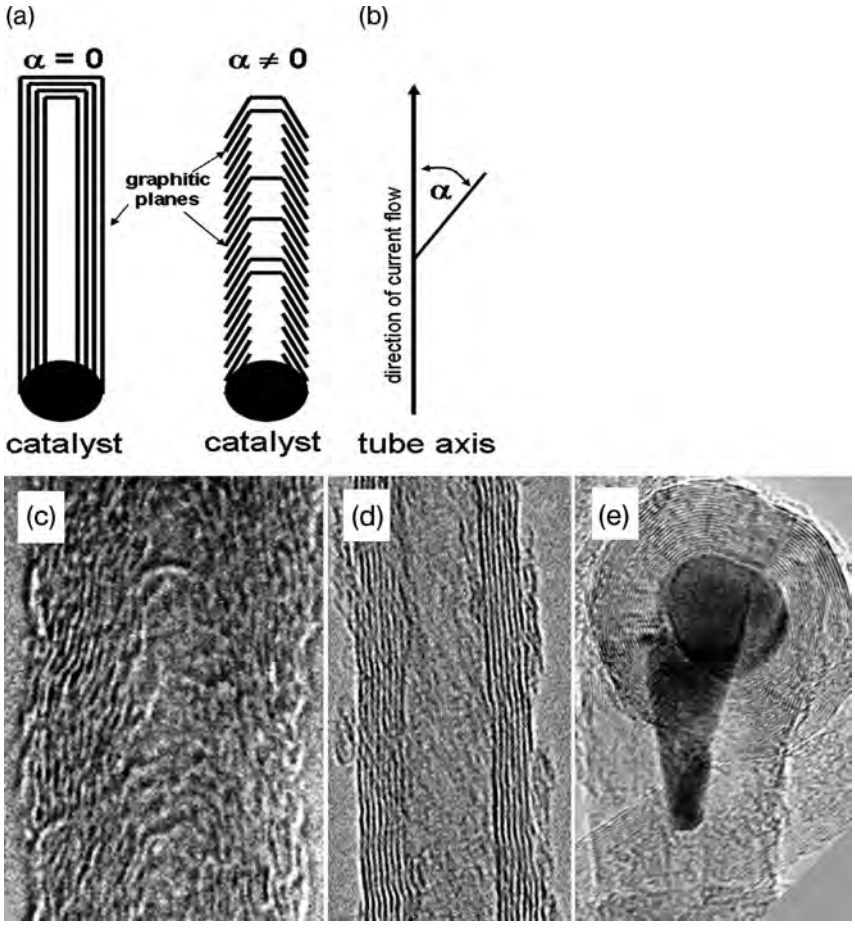


Figure 1.5 (a, b) Factors influencing the resistivity of a tube: number of shells and orientation of the graphitic planes. Ballistic transport can only occur for $\alpha = 0°$; for graphite $\rho_c = 1000\rho_a$ and the averaged resistivity can be expressed as $\rho(\alpha) = \rho_a \sin^2(90° - \alpha) + \rho_c \cos^2(90° - \alpha)$. (c–e) TEM images for CVD-grown MWCNTs. The interlayer distance is 0.34 nm. (c) A poor-quality tube grown at 450 °C with $\alpha \approx 18°$. (d) A high-quality tube with $\alpha \approx 0°$, but with only seven shells. (e) A high-quality tube with ~25 shells also showing the encapsulated catalyst particle.

of tungsten. The length-dependent resistance for SWCNTs can be approximated by ~6 kΩ μm^{-1} if the length exceeds the mean free path length. This explains the superior performance of metallic SWCNTs in interconnect applications.

The resistivity calculation of the MWCNTs in Figure 1.4 is based on a ratio of 0.5 for the inner to outer diameter of the MWCNT, because transmission electron microscopy, as shown in Figure 1.5d, demonstrates that most of the MWCNTs are not completely filled but have a hollow core, which does not contribute to the conductance. The conductivity values can vary by a factor of two for completely filled MWCNTs. A unique feature of the mean free path in metallic nanotube is

its proportionality to the diameter of the nanotube [14]. This is shown in Figure 1.4b, where a long 100-nm thick MWCNT can achieve the same resistivity as an SWCNT despite the fact that a huge portion of its diameter (~50 nm) is hollow and cannot contribute to the conductivity. The missing inner conducting shells are compensated by a larger mean free path of the thicker outer shells. Experimental data support this finding. Li et al. have contacted an MWCNT with spot welding, which almost assures contact with all shells [15]. The contacted MWCNT has a diameter of about 100 nm and a length of 25 μm with a resistance of 37 Ω. The resistivity obtain from these values is around 1 μΩ cm and close to the respective values in Figure 1.4b. A second example, also shown in Figure 1.4b, from de Pablo et al. [16], gives a value of 15 μΩ cm for a 4 μm long MWCNT of 40 nm diameter. Other experimental data often refer to situations where only the outer tube of a MWCNT is contacted and the contributions of the inner shells are not known in detail [17]. The outer shell is often corrupted by processing methods and does not perform adequately and therefore gives rise to irreproducible results. Furthermore, growth of CNTs with chemical vapor deposition (CVD), especially when supported by plasma, results often in misaligned shells, as indicated in Figure 1.5. Quasi-ballistic transport can only occur if the shells are strictly aligned in the direction of current flow. Any misalignment as shown in the TEM image of Figure 1.5c impairs the conductivity as the charge carriers have to tunnel from shell to shell. The conductance perpendicular to the shells is almost a factor of 1000 smaller than the in-graphene-plane conductance. A typical value for the resistivity of these more carbon fiber-like structures is in the region of 4 mΩ cm.

1.2.4 Doping of Multi-Walled Carbon Nanotubes

The diagram of the DOS of the CNTs in Figure 1.3 suggests the possibility of enhancing the conductivity of MWCNTs by doping the outer shell. Chemical doping of CNTs by charge transfer would shift the Fermi energy (E_F) of the nanotubes to a level with a higher DOS and, consequently, increase the conductivity. As the DOS is independent of the circumference of the CNT, it is much easier to achieve higher conductive channels for metallic MWCNTs than for metallic SWCNTs, for two reasons. First, the surface area for interaction with charge donors is larger for MWCNTs, and second, additional channels are energetically closer to the Fermi level for MWCNTs. Therefore, the doping of the MWCNTs with either an aryldiazonium salt or with an oxonium salt can reduce the resistance by 20% on average to values as low as 2.8 kΩ, as will be demonstrated below [18].

In the following, the as-deposited CNTs are compared with those doped by the deposition of various charge-transfer adsorbates. In addition, the chemical doping of two different qualities of MWCNTs, namely CNTs grown by CCVD and arc discharge fabricated MWCNTs are investigated [18].

The MWCNT samples were dispersed in a solution of 1% sodium dodecyl sulfate (SDS) and deposited on a silicon–silicon oxide substrate with cobalt microelectrodes with gap spacings ranging between several hundred nanometers and

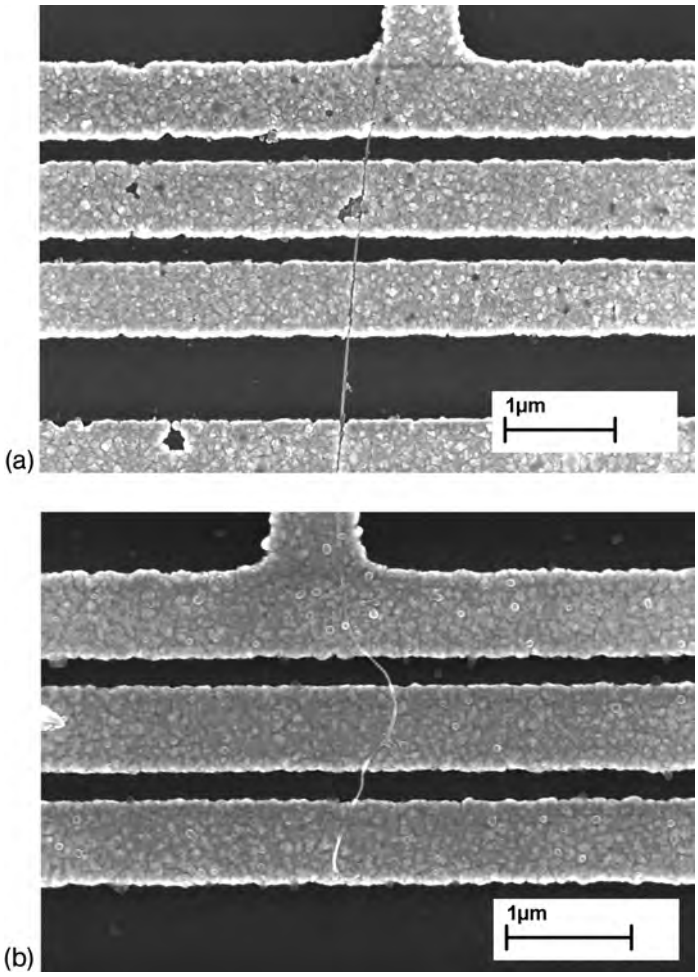


Figure 1.6 (a) Scanning electron microscope images of MWCNTs embedded in palladium contacts on a silicon oxide surface. The nanotubes shown in the images (a) were produced in an arc discharge, whereas those in the images (b) were generated using a CCVD process.

15 μm. The contact resistances were reduced by embedding the tubes in palladium using an electroless metal deposition process that has been described earlier [19, 20] and annealing at 400 °C in an argon atmosphere. Figure 1.6 shows samples of MWCNTs on cobalt electrodes made by arc discharge (a) and by CCVD (b). It can be seen that the CVD tubes have a number of kinks, whereas the arc discharge tubes appear very straight. This is ascribed to the higher density of defects in CCVD tubes and the misaligned shells as discussed in Figure 1.5. Figure 1.6 shows the contact regions between the CNTs and the metal electrodes after electroless palladium deposition.

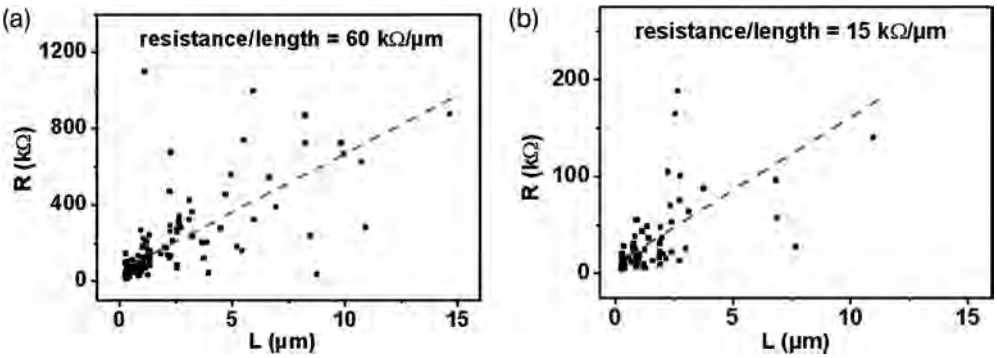


Figure 1.7 Two-point resistance measurements of (a) CCVD and (b) arc discharge CNTs of different lengths between palladium contacts. The CCVD produced CNTs display an intrinsic resistance that is four times higher than those produced by arc discharge [18].

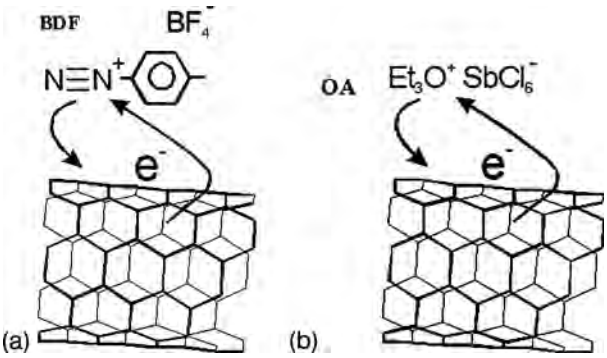


Figure 1.8 Schematic of the adsorbate doping of CNTs by electron extraction using 4-bromobenzenediazonium tetrafluoroborate (BDF) or triethyloxonium hexachloroantimonate (OA).

The two-point resistances of about 100 devices with different nanotube lengths were determined. The length dependence of the resistances is shown in Figure 1.7 for the CCVD- and arc discharge-produced tubes. As can be seen, the CCVD tubes show a significantly higher length-dependent or intrinsic resistance compared with the arc discharge tubes. This probably originates from a higher defect density due to the different growth conditions. Further, the average intrinsic resistances derived from four-point probe measurements turned out to be $60\,k\Omega\,\mu m^{-1}$ for the CCVD CNTs and $15\,k\Omega\,\mu m^{-1}$ for the CNTs produced by arc discharge. These values differ from two-point probe measurements due to scattering of electrons in the vicinity of the contacts and due to the inter-shell conductance in MWCNTs by the application of four microelectrodes [17].

The influence of chemical doping can be investigated by two approaches. One way that has been well investigated is chemical functionalization of CNTs by diazonium salts [21, 22]. As shown in Figure 1.8, 4-bromobenzenediazonium tetra-

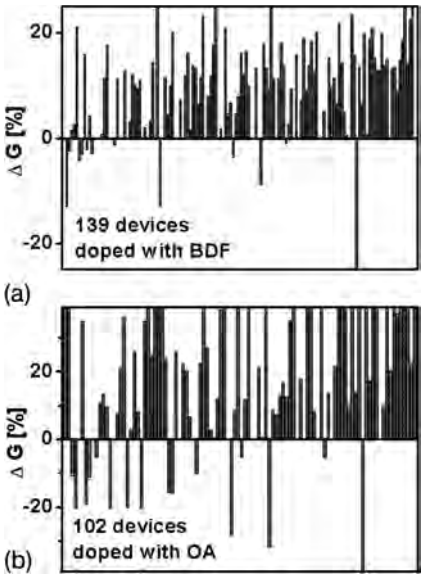


Figure 1.9 Percentage difference between the two point resistances of pristine and doped CNTs between palladium contacts after doping [18].

fluoroborate (BDF) [21, 22] extracts electrons from the CNT and releases nitrogen. The reaction is driven by the formation of a stabilized charge transfer complex and will lead to p-type doping of the CNTs. Another approach uses triethyloxonium hexachloroantimonate (OA) as a one-electron oxidant, thus leading to a similar doping state. The devices were treated with either a 5.5 mM solution of BDF in water for 10 min or with a 2.7 mM solution of OA in chlorobenzene for 12 h [23, 24]. After chemical modification, the samples were annealed at 100 °C in air. Both chemical reactions should lead to hole injection into the CNTs and will preferentially affect defects in the sidewalls of the CNTs. In addition, the conditions must be optimized so that no additional structural defects are introduced.

Two-point probe measurements of a large number of devices confirmed a statistical increase in the conductance of CNTs after chemical doping with either BDF or OA. As shown in Figure 1.9, more than 70% of the devices showed higher conductance after chemical doping than before. The conductance was found to improve by up to 20% on that of the initial state. The decrease in the conductance in some cases (less than 10% for BDF doping) is attributed to a destructive reaction with the outer shells [21]. As a result of the large diameter of the CNTs, and the corresponding separation of the states, there is no significant difference between metallic and semiconducting CNTs at room temperature. Thus, by optimization of the doping conditions it will be possible to reduce the amount of destruction. The reaction should preferentially lead to chemical adsorption and not to the formation of covalent bonds.

The highest conductivity was obtained for individual MWCNTs treated with OA, where about 20% of the tubes showed conductivity above the quantum

conductance limit ($G = 4e^2/h$) and a minimum resistance of about 3 kΩ. Finally, four-point probe measurements showed an average conduction increase of about 10%, which confirms the above results after consideration of the scattering effects and the smaller number of samples. The temperature stability has not been studied in detail, but seems to be limited to below 200 °C.

In conclusion, a chemical modification increases the conductivity of MWCNTs. The conductivity of an individual CNT can be more than twice as high as the quantum limit, indicating a shift of E_F and, thus, the activation of additional electronic states. The doping of the inner shells cannot be achieved with that method and intercalation approaches needs to be considered. However, the presented methods and results indicate a first approach to overcome the fundamental limitation of the conductivity of CNTs.

1.3 Carbon Nanotube Interconnects

The resistivity of various chip interconnects, with cross-sectional dimensions of the order of the mean free path of electrons (~40 nm in Cu at room temperature) in current and imminent technologies, is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of a highly resistive diffusion barrier layers. The resistivity increases further at higher temperatures (metal interconnect temperatures are above the typical device operating temperature of ~100 °C) due to temperature-dependent bulk resistivity and electron mean free path [25].

The rising Cu resistivity also leads to a significant rise in the metal temperature due to self-heating. This rise in the metal temperature is further exacerbated by decreasing thermal conductivity of low-*k* dielectrics and increasing current density (J) demands from interconnects. Since the electromigration lifetime of metal interconnects depends quadratically on J and exponentially on the metal temperature, all these trends of interconnect scaling lead to a growing threat to the reliability of future interconnects and severely limits their current-carrying capacity to below the requirements. While interconnect delay has always been a major concern, these reliability issues have become the driving force behind the search for alternative interconnect materials [25]. Carbon nanotubes, with their many attractive properties, are emerging as frontrunners in this search if their large-scale integration can be shown. In the following, the current status and possible applications will be discussed.

1.3.1 Fabrication and Integration Challenges for Carbon Nanotube Interconnects

The current state of the art of on-chip integration of CNTs focuses on the substitution of vertical interconnects (vias) for two reasons. First, vias carry the highest current densities and are prone to failure, hence the use of more reliable materials

such as CNTs would be a distinct advantage. Second, there is no convincing approach yet for growing dense CNT bundles of varying length parallel to the chip surface in two perpendicular directions. The only demonstration of CNT bundle growth in a horizontal direction (parallel to the silicon wafer surface) uses the fact that CNT bundles always tend to grow perpendicular to a surface [26, 27]. However, it requires challenging catalyst deposition techniques and various growth steps to provide a two-dimensional mesh of CNT bundles and therefore, it has not yet been accomplished. Horizontal alignment in two dimensions up to millimeters length has been achieved for small SWCNT bundles and single SWCNTs [28, 29]. The orientation of nanotubes is directly controlled by the direction of gas flow in the CVD system. The substrate needs to be rotated to acquire a different orientation of the CNTs. Other approaches such as electric field-induced alignment [30] or fluidic methods are not suited for large-scale integration [31].

The only viable solution for large-scale integration of CNTs seems to be to grow them directly in the place of use on the chip by CVD methods. This imposes the challenge of implementing a microelectronic-compatible manufacturing approach that guarantees an array of dense catalyst particles capable of growing a dense bundle of CNTs.

Achieving a good contact resistance in addition to a fertile catalyst is a non-trivial task because at the high temperatures required for CNT growth the catalyst particles tend to alloy with the underlying substrate to form a catalyst component which does not facilitate CNT growth, or the particles agglomerate to large particles by a high surface mobility at a given material combination. The problem has been solved in most cases by the introduction of a thin oxide layer below the catalyst particle. The oxide forms also in most metal substrates (Ta, Ti, TaN, TiN, Ni, Cu) unintentionally by oxidation of the surface under ambient conditions or by residual water contamination in the CVD chamber. The oxide layer in turn is responsible for bad contact resistance because the charge carriers have to tunnel through the insulating layer. Fortunately, both the oxide layer growth and the mobility of the catalyst on the oxide become lower at lower temperatures. By tailoring the amount and size of catalyst in combination with a suitable material combination, the temperature for CNT growth can be brought down to microelectronic-compatible temperatures of 400–600 °C. Another aspect influencing the contact resistance arises from the interaction of hydrocarbon gases with the substrate material. Depending on the temperatures and gases, considerable formation of carbide on the substrate may occur, which leads to degradation of the resistivity of the underlying contact material. A decrease in the process temperature is also beneficial for lower carbide formation.

Until recently, it was not possible to grow dense bundles of SWCNTs and all of the work has focused on the implementation of MWCNTs which can also guarantee a metallic behavior.

Currently, two different approaches to integrate CNTs have been investigated by four groups. Li et al. [32] proposed a so-called bottom-up approach, shown in Figure 1.10a. Here, the CNT via is grown on the metal layer 1 before the deposition of the inter-metal dielectric (IMD). Lithographically defined nickel spots act

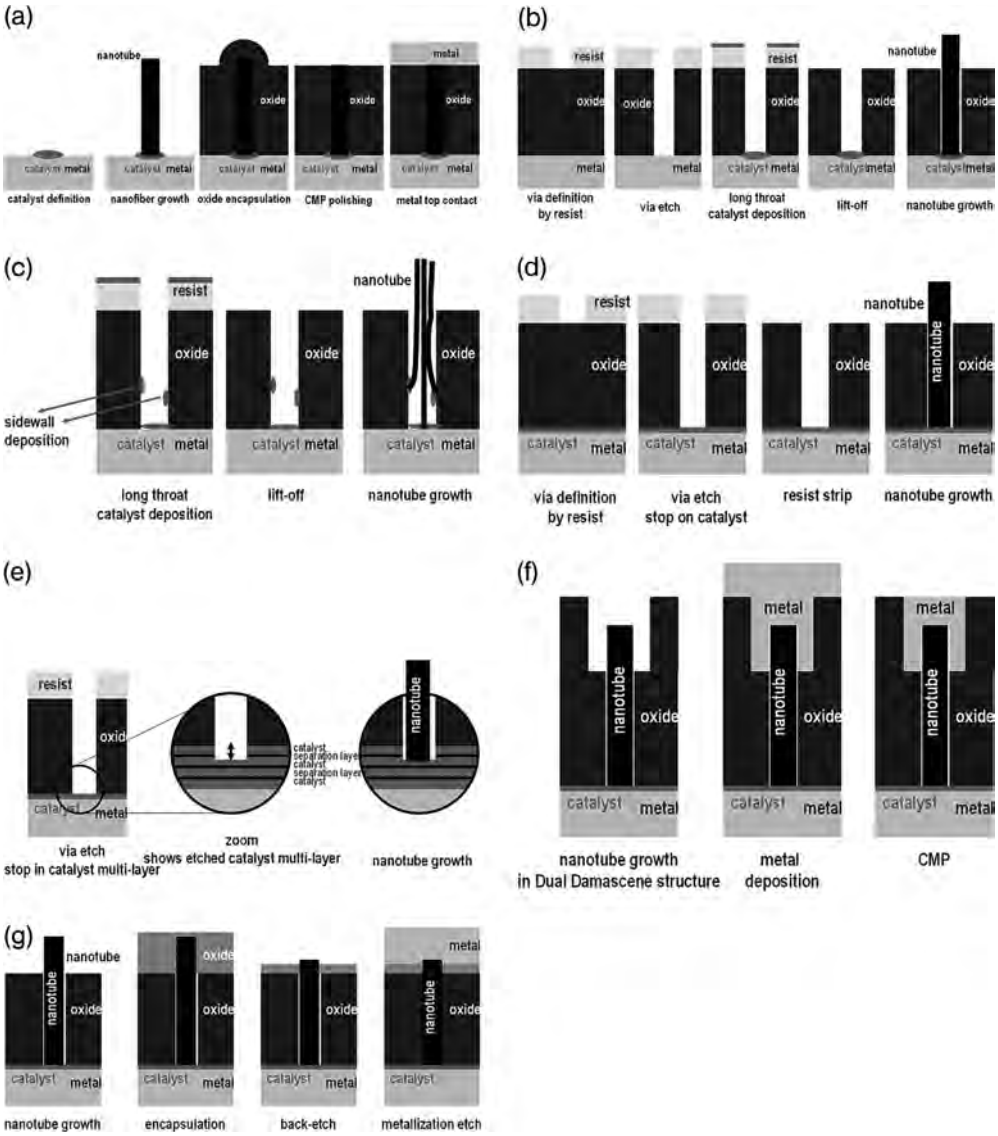
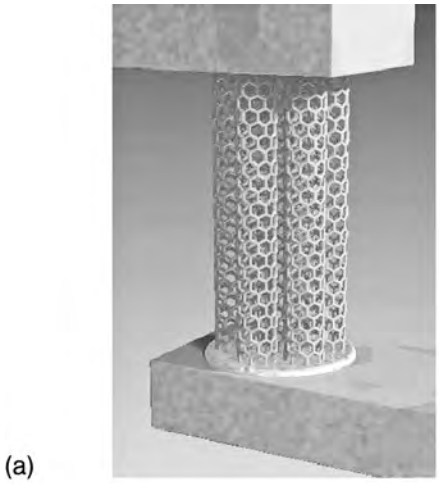


Figure 1.10 (a) Schematic of process sequence for bottom-up fabrication of CNT bundle vias [32]. (b) Schematic of process sequence for via first integration with catalyst deposition after via formation and lift-off process. (c) Problems of the lift-off approach due to sidewall deposition of the catalyst. (d) Schematic of process sequence for the buried catalyst approach. (e) The buried catalyst may consist of a multilayer to increase the yield [33]. (f) Top metallization can be employed by a conventional dual-damascene approach or with (g) conventional subtractive etching of the metallization.

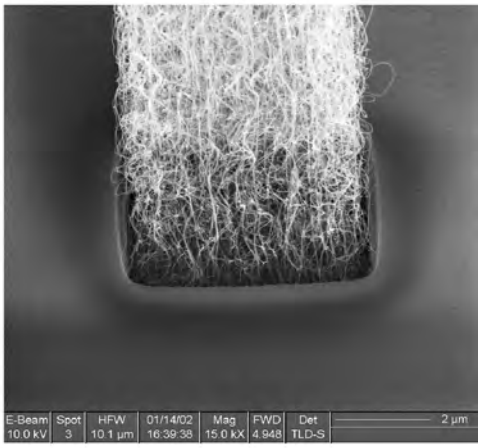
as catalyst particles, from where carbon fibers are grown. As a prerequisite, the fibers need to be aligned perpendicular to the surface. This is achieved by PECVD and an applied bias voltage, which aligns the fibers almost perpendicular to the wafer. Subsequently, SiO_2 is deposited and the wafer is planarized with chemical wafer polishing (CMP). The last step also opens the nanotube ends for contacts with metal layer 2. A high resistance of ~300 kΩ per CNT interconnect has been evaluated for that approach, which may be attributed to the imperfect structure of PECVD-grown MWCNTs [34]. The approach is especially suited for single MWCNT fillings because high-density growth cannot be demonstrated. Another drawback of this approach is that the fibers do not always grow at the selected location and are sometimes shifted and tilted from the projected locations. This makes lithographic overlay at minimum pitch size for further processing a nightmare. Therefore, the more conventional approach of etching the vias down to metal layer 1 and growing the CNTs in these vias has been pursued by semiconductor companies and first results have been presented by Kreupl et al. (Infineon) [35], Nihei et al. (Fujitsu) [36] and Choi et al. (Samsung) [37]. Figure 1.10 gives an overview of the different approaches that have been realized so far.

The straightforward method shown in Figure 1.10b deposits a thin catalyst layer by physical vapor deposition or related methods into the etched via. The catalyst on top of the resist needs to be removed carefully by a lift-off process from the chip surface so that only the catalyst in the vias remains. The lift-off process is not favored in semiconductor manufacturing because it creates a lot of particles which, in turn, are considered to be yield detractors. Another disadvantage for this approach is sketched in Figure 1.10c. Sidewall deposition of the catalyst occurs and leads to CNT growth from the sidewalls. These CNTs are not directly connected to the lower electrode and do not contribute proportionally to the conductivity of the CNT-filled via. The influence of these sidewall CNTs is strongest in high aspect ratio holes and almost negligible in low aspect ratio vias. Furthermore, shadowing of the sidewall in high aspect ratio holes reduces the amount of catalyst material which reaches the bottom. The main advantage of this approach is that there are fewer process steps after the catalyst deposition and this reduces degradation of the catalyst. In Figure 1.11, one of the first realized CNT vias is shown where a $4 \times 4\,\mu m$ wide via with Ta bottom electrode has been filled with CNTs. A lift-off approach together with an iron-based catalyst has been used to enable CNT growth [35].

A buried catalyst approach has been developed in order to omit the lift-off process. Figure 1.10d shows the basic schematics of the buried catalyst approach. The catalyst layer is deposited on top of the lower bottom electrode and embedded in the inter-metal dielectric. After lithographic definition of the vias in the resist, a fluorine-based dry etch process etches the oxide and stops on the catalyst layer. The etching process impairs the fertility of the catalyst layer due to polymer residues and implanted ions from the etch chemistry. Preconditioning steps and cleaning methods have to be applied to allow successful CNT growth. The etch stop on the 1–5 nm thin catalyst is challenging. Nihei et al. used a buried catalyst approach, where the dry etching of the vias has to stop on the thin Ni or Co catalyst



(a)



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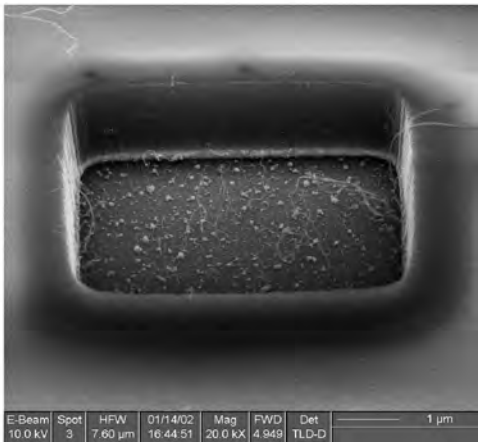


(c)

Figure 1.11 (a) Schematic view of a CNT interconnect. (b) One of the first CNT via interconnects before top electrode contacts are deposited. (c) Via with removed CNTs. Some catalyst particles can still be seen on the Ta bottom plate.

layer [36]. Arrays of MWCNTs have been grown in ~2-μm diameter vias by hot-filament CVD (HF-CVD). A resistance of ~134 kΩ per MWCNT has been achieved, a value which again can be attributed to the quality of the tubes grown by HF-CVD. The process has been improved to yield lower resistances [27], but careful interpretation of the data is needed, because the possibility of shorts induced by the top metal electrode deposition exists. Figure 1.10f and g detail how to make various top contacts in a dual-damascene or a conventional subtractive etching approach.

If the CNTs are not encapsulated after growth with oxide or spin-on-glass, the top metal deposition could lead to shorts induced by line-of-sight connections to the bottom contact during sputtering. This would yield a better resistivity because a metal–CNT composite would give a much better value than an oxide–CNT composite. In the work of Kreupl et al. [35], Li et al. [32] and Choi et al. [37], oxide encapsulation was used to ensure that only the contribution of the CNTs is evaluated.

A multilayer buried catalyst approach, as shown in Figure 1.10e, has been developed to increase the CNT growth yield after the via etch [33, 38]. The metal multilayer system includes a high-melting metal layer, a metal separating layer, a catalyst layer and a final metal separating layer. The high-melting metal layer is composed of at least one of tantalum, molybdenum and tungsten. The metal separating layer is composed of aluminum, gold or silver. The catalyst layer is composed of at least one of iron, cobalt, nickel, yttrium, titanium, platinum and palladium or a combination thereof. The final metal separating layer, which is arranged below the inter-metal dielectric (oxide), is composed of aluminum. Each of the layers is around 1 nm thick. With this approach, end-of-the-roadmap-sized CNT interconnects of diameter 20 nm have been fabricated [38]. Figure 1.12 details the results, where a lowest resistance of 8 kΩ has been achieved for a completely integrated carbon nanotube via.

Until recently, it was difficult to grow bundles of SWCNTs for interconnects because the fertility of the catalyst particles for SWCNT growth was low. Although progress has been made recently in growing bundles of SWCNTs by addition of water or oxygen to increase the fertility of the growth catalyst [39, 40], this approach has not yet been applied to the fabrication of interconnects. Moreover, the lack of control of chirality means that it is difficult to ensure that the SWCNTs forming a bundle are all metallic. As mentioned in the Introduction, more than two-thirds of all SWCNTs are semiconducting. Therefore, it will be very challenging to obtain densely packed bundles of metallic SWCNTs. One viable method would probably be to use double-walled CNTs (DWCNTs) as there are indications that the plurality of DWCNTs show metallic behavior with considerable DOS at the Fermi level [41, 42]. The orbital mixing in thin-diameter CNTs by neighboring shells leads to significant interlayer interactions and can cause semiconductor–metal transitions, which in turn can be employed for interconnect applications.

1.3.2 Application Areas for Multi-Walled Carbon Nanotubes

The useful competitive applications of MWCTs in microelectronic applications are determined by their length-dependent resistivity as shown in Figure 1.4b. The

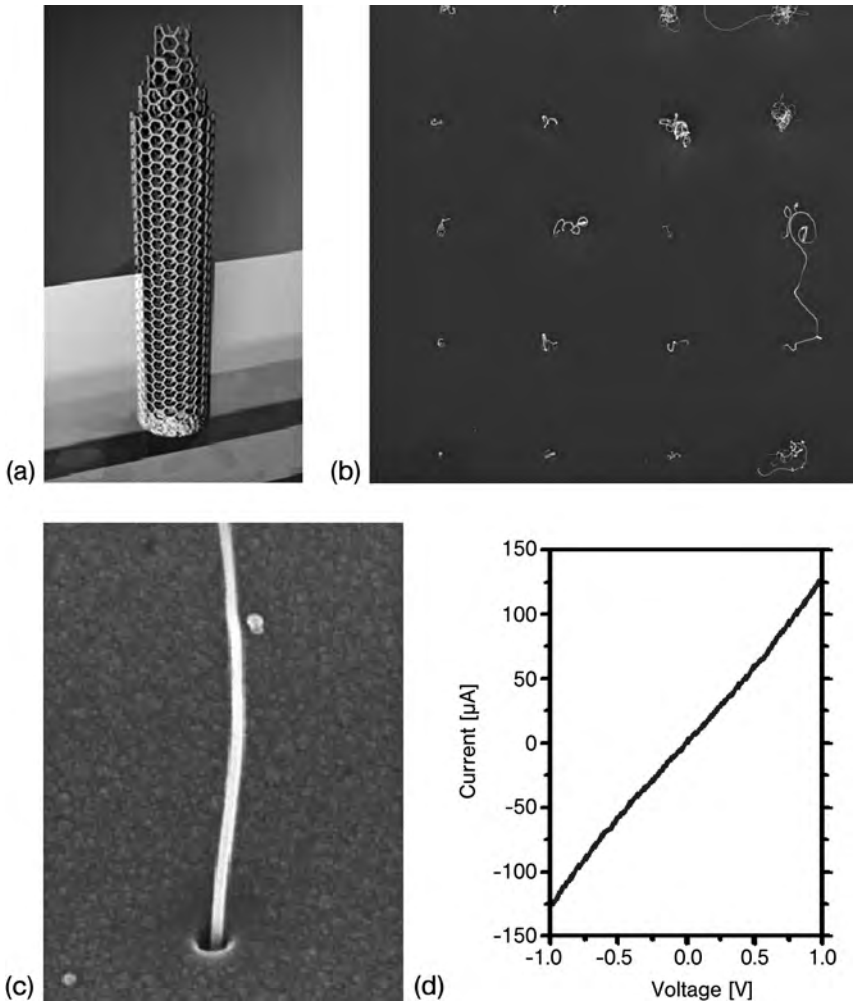


Figure 1.12 (a) Schematic view of the 20-nm diameter CNT interconnect. (b) Array of single MWCNTs protruding from the vias and demonstrating the high yield of the buried catalyst multilayer approach. (c) Single 20-nm diameter MWCNT protruding from a 100-nm deep via. (d) *I*(*V*) curve of a 20-nm CNT interconnect having a resistance of 8 kΩ.

competitive range starts at a length of 1–2 µm where MWCNTs already outperform tungsten. These might be applicable in typical high aspect ratio vias and contact holes which are usually filled with polysilicon or tungsten. It is worth noting that MWCNTs can compete with highly doped silicon at length scales below 100 nm as their resistivity is usually in the range 1–5 mΩ cm. However, contact resistances of the MWCNTs to the underlying contact needs to be taken into account. Other applications may include vias in DRAMs where the typical capacitor structure

height is in the region of 8 μm and higher and deep vias needs to be filled for contacting the lower structures. In this case, MWCNTs already approach the values for copper and are therefore more competitive. Longer on-chip interconnects are usually global wires which run in-plane of the chip surface, but this is an area where no CNT technology exists in terms of integration to compete with current copper or aluminum processes.

The high thermal conductivity combined with the mechanical strength make MWCNTs applicable for flip-chip bonding. An impressive example has been given by Iwai et al. [43], who successfully developed thermal and source bumps made of CNTs for flip-chip high-power amplifiers. The developed 15-μm long MWCNT bumps exhibit a thermal conductivity of $1400\,W\,m^{-1}\,K^{-1}$. A flip-chip AlGaN/GaN HEMT amplifier utilizing CNT bumps exhibits an output power of 39 dB at a frequency of 2.1 GHz without any degradation due to heat-up. Furthermore, the MCNT bumps reduced ground inductance and maintained RF gain up to very high frequencies.

To circumvent the high growth temperature and poor adhesion with the substrates Zhu et al. proposed a MWCNT transfer technology enabled by open-ended MWCNTs [44]. The process is featured with separation of MWCNT growth and device assembly. The hollow cavity of MWCNTs will allow the wicking of solders, such as Sn/Pb and Sn/Ag/Cu, due to capillary forces. As a result, interconnects of MWCNTs with metal electrodes by solders are possible and the limited wetting of solders on CNT films is eliminated [45].

In response to environmental legislation, the lead–tin alloys commonly used for soldering of chips will be replaced with lead-free alloys and electrically conductive adhesives. Lead-free alloys usually require higher reflow temperatures than the traditional lead–tin alloys, which can impact the assembly yields. Isotropic conductive adhesives are an alternative to solder reflow processing; however, they require up to 80 wt.% metal filler to achieve minimum electrical resistivity. The high loading content degrades the mechanical properties of the polymer matrix and reduces the reliability and assembly yields compared with soldered assemblies. MWCNTs make it possible to provide electrical conductivity for the polymer matrix while maintaining or even reinforcing the mechanical properties. Replacing the metal particles with carbon nanotubes in compositions has the potential benefits of using a low process temperature, being lead free, corrosion resistant and lightweight and having high electrical conductivity and high mechanical strength. Li and Lumpp recently investigated the properties of conductive adhesives with 50-μm long MWCNTs [46]. Their findings show that MWCNT-filled epoxy retains its shear strength (in contrast to metal-filled epoxy) and can compete with the electrical performance of metal-filled epoxy up to an evaluated frequency of 3 GHz.

1.3.3
Low-*k* Dielectrics with Carbon Nanotubes

Electrically insulating layers are required for many applications in semiconductor technology, in particular when forming integrated circuits in semiconductor

substrates. With ongoing miniaturization in silicon microelectronics, i.e. as the distance between adjacent interconnects decreases, a high coupling capacitance C results in particular if the mutually adjacent surfaces of the interconnects are large, i.e. if the interconnects run parallel to one another over a considerable length in the integrated circuit. By contrast, the coupling capacitance of two lines which cross one another is lower. Problems with coupling capacitances are intensified by the ongoing miniaturization of integrated circuits. As the coupling capacitance increases, the propagation time of a signal in the electrical coupling means becomes ever longer, since this propagation time is determined by the product of resistance R and capacitance C (known as the "RC delay"). On the other hand, the energy uptake for a chip is simply proportional to the capacitances involved and can be reduced considerably if the participating capacitances are diminished.

It is possible to reduce a coupling capacitance if the relative dielectric constant k of the insulating material is reduced. It is therefore attempted to use materials with a low relative dielectric constant (known as "low-k materials") as materials for insulation layers in integrated circuits.

Amorphous silicon dioxide with a relative dielectric constant of approximately 4.0 is often used as dielectric for electrically insulating metallic interconnects from one another. It is possible to reduce further the dielectric constant of a material for an electrically insulating layer if silicon oxide material which additionally contains fluorine, hydrogen or alkyl groups (in particular CH groups) is used for this purpose. This makes it possible to reduce the relative dielectric constant to as little as 2.5. Furthermore, organic materials, in particular polymers or PBO (polybenzoxazole), are used to achieve relative dielectric constants of 2.7. It is also possible for the "low-k materials" used to be materials based on silicon, such as a silicon–oxygen–fluorine compound, a silicon–carbon–oxygen–hydrogen compound, hydrogen silsesquioxane (HSQ) or methyl silsesquioxane (MSQ).

The relative dielectric constant of electrically insulating layers can be reduced further by introducing cavities into the "low-k material". The k value of the porous material is reduced further as a function of the proportion of the volume formed by the cavities or pores.

It can be seen from Figure 1.13a that the higher the proportion of the volume formed by cavities, the greater is the extent to which the k value in a porous material is reduced compared with the k value in a homogeneous material. The dependent relationship between the effective k value and the pore cross-sectional area is shown in a semilogarithmic illustration for different pore shapes and pore geometries in Figure 1.13b. The simulation calculations demonstrate that the effective k value decreases to a greater extent with the pores oriented perpendicular to an electric field than in the case of a parallel orientation between the direction in which the pores run and the electric field vector.

If elongate and oriented pores are used, it is possible to reduce significantly the effective k value without increasing the proportion of the volume which is made up of the pores. With the same proportion of pores by volume, a reduction of 13% is achieved with a pore aspect ratio of 4 : 1 and a reduction of 20% is achieved with a pore aspect ratio of 24 : 1. If the pores are randomly oriented, there is no

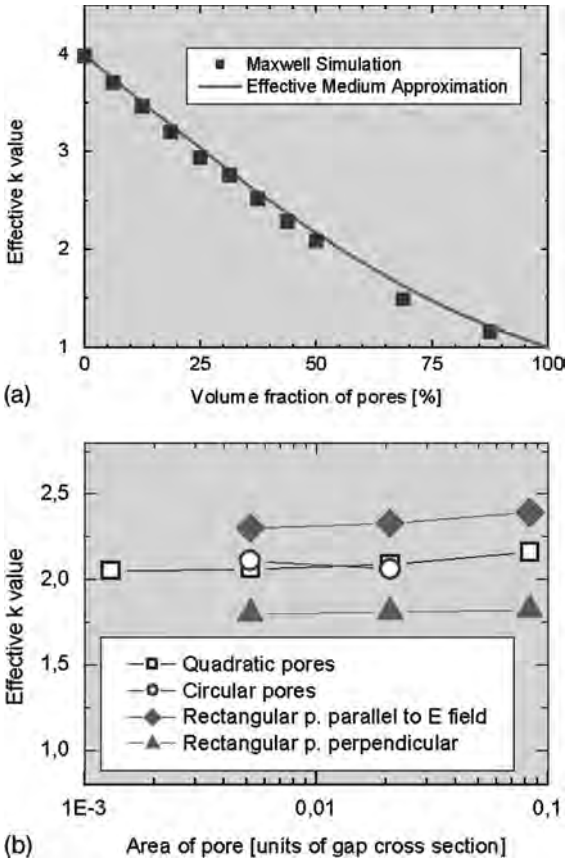


Figure 1.13 (a) Effective *k* value for silicon oxide depending on the volume fraction of the pores [47, 48]. (b) Effective *k* value with volume fraction of 50% in silicon dioxide for different pore sizes and orientations. Pores aligned perpendicular to the electric fields have the lowest effective *k* [47, 48].

advantage over round pores (aspect ratio 1 : 1). In this case, the same mean *k* value is obtained.

Nanotubes can be used to introducing elongate, oriented pores into a dielectric in order to reduce the effective *k* value of a dielectric. As shown in Figure 1.14a, a dense felt of CNTs needs to be grown on the desired surface – preferentially in the tip-growth mode. After infiltration of the CNT felt by silicon dioxide, the top oxide is removed by chemical mechanical polishing (CMP) and/or by a fluorine-based dry-etch process. This gives access to the CNTs again, which are subsequently removed by high-temperature oxidation and/or oxygen or hydrogen plasma. High-rate SiO_2 deposition by PECVD, as shown in Figure 1.14b, is not recommended, because only the outer surface becomes covered and the inner part

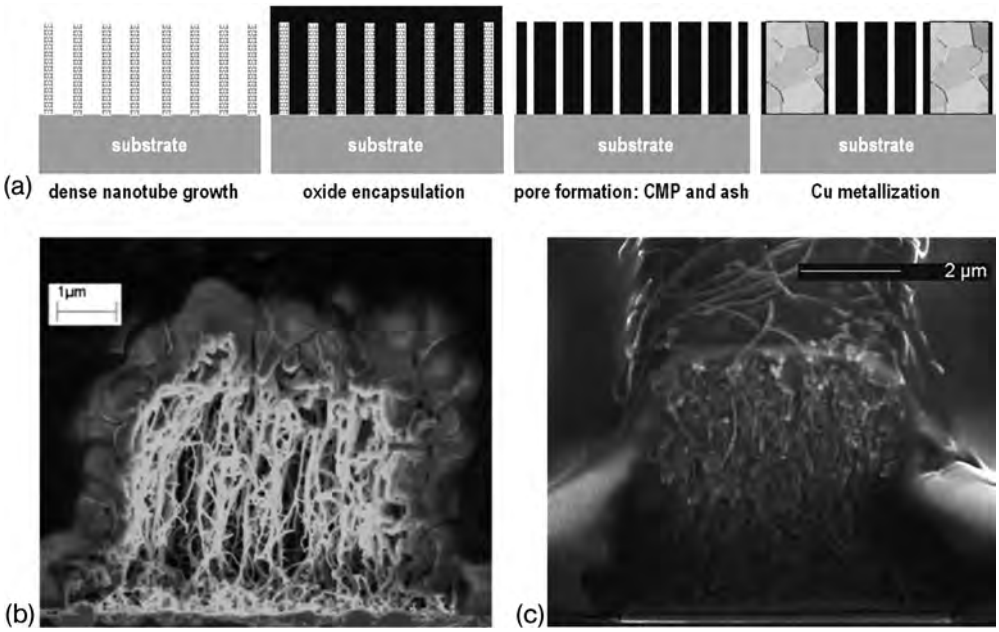


Figure 1.14 (a) Process for longitudinal pore formation with nanotubes as sacrificial structures. The CNTs are burned off with oxygen after encapsulation in oxide. This results in fine pores in the oxide and forms a low-*k* dielectric based on silicon dioxide. The metallization is then embedded in this porous oxide [48]. (b) SEM cross-section of CNT felt covered with SiO_2 deposited by high-rate PECVD deposition. (c) SEM cross-section of CNT felt infiltrated with a spin-on-glass.

is only covered at the initial deposition state. The use of spin-on-glasses (SOGs), as shown in Figure 1.14c, is most useful for achieving complete infiltration of the CNT film. In order to avoid crack formation, a combination of a thin layer of SiO_2 deposited by PECVD and subsequent SOG infiltration seems to work best. The SOG process parameters need to be optimized and the focus in the SOG process should be placed on initial oxide thickness, bake temperatures, cure temperatures and ramp rate.

Fabricating low-*k* dielectrics with CNTs as sacrificial structures is still in its infancy but holds promise to lower considerably the *k* values with aligned pores. Given the recent progress [49] in the density of grown CNTs, which yielded almost 10^{12} CNTs cm^{-2}, the approach may also be suited for advanced feature sizes.

1.3.4
Stretchable and Flexible Interconnects with Carbon Nanotubes

There are numerous potential applications where lightweight, flexible and stretchable conductors are needed. Protective packaging for electromagnetic shielding, transparent conductors for displays and photosensors, elongation and pressure

sensors, electronic textiles and skins and microelectrode arrays for brain and body signal recording would all benefit from flexible and bendable interconnects [50–52]. Normal metal interconnects fracture during deformation of the substrate by a few percent and the recently developed gold– polydimethylsiloxane (PDMS) interconnects [50] withstand unidirectional elongation of 10–15% but fail to be elongated in an arbitrary direction. In contrast, CNT-based stretchable interconnects can be elongated by 100% in an arbitrary direction.

In order to fabricate stretchable CNT interconnects, the desired structure is lithographically defined on a conventional silicon substrate as shown in Figure 1.15a. MWCTs are grown to a height of 50–500 µm perpendicular to the substrate. A liquid prepolymer is poured over the CNT structures and cured for 1 h at 60 °C to obtain a solid, flexible PDMS structure [53]. Subsequently the PDMS is peeled off the substrate, taking the lithographically defined CNT interconnect structure

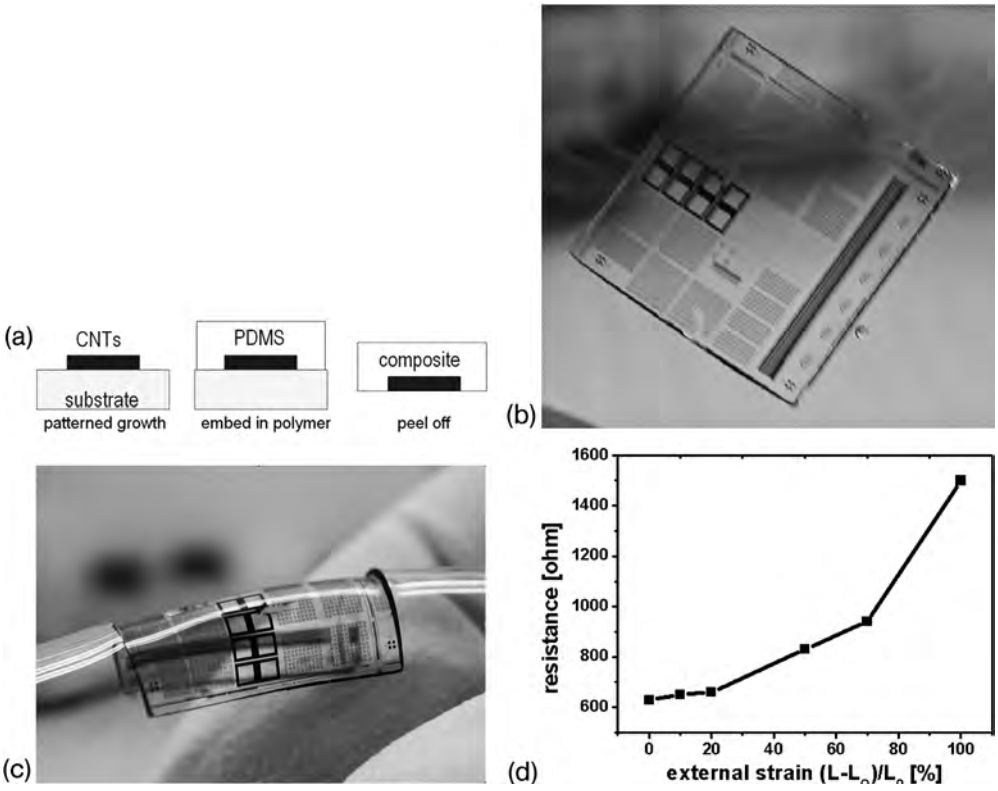


Figure 1.15 (a) Process for fabrication of stretchable integrated circuits with PMDS embedded CNTs. (b) CNT interconnect circuitry embedded in bendable PMDS. The size is roughly 2 × 2 cm (c) Picture demonstrating the flexibility of the created stretchable wiring. (d) Variation of electrical resistance of an embedded CNT stripe with applied tensile strain.

with it, as shown in Figure 1.15b and c. The structure is cured for additional 24 h at 60 °C before further investigations. PDMS is the most widely used silicon-based organic polymer and is particularly known for its elasticity. It is optically clear and is generally considered to be inert, non-toxic and non-flammable. The good wettability of PDMS on CNTs enables the PDMS to infiltrate effectively into the CNT felt and form a relatively defect-free composite film.

The electrical volume resistivity which can be achieved in these samples depends on the area density of the grown CNTs and amounts typically to 1–5 Ω cm. This is a fairly high value compared with ordinary metals (~μΩ cm) but can compete with resistances obtained for stretchable metal interconnects made of metal because the metal film needs to be as thin as 25 nm for this purpose [50]. The elongation-dependent resistance in these CNT composites is shown in Figure 1.15d. Up to an elongation of 20% the resistance increases almost linearly, which has also be confirmed by the results of Jung et al. [53]. Further elongation results in a parabolic increase in the resistance up to a maximum evaluated elongation of 100%. The composite withstands repeated elongation to 100% without major deterioration of its electrical performance. This may be related to the interwoven structure of the CNT felt in combination with the elasticity of PDMS.

The properties of CNT-based flexible interconnect outperform the unidirectional properties of metal-based stretchable interconnects in terms of resistance isotropy of the deformation direction and maximum achievable elongation.

1.4 Carbon Nanotube Devices

Many of the problems that silicon transistor technology is or will be confronted with do not exist for CNT transistors. The strictly one-dimensional transport in CNTs results in a reduced phase space, which allows almost ballistic transport and reduced scattering, especially at reduced gate length and low voltages. The direct band structure of CNTs is completely symmetric for hole and electron transport and allows for symmetrical devices and optically active elements. As there are no dangling bonds in CNTs, the use of high-*k* material as gate dielectrics is simple. In fact, the application of Ta_xO_y, Hf_xO_y and Al_xO_y as gate material has produced superior CNT transistors with low sub-threshold slopes and low hysteresis [54–58]. Both n-type and p-type conduction is possible, enabled by charge transfer doping or different work functions for gate, source or drain. CNTs are created in a "self-assembling" process and not by conventional top-down structuring methods. The scalability has been shown down to an 18-nm channel length recently [59]. CNTs are chemically inert and due to the covalent bonds mechanically very stable. Therefore, they would allow integration even in a high-temperature process. The device performance is considered to be more robust against process-induced fluctuations than their silicon counterpart [60]. Due to the extensive literature available on CNT transistors, the following discussion is focused primarily on some fundamentals and our own work.

1.4.1 Carbon Nanotube Transistors

Transistor devices made of semiconducting SWCNTs can be considered as a simple silicon CMOS field-effect transistors with the silicon material replaced by the carbon nanotube structure. The source and drain contacts in conventional silicon devices are made by highly doped silicon regions, which in turn are contacted by metals to form low-resistance contacts, as shown in Figure 1.16. Contacting a piece of silicon with metals leads to the formation of a Schottky contact and results in a Schottky barrier transistor if the source–drain areas have not been doped. The doping of the source–drain areas makes the Schottky barrier thin enough so that charge carriers can easily tunnel through the barrier and at an interface doping level of ~$2 \times 10^{21}\,cm^{-3}$, a contact resistance of the order of $10^{-7}\,\Omega\,cm^2$ should be achievable. Therefore, a low-resistance contact to a MOSFET-type transistor can be formed with metal contacts if the contact regions are highly doped.

The same approach can be applied to the contact formation of a nanotube transistor. The metal contacts can be formed on highly doped CNT regions, where the doping can also be introduced by electrostatic doping of a nearby gate voltage, or the intrinsically doped nanotube is contacted directly by the metal, as shown in Figure 1.16. In the latter case, a Schottky barrier field effect transistor (SBFET) is formed. The height of the Schottky barrier is basically determined by the differences in the work function of the CNT and the metal contact. Therefore, the Schottky barrier can be considerably reduced and a quasi-MOSFET transport behavior established if the right work function material is chosen. For a typical CNT, the mid-gap work function is 4.5 eV. High work function materials such as Au, Pt and Pd with work function values of around 5.1 eV give almost ohmic contacts to CNTs with a band gap of 0.8–0.6 eV [8]. The use of aluminum contacts leads to n-type transistors because Al has a work-function of ~4.2 eV [8, 57]. Titanium contacts lead to the formation of SBFETs despite the fact that Ti has a work

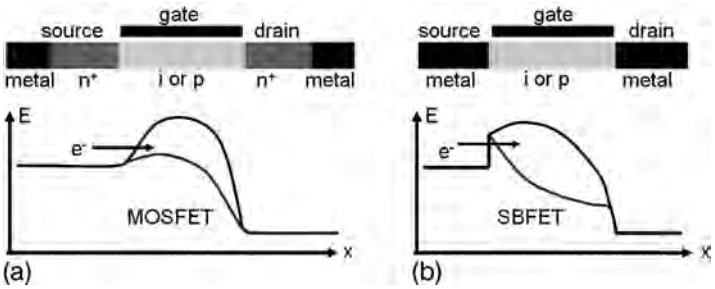
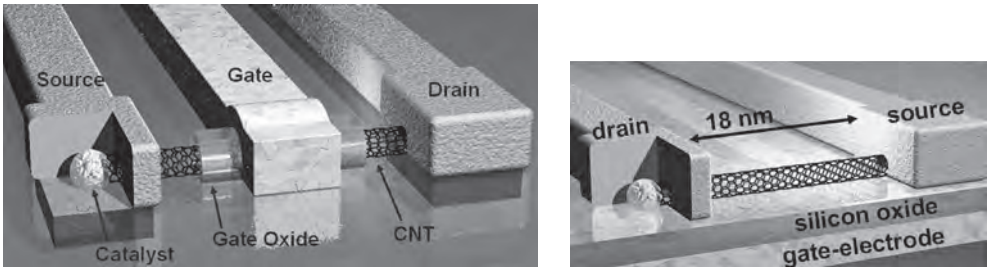


Figure 1.16 Schematic for MOSFET-type (a) and Schottky barrier-type (b) transistor. The energy diagram shows the conduction band in the off-state (black) and in the on-state (gray) of the transistors. Charge carrier conduction is by emission over the barrier for the MOSFET-type transistor. The current flow for the SBFET is controlled by the tunneling current through the Schottky barrier. The schematic is applicable to silicon and carbon nanotube transistors.

function of ~4.3 eV. The interface reaction at the contact leads almost always to the formation of TiC, which has a CNT mid-gap work function of ~4.5 eV. Interface design, cleanness, temperature treatment and the way in which the metal is deposited account for the quality of the contact [57]. Titanium contacts to nanotube transistors lead to ambipolar behavior of the transistor in the gate voltage-dependent conductance. The ambipolar behavior is characterized by hole *and* electron transport in the channel depending on the polarity of the gate voltage. The on/off ratio of the current is severely affected by the ambipolar behavior, which therefore should be avoided in logic devices. Exceptions to this are optoelectronic applications of CNTs where the injection of electrons and holes is mandatory [54] and the intentionally created carbon nanotube Schottky diodes, which are fabricated by contacting one end of a SWCNT by a high work function metal and the other by a low work-function metal.

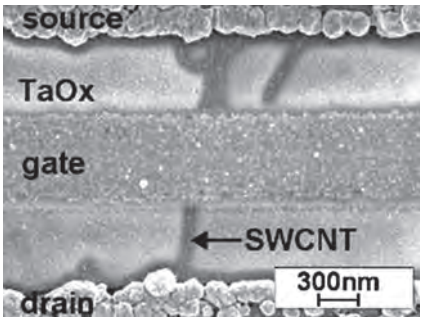
The formation of the gate stack in CNT devices is of the utmost importance and should be discussed next. The threshold voltage and performance are influenced by the structure and choice of the gate oxide and metal gate. Two implementations of the gate can be envisioned, as indicated in Figure 1.17. The natural and first approach was the bottom-gate or back-gate approach, where an oxidized silicon substrate can be used and the CNT, source and drain contacts are formed on top of it. The whole Si substrate is then acting as a gate electrode. Another approach is the top-gate approach, also shown in Figure 1.17. Here, the nanotubes are covered with the gate dielectric prior the top metal-gate deposition. In the following, it will be shown that a combination of top and bottom gates achieves the best performance.

The capacitance of the gate is a critical issue for future high-performance transistors. A high-*k* dielectric is, therefore, unavoidable since the thickness of a silicon oxide or an oxy-nitride gate dielectric cannot be reduced below a certain value without causing an intolerable increase in the gate leakage by direct tunneling. In

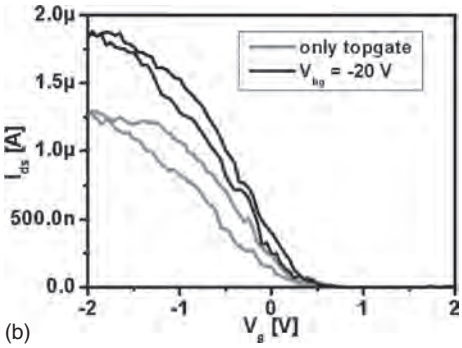


(a) (b)

Figure 1.17 Schematic of two different gate contacts for nanotube transistor. A top-gate is shown on the image in (a), where a gate dielectric needs to be deposited on the CNT before the metal gate is formed. A cross-section through a bottom-gate (back-gate) device where the CNT is grown on top of the silicon oxide and the gate-electrode is depicted on the image in (b).



(a)



(b)

Figure 1.18 (a) SEM image showing a CNTFET with a Ta_xO_y high-*k* dielectric. The tantalum oxide gate dielectric is ~4 nm thick [55]. The gate electrode has been deposited by evaporation of Al and the source–drain contacts improved by electroless Pd deposition. The curves in (b) compare the top-gate measurements with Ta_xO_y dielectric at floating back-gate or with back-gate voltage set to –20 V [55]. The gate-voltage sweep is from +2 to –2 V and back to +2 V and induces some hysteresis due to trapped charges near the nanotube.

addition, encapsulation of nanotubes is necessary in order to protect the dopants from desorption and to allow further integration. Therefore, it is necessary to evaluate different processes and high-*k* materials for the encapsulation of nanotubes. While the application of high-*k* stacks to silicon transistors is still cumbersome due to severe mobility degradation of the Si device, the use of high-*k* dielectrics for CNT transistors is relatively easy. A "poor man's" atomic layer deposition (ALD) process has been developed to deposit high-*k* Ta_xO_y dielectric on the CNT [55]. About 3–5 nm of Ta_xO_y is deposited during each cycle of the dip-coating process. Since no high-temperature anneal was performed, it has to be assumed that instead of Ta_2O_5 a non-stoichiometric Ta_xO_y is obtained.

Figure 1.18 shows an SEM image of CNT transistor with Al top gate, Ta_xO_y dielectric and Pd source/drain contacts. The difference in the on-current, shown in Figure 1.18b, is caused by enhanced transmission through the Schottky barrier. If a negative back gate voltage is applied, the Schottky barriers at the contacts are made more transparent for the tunneling of holes. This reduces the series resistances originating from the Schottky barriers and, therefore, decreases the on-resistances.

The scaling properties of every rival technology to silicon need to be explicitly demonstrated before the new technique can be taken seriously. And although CNT transistors have already shown their superior performance at gate lengths above 100 nm, the key question of how they will perform at very short gates has not been addressed until recently. As the Schottky barriers at the contacts play a major role, as discussed above, their influence on the device scaling might become stronger when both depletion width interact at short gate lengths. Therefore, short channel nanotube transistors with gate length down to 18 nm have been fabricated successfully in a back-gate geometry, such as that shown in Figure 1.17b, with

different source-drain contact materials [59]. The SEM image in Figure 1.19 shows a top view image of an 18-nm channel length nanotube transistor contacted with Pd contacts. The highly doped silicon substrate is acting as a gate electrode and the nanotube resides on a 12-nm thick silicon dioxide gate dielectric as shown in Figure 1.17b. The diameters of the CVD-grown CNTs are in the range 0.7–1.1 nm, yielding reasonable band gaps in the range 0.8–1.3 eV, which, in turn, are able to suppress ambipolar switching. In fact, Figure 1.19b details the drain–source current of the 18-nm transistor with Pd source–drain contacts as the gate voltage is swept from –5 to +5 V.

The device delivers a record 15 μA of current at a mere 0.4 V source–drain voltage and no current saturation can be seen in the logarithmic transfer curve as the gate voltage is increased to more negative values. Apparently, no ambipolar behavior can be seen at positive gate voltages, which is in striking contrast to the logarithmic transfer curve of the device with Ti source–drain contacts, shown in Figure 1.19c.

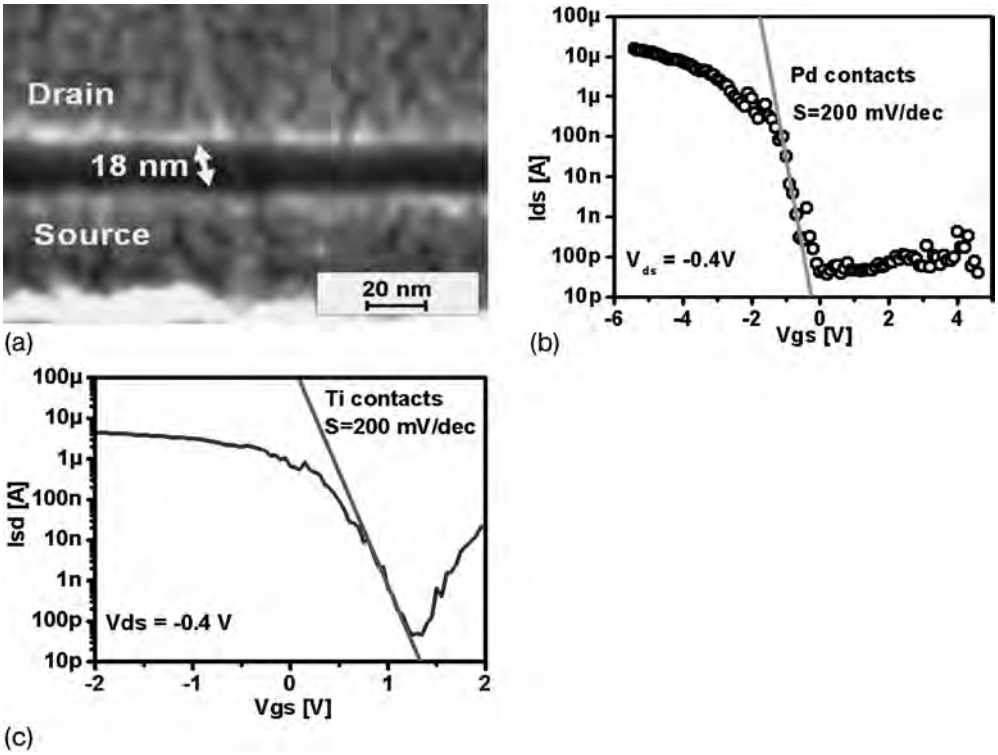


Figure 1.19 (a) SEM image showing the shortest nanotube transistor to date with a channel length of only 18 nm and Pd source–drain contacts [59]. (b) The logarithmic transfer curve of the device with Pd contacts shows no ambipolar behavior and has a record current of 15 μA. (c) The logarithmic transfer curve of a 20-nm gate length device with Ti contacts demonstrates lower on-currents due to the higher Schottky barriers for holes and ambipolar behavior due to lower Schottky barriers for electrons.

Here, a device with a slightly larger gate length of ~20 nm and with Ti drain–source contacts exhibits current saturation at a gate voltage of only 2 V and considerable ambipolar behavior, indicated by the current increase at positive gate voltages. The current amounts only to 5 μA at an applied voltage of 0.4 V – only one-third of the value of the device with Pd contacts. This is due to the different Schottky barriers for holes and electrons induced by the varying work functions of titanium and palladium. It also demonstrates that the threshold voltage of the devices can be shifted by using different metal contacts. The minimum current is achieved at $V_{gate} \approx 0$ V for Pd and at $V_{gate} \approx 1.3$ V for Ti.

The sub-threshold slope S, which is a measure of how many decades of current can be reduced by a change in gate voltage and indicates how fast a device could be switched off, is around 200 mV per decade for both devices. This is almost a factor of three higher than the theoretical limit of ~70 mV per decade. The deviation can be attributed to the "bad" electrostatic design of the device, where the gate electrode is 12 nm away from the channel and the source–drain distance of ~20 nm shields the influence of the gate. In fact, devices from this batch with 360 nm channel length exhibits a sub-threshold slope of around 80 mV per decade, which is close to the ideal value.

The tremendous progress in device performance can only be judged if a thorough benchmark, as suggested by Chau et al. [61], is performed. Although a complete benchmark is out of reach, but has been tackled theoretically [60], one can at least address one important metric of it: the intrinsic speed versus gate length is measured by the CV/I metric and is characteristic for the device speed. For the 18-nm CNT device, the insulator capacitance is 0.4 pF cm^{-1} and the quantum capacitance which accounts for the finite DOS in nanoscale systems [8] is 4 pF cm^{-1}. Given the current of 15 μA at 0.4 V, a device speed ($t = CV/I$) of 18 fs is evaluated for this short-channel CNT device. This value is almost two orders of magnitude lower than what has been achieved with silicon devices ($t \approx 1$ ps) of similar gate length. Calculations of power consumptions for various digital circuits made of scaled nanotube device suggest a similar improvement for the dynamic and static behavior [60].

1.4.2
Carbon Nanotube Diodes

Nanotube diodes can be fabricated as Schottky diodes or as pn-diodes as is the case with silicon. For state-of-the-art Schottky diodes used as detectors at frequencies above a few hundred gigahertz, the parasitic capacitances and the resistances associated with low electron mobilities limit the achievable sensitivity. The performance of such a detector falls off exponentially with frequency roughly above 400 GHz [62]. Moreover, when used as frequency multipliers, state-of-the-art solid-state Schottky diodes exhibit low efficiencies, generally putting out only microwatts of power at frequencies up to 2 THz. The shortcomings of the state-of-the-art solid-state Schottky diodes can be overcome by Schottky diodes based on carbon nanotubes. Because of the narrowness of nanotubes, Schottky diodes based on carbon

nanotubes have ultra-small junction areas and consequently junction capacitances of the order of 10^{-18} F, which translates to cutoff frequencies >5 THz, if several CNTs are paralleled to reduce the serial resistances [62, 63].

For the fabrication of pn-diodes, the nanotubes need to be doped. This can be done electrostatically by gating electrodes [64] or by charge transfer doping [65]. In classical devices, the dopants are impurity atoms in the bulk of the semiconductor. However, doping can also be achieved by an electron exchange between the semiconductor and dopants situated at its surface. For instance, the surface dopants have unoccupied molecular orbitals for electrons. If the energetically lowest of these orbitals is close to the valence band maximum of the semiconductor, an electron from the semiconductor can occupy this orbital. As a result, holes will form in the semiconductor and negative charge will be localized on the surface acceptors [66]. This happens for the usually p-doped nanotubes by oxygen absorption. UV irradiation of the CNT in an ultra-high vacuum environment results in desorption of water and oxygen and reveals mid-gap doped device properties. The absence of substitutional doping in nanotubes leads to reduced scattering rates and higher currents. Successful n-type doping has been achieved with functionalization of the SWCNTs with amine-rich polymers [65]. Figure 1.20 shows the completely altered characteristics of an SWNT transistor after doping with

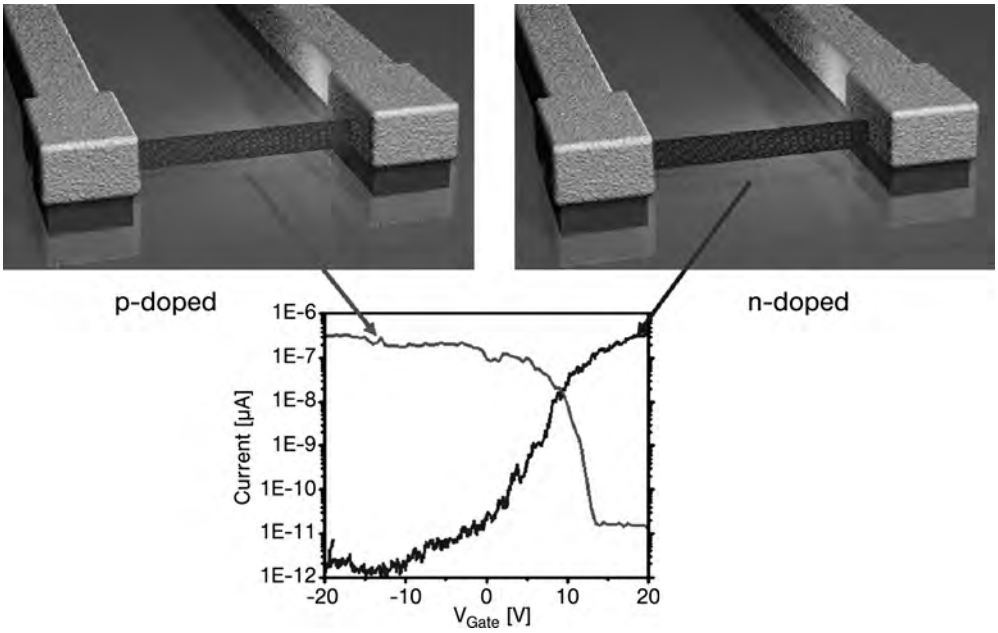


Figure 1.20 Both p- and n-doping of the same SWCNT device. The light gray curve is the current response of a p-doped device. After polymer amine doping the same device has an equally high on-current as the p-doped device indicating no additional charge scattering induced by this doping method.

polyethylenimine (PEI). The device was submerged in a 20 wt.% solution of PEI (average molecular weight 500 Da) in methanol for various times. Subsequently, the sample was rinsed with methanol and 2-propanol to remove non-specifically adsorbed PEI on the sample, leaving approximately a monolayer of PEI adsorbed on the device. A 1-min anneal at 50 °C evaporated the remaining solvent. Prior to PEI adsorption, the semiconducting SWNT exhibits p-type FET characteristics revealed by the decreasing current as a gate voltage is stepped to more positive values. The p-type behavior is due to adsorbed O_2 from the ambient. After PEI adsorption, the SWNT exhibits clear n-type FET characteristics. The current of the device increases when V_{gate} is stepped to more positive values (Figure 1.20). The current of the device is completely undisturbed, remaining at around 400 nA at 0.1 V source–drain voltage after n-doping. This is indicative of the low number of scattering centers introduced in the device by this doping scheme.

A nanotube pn-diode can be fabricated with this doping scheme by exposing only one half of a nanotube transistor channel to the polymer amine and leaving the other half p-doped, as shown in Figure 1.21. This is achieved by covering the CNT device with PMMA resist and exposing only a small area of the channel to

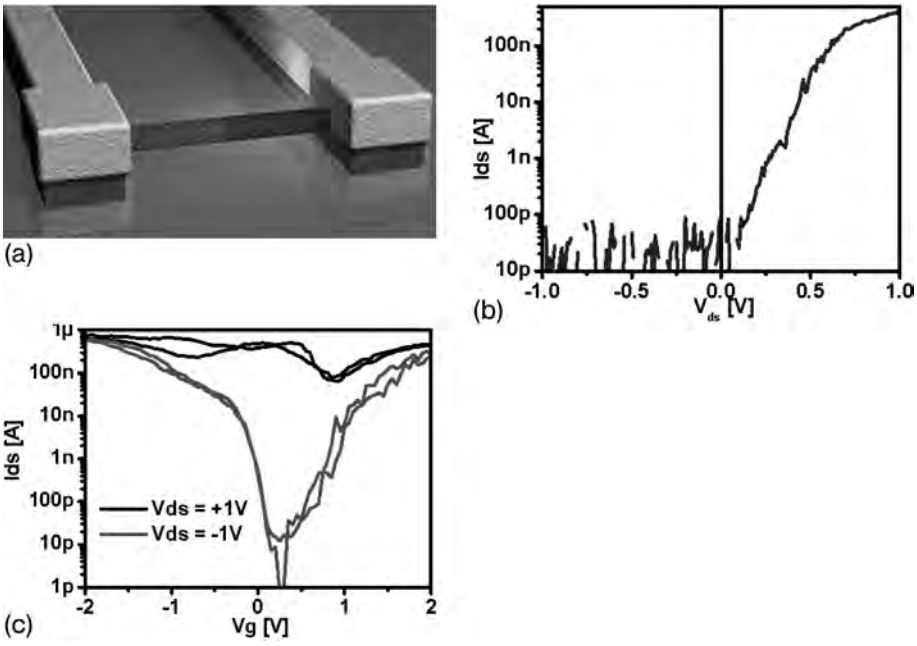


Figure 1.21 (a) Fabrication of a nanotube pn-diode by doping only half of a p-doped nanotube with polymer amine. (b) Diode characteristic of Pd-contacted ~1 µm long nanotube with one half of the channel being n-doped. (c) The gate voltage dependency of the nanotube pn-diode for forward and reverse-biased diode. A low hysteretic behavior can be observed during the gate voltage sweep.

the electron beam. After dissolution of the exposed PMMA area the device is locally n-doped with PEI. The diode-like current voltage characteristic is shown in Figure 1.21b. The off-current cannot be determined exactly and is limited by the measurement setup. However, an extrapolation from the positive exponential behavior would yield a value of ~2 pA. The forward current grows exponentially and is limited by the overall serial resistance of ~1 MΩ. If one applies the ordinary diode equation for the exponential forward current an ideality factor of the diode of $n \approx 2.1$ can be fitted to the curve. The device behaves like a gated diode if operated with the Si substrate as gate (Figure 1.21c). There is only a current modulation of one order of magnitude, if the diode is biased in the forward direction. The influence of the gate voltage is more pronounced in the reverse direction where the blocking behavior can be completely lifted by the application of a positive or negative gate voltage. The gated diode leads to new applications as it is able to detect and amplify small signals and sense amplifier circuits make use of the gated-diode unique property that allows precise distinction of small signals of low and high levels and the nonlinear boosting of only one of them [67].

1.4.3 Carbon Nanotube Power Transistors

Power switches are ubiquitous in use and need high blocking voltages and very low on-resistances. CNTs could even improve these power devices due to the following key advantages.

First, the nanotube acts as a current limiter, because the current in one single-walled CNT is limited to ~25 μA for CNT lengths exceeding 200 nm due to optical phonon emission [8]. This is in contrast to most silicon devices where overload leads to heating up and the avalanche effect, which destroy the device. Second, the specific resistivity of a long SWCNT is roughly one-tenth of that of copper wire, which means that one can in principle construct a power device with an on-resistance similar to a copper wire. The length of the nanotube should be proportional to the required operation voltage to guarantee proper operation and avoid impact ionization. A typical scaling factor would be ~200 nm V^{-1} and that includes already a safety margin for over-voltage protection. For normal Si-based devices the on-resistance is orders of magnitude higher and scales roughly with a power law of the form $V^{2.5}$ for the required blocking voltage. Third, the sustained current densities in CNTs are orders of magnitudes higher than in silicon or even copper. Therefore, CNTs would allow very compact low-loss power switches if thousands and millions could be paralleled to deliver an overall current up to some kA. Figure 1.22 gives an example of a vertical CNT power transistor and compares the obtainable values for on-resistance and maximum operating current densities with those of silicon. The on-resistance is already one order of magnitude better at a CNT density of only 100 μm^{-2}. The values in Figure 1.22b are calculated for two different CNT resistances. A 25 μm long CNT would have an on-resistance of ~200 kΩ and could sustain an operating voltage of 125 V. A 62 μm long CNT could be operated at 300 V and would have an on-resistance of ~500 kΩ. The current density

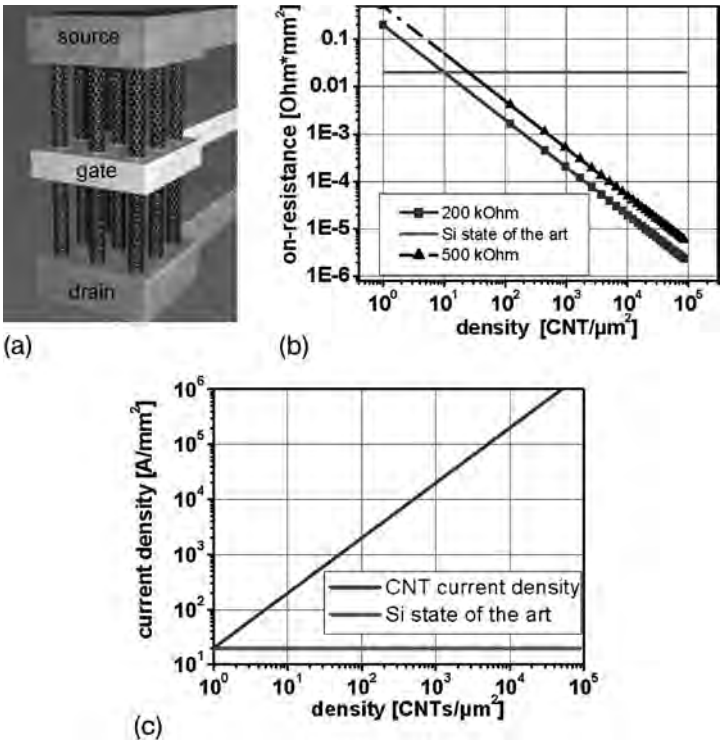


Figure 1.22 (a) Proposed vertical CNT power transistor, where many CNTs are paralleled. (b) The on-resistance of a CNT power transistor is plotted against the varying density of CNTs for two different resistances of the CNTs and compared with the silicon limit. (c) The maximum current density for varying CNT densities is compared to the silicon limit.

dependence in Figure 1.22c is calculated with a maximum current density of 20 µA for one CNT and gives the upper limit for the current. A low resistance design approach would restrict the current per nanotube to below 5 µA to ensure the operation in the linear current voltage regime.

From integration point of view, there would be the advantage that no precise control of the CNT arrangement on the nanometer scale would be required for a power switch that uses millions of paralleled CNTs. However, all metallic and small band gap CNTs need to be removed by either selective burning or functionalization.

The fabrication of a power switch which uses vertical SWCNTs, as shown in Figure 1.22a, is very challenging. Therefore, a planar prototype with horizontally aligned SWCNTs has been fabricated to support this idea [68]. The prototype with ~300 CNTs in parallel was able to deliver up to 2.4 mA at 1 V. The device, sketched in Figure 1.23, had enough power to operate small motors and LEDs. It consists of a metallic back gate layer covered with a thin layer of high dielectric constant

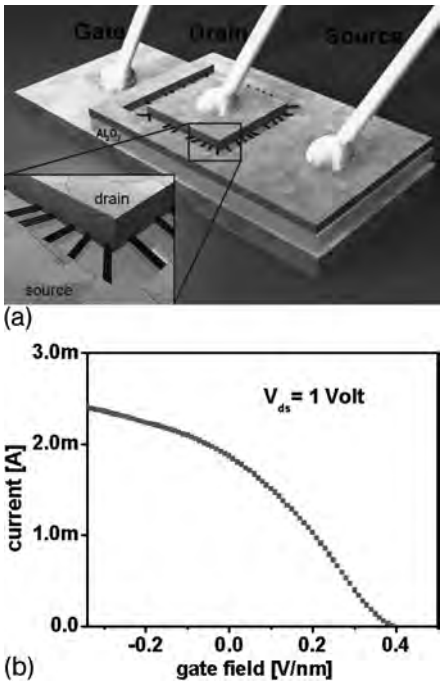


Figure 1.23 (a) Schematic of the first nanotube power transistor with 300 nanotubes operating in parallel. (b) The plot of the device current versus gate field demonstrates a current drive of 2.4 mA at 1 V source–drain bias voltage [68].

material on which a sparse layer of small diameter SWCNTs was grown. The palladium source and drain regions were defined on the SWCNT layer using electron beam lithography, metal deposition and lift-off. These transistors initially display an on/off ratio of about 3 due to the parallel connection of metallic and small band gap SWCNTs together with the semiconducting nanotubes. As progressively higher burn pulses are applied at high positive gate voltage, which turns the semiconducting CNTs off, first the metallic and then the small band gap SWCNTs are eliminated. The semiconducting tubes remain unaffected since they are switched off by the positive gate voltage. Using this method, on/off current ratios of over 1000 could be achieved. Despite the relatively modest performance of this transistor, it demonstrates that high current devices can be created by the parallel connection of many SWCNTs.

In order to investigate the possible performance of horizontally aligned nanotube power switches, an interdigital structure, as shown in Figure 1.24, can be considered. Here, the surface of a substrate is covered with aligned nanotubes and an interdigital metal contact structure is formed on the nanotubes for source and drain contacts. In this example, a distance of 1 μm is assumed, which translates to an operating voltage of 5 V. The achievable current densities (b) and on-resistances (c) are plotted in Figure 1.24 for various CNT packing densities. For a reasonable 3 μA per CNT and a packing density of 50 CNTs per micrometer, the

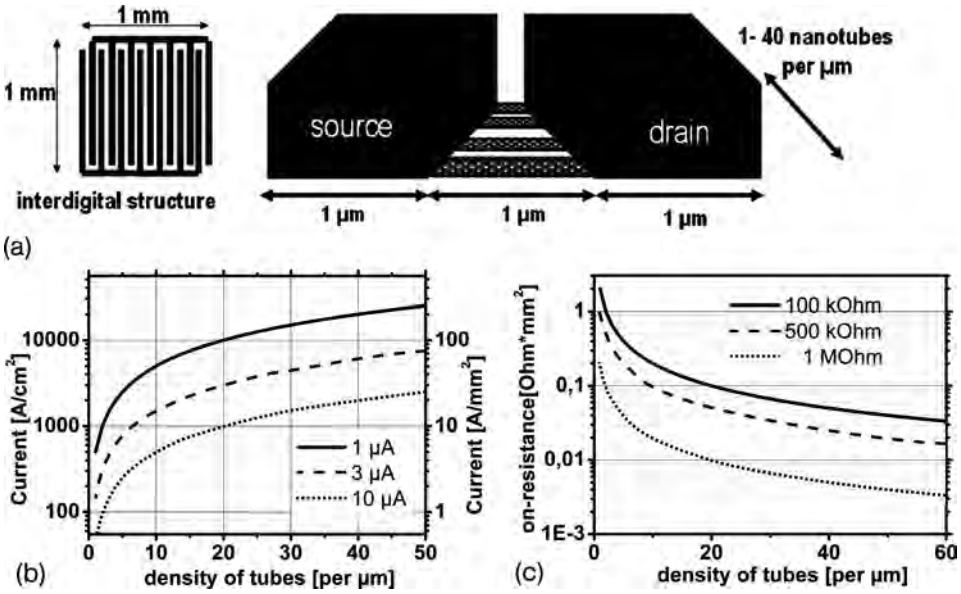


Figure 1.24 (a) Schematic of an interdigital source–drain structure for a high current switch. (b) Current density versus CNT density for the interdigital contacts at three different current levels. (c) On-resistance for varying CNT densities and three individual CNT resistances.

device can deliver 8 kA cm^{-2} at an on-resistance of only 3 mΩ mm^2. However, these optimistic values can only be obtained with challenging progress in the aligned fabrication of small-diameter semiconducting nanotubes.

1.5 Conclusions

The promising properties of carbon nanotubes have sparked a huge world-wide activity to investigate these objects in many technical areas – not only in microelectronic applications. Implementations, which rely on the statistical averaging of material properties, i.e. CNTs as additives in plastics, polymers and epoxies or as transparent conductive coatings, are closer to or already in the market. For microelectronic applications, the attractiveness has been already verified experimentally on the laboratory scale; however, a detailed strategy for large-scale integration of carbon nanotubes is still lacking. Integrated CNTs have to fulfill a whole range of requirements simultaneously – the most stringent demand being the precise placement of only one kind of CNT. The placement might be solved by localized growth of CNTs in vertical structures and the yield of semiconducting CNTs increased by special growth methods which favor the occurrence of only semiconducting CNTs. However, up to now, no-one has devised a CNT device which incorporates all needs for a scalable, reliable switch. Meanwhile, CNTs are

facing severe competition from nanowire technology [69], which benefits from clearly defined semiconducting properties of the nanowires and the lower processing temperature. However, the performance of nanotube-based devices still outperforms every other existing technology [69]. And if one looks back and recognizes the tremendous progress which has been achieved in nanotube technology during the past decade, one is certainly looking forward to what the future might bring.

1.6 Acknowledgments

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