

Contents

Preface XIII

List of Contributors XVII

I	Logic Devices and Concepts	1
1	Non-Conventional Complementary Metal-Oxide-Semiconductor (CMOS) Devices	3
	<i>Lothar Risch</i>	
1.1	Nano-Size CMOS and Challenges	3
1.2	Mobility Enhancement: SiGe, Strained Layers, Crystal Orientation	5
1.3	High- <i>k</i> Gate Dielectrics and Metal Gate	7
1.4	Ultra-Thin SOI	9
1.5	Multi-Gate Devices	12
1.5.1	Wafer-Bonded Planar Double Gate	13
1.5.2	Silicon-On-Nothing Gate All Around	14
1.5.3	FinFET	16
1.5.4	Limits of Multi-Gate MOSFETs	19
1.6	Multi-Gate Flash Cell	19
1.7	3d-DRAM Array Devices: RCAT, FinFET	22
1.8	Prospects	25
	References	26
2	Indium Arsenide (InAs) Nanowire Wrapped-Insulator-Gate Field-Effect Transistor	29
	<i>Lars-Erik Wernersson, Tomas Bryllert, Linus Fröberg, Erik Lind, Claes Thelander, and Lars Samuelson</i>	
2.1	Introduction	29
2.2	Nanowire Materials	30
2.3	Processing	30
2.4	Long-Channel Transistors	33

2.5	Short-Channel Transistors	35
2.6	Heterostructure WIGFETs	36
2.7	Benchmarking	39
2.8	Outlook	41
	References	42
3	Single-Electron Transistor and its Logic Application	45
	<i>Yukinori Ono, Hiroshi Inokawa, Yasuo Takahashi, Katsuhiko Nishiguchi, and Akira Fujiwara</i>	
3.1	Introduction	45
3.2	SET Operation Principle	46
3.3	SET Fabrication	49
3.4	Single-Electron Logic	54
3.4.1	Basic SET Logic	54
3.4.2	Multiple-Gate SET and Pass-Transistor Logic	56
3.4.3	Combined SET-MOSFET Configuration and Multiple-Valued Logic	59
3.4.4	Considerations on SET Logic	60
3.5	Conclusions	65
	References	65
4	Magnetic Domain Wall Logic	69
	<i>Dan A. Allwood and Russell P. Cowburn</i>	
4.1	Introduction	69
4.2	Experimental	72
4.3	Propagating Data	73
4.4	Data Processing	75
4.5	Data Writing and Erasing	84
4.6	Outlook and Conclusions	88
	References	90
5	Monolithic and Hybrid Spintronics	93
	<i>Supriyo Bandyopadhyay</i>	
5.1	Introduction	93
5.2	Hybrid Spintronics	94
5.2.1	The Spin Field Effect Transistor (SPINFET)	94
5.2.1.1	The Effect of Non-Idealities	97
5.2.1.2	The SPINFET Based on the Dresselhaus Spin–Orbit Interaction	100
5.2.2	Device Performance of SPINFETs	101
5.2.3	Other Types of SPINFET	102
5.2.3.1	The Non-Ballistic SPINFET	102
5.2.3.2	The Spin Relaxation Transistor	104
5.2.4	The Importance of the Spin Injection Efficiency	105
5.2.4.1	Spin Injection Efficiency	105
5.2.5	Spin Bipolar Junction Transistors (SBJTs)	106
5.2.6	The Switching Speed	107
5.3	Monolithic Spintronics: Single Spin Logic	107

5.3.1	Spin Polarization as a Bistable Entity	107
5.3.2	Stability of Spin Polarization	108
5.3.3	Reading and Writing Spin	108
5.3.3.1	Writing Spin	109
5.3.3.2	Reading Spin	109
5.3.4	The Universal Single Spin Logic Gate: The NAND Gate	109
5.3.5	Bit Error Probability	111
5.3.6	Related Charge-Based Paradigms	113
5.3.7	The Issue of Unidirectionality	114
5.3.8	Unidirectionality in Time: Clocking	115
5.3.9	Energy and Power Dissipation	116
5.3.10	Operating Temperature	117
5.3.11	Energy Dissipation Estimates	117
5.3.12	Other Issues	118
5.4	Spin-Based Quantum Computing: An Engineer's Perspective	118
5.4.1	Quantum Parallelism	120
5.4.2	Physical Realization of a Qubit: Spin of an Electron in a Quantum Dot	121
5.5	Conclusions	122
	References	122
6	Organic Transistors	125
	<i>Hagen Klauk</i>	
6.1	Introduction	125
6.2	Materials	128
6.3	Device Structures and Manufacturing	134
6.4	Electrical Characteristics	138
6.5	Applications	143
6.6	Outlook	148
	References	149
7	Carbon Nanotubes in Electronics	155
	<i>M. Meyyappan</i>	
7.1	Introduction	155
7.2	Structure and Properties	155
7.3	Growth	157
7.4	Nanoelectronics	160
7.4.1	Field Effect Transistors	161
7.4.2	Device Physics	166
7.4.3	Memory Devices	167
7.5	Carbon Nanotubes in Silicon CMOS Fabrication	167
7.5.1	Interconnects	167
7.5.2	Thermal Interface Material for Chip Cooling	169
7.5.3	CNT Probes in Metrology	170
7.6	Summary	172
	References	172

8	Concepts in Single-Molecule Electronics	175
	<i>Björn Lüssem and Thomas Bjørnholm</i>	
8.1	Introduction	175
8.2	The General Set-Up of a Molecular Device	176
8.2.1	The Strong Coupling Regime	177
8.2.2	The Weak Coupling Regime	178
8.3	Realizations of Molecular Devices	179
8.3.1	Molecular Contacts	179
8.3.2	Mechanically Controlled Break Junctions	180
8.3.3	Scanning Probe Set-Ups	181
8.3.4	Crossed Wire Set-Up	183
8.3.5	Nanogaps	183
8.3.6	Crossbar Structure	184
8.3.7	Three-Terminal Devices	185
8.3.8	Nanogaps Prepared by Chemical “Bottom-Up” Methods	187
8.3.9	Conclusion	187
8.4	Molecular Functions	189
8.4.1	Molecular Wires	190
8.4.2	Molecular Diodes	190
8.4.2.1	The Aviram–Ratner Concept	191
8.4.2.2	Rectification Due to Asymmetric Tunneling Barriers	192
8.4.2.3	Examples	193
8.4.2.4	Diode–Diode Logic	193
8.4.3	Negative Differential Resistance Diodes	194
8.4.3.1	Inverting Logic Using NDR Devices	195
8.4.4	Hysteretic switches	196
8.4.4.1	The Crossbar Latch: Signal Restoration and Inversion	197
8.4.5	Single-Molecule Single-Electron Transistors	199
8.4.6	Artifacts in Molecular Electronic Devices	201
8.4.6.1	Sources of Artifacts	201
8.4.7	Conclusions	203
8.5	Building Logical Circuits: Assembly of a Large Number of Molecular Devices	203
8.5.1	Programmable Logic Arrays Based on Crossbars	204
8.5.2	NanoCell	206
8.6	Challenges and Perspectives	207
	References	208
9	Intermolecular- and Intramolecular-Level Logic Devices	213
	<i>Françoise Remacle and Raphael D. Levine</i>	
9.1	Introduction and Background	213
9.1.1	Quantum Computing	213
9.1.2	Quasiclassical Computing	214
9.1.3	A Molecule as a Bistable Element	214
9.1.4	Chemical Logic Gates	215

9.1.5	Molecular Combinational Circuits	216
9.1.6	Concatenation, Fan-Out and Other Aspects of Integration	217
9.1.7	Finite-State Machines	217
9.1.8	Multi-Valued Logic	219
9.2	Combinational Circuits by Molecular Photophysics	219
9.2.1	Molecular Logic Implementations of a Half Adder by Photophysics	221
9.2.2	Two Manners of Optically Implementing a Full Adder	224
9.3	Finite-State Machines	228
9.3.1	Optically Addressed Finite-State Machines	229
9.3.2	Finite-State Machines by Electrical Addressing	236
9.4	Perspectives	242
	References	244
II	Architectures and Computational Concepts	249
10	A Survey of Bio-Inspired and Other Alternative Architectures	251
	<i>Dan Hammerstrom</i>	
10.1	Introduction	251
10.1.1	Basic Neuroscience	252
10.1.2	A Very Simple Neural Model: The Perceptron	253
10.1.3	A Slightly More Complex Neural Model: The Multiple Layer Perceptron	255
10.1.4	Auto-Association	256
10.1.5	The Development of Biologically Inspired Hardware	257
10.2	Early Studies in Biologically Inspired Hardware	258
10.2.1	Flexibility Trade-Offs and Amdhal's Law	260
10.2.2	Analog Very-Large-Scale Integration (VLSI)	263
10.2.3	Intel's Analog Neural Network Chip and Digital Neural Network Chip	265
10.2.4	Cellular Neural Networks	266
10.2.5	Other Analog/Mixed Signal Work	267
10.2.6	Digital SIMD Parallel Processing	268
10.2.7	Other Digital Architectures	272
10.2.8	General Vision	273
10.3	Current Directions in Neuro-Inspired Hardware	273
10.3.1	Moving to a More Sophisticated Neuro-Inspired Hardware	275
10.3.2	CMOL	278
10.3.3	An Example: CMOL Nano-Cortex	279
10.4	Summary and Conclusions	281
	References	282
11	Nanowire-Based Programmable Architectures	287
	<i>André DeHon</i>	
11.1	Introduction	287

11.2	Technology	289
11.2.1	Nanowires	289
11.2.2	Assembly	290
11.2.3	Crosspoints	290
11.2.4	Technology Roundup	291
11.3	Challenges	291
11.3.1	Regular Assembly	292
11.3.2	Nanowire Lengths	292
11.3.3	Defective Wires and Crosspoints	292
11.4	Building Blocks	293
11.4.1	Crosspoint Arrays	294
11.4.1.1	Memory Core	294
11.4.1.2	Programmable, Wired-OR Plane	294
11.4.1.3	Programmable Crossbar Interconnect Arrays	295
11.4.2	Decoders	296
11.4.2.1	NW Coding	296
11.4.2.2	Decoder Assembly	297
11.4.2.3	Decoder and Multiplexer Operation	297
11.4.3	Restoration and Inversion	298
11.4.3.1	NW Inverter and Buffer	299
11.4.3.2	Ideal Restoration Array	300
11.4.3.3	Restoration Array Construction	301
11.5	Memory Array	302
11.6	Logic Architecture	303
11.6.1	Logic	304
11.6.1.1	Construction	304
11.6.1.2	Logic Circuit	305
11.6.1.3	Programming	305
11.6.2	Registers and Sequential Logic	305
11.6.2.1	Basic Clocking	305
11.6.2.2	Precharge Evaluation	306
11.6.3	Interconnect	307
11.6.3.1	Basic Idea	307
11.6.3.2	NanoPLA Block	308
11.6.3.3	Interconnect	309
11.6.4	CMOS IO	311
11.6.5	Parameters	312
11.7	Defect Tolerance	313
11.7.1	NW Sparing	313
11.7.2	NW Defect Modeling	314
11.7.3	Net NW Yield Calculation	315
11.7.4	Tolerating Non-Programmable Crosspoints	315
11.8	Bootstrap Testing	317
11.8.1	Discovery	317
11.8.2	Programming	318

11.8.3	Scaling	319
11.9	Area, Delay, and Energy	319
11.9.1	Area	319
11.9.2	Delay	320
11.9.3	Energy and Power	320
11.10	Net Area Density	321
11.11	Alternate Approaches	322
11.12	Research Issues	324
11.13	Conclusions	324
	References	325
12	Quantum Cellular Automata	329
	<i>Massimo Macucci</i>	
12.1	Introduction	329
12.2	The Quantum Cellular Automaton Concept	330
12.2.1	A New Architectural Paradigm for Computation	330
12.2.2	From the Ground-State Approach to the Clocked QCA Architecture	336
12.2.3	Cell Polarization	338
12.3	Approaches to QCA Modeling	339
12.3.1	Hubbard-Like Hamiltonian	339
12.3.2	Configuration–Interaction	341
12.3.3	Semi-Classical Models	343
12.3.4	Simulated Annealing	346
12.3.5	Existing Simulators	347
12.4	Challenges and Characteristics of QCA Technology	348
12.4.1	Operating Temperature	348
12.4.2	Fabrication Tolerances	349
12.4.3	Limitations for the Operating Speed	350
12.4.4	Power Dissipation	353
12.5	Physical Implementations of the QCA Architecture	354
12.5.1	Implementation with Metallic Junctions	354
12.5.2	Semiconductor-Based Implementation	355
12.5.3	Molecular QCA	357
12.5.4	Nanomagnetic QCA	358
12.5.5	Split-Current QCA	359
12.6	Outlook	360
	References	361
13	Quantum Computation: Principles and Solid-State Concepts	363
	<i>Martin Weides and Edward Goldobin</i>	
13.1	Introduction to Quantum Computing	363
13.1.1	The Power of Quantum Computers	364
13.1.1.1	Sorting and Searching of Databases (Grover’s Algorithm)	365
13.1.1.2	Factorizing of Large Numbers (Shor’s Algorithm)	365
13.1.1.3	Cryptography and Quantum Communication	366

13.2	Types of Computation	366
13.2.1	Mathematical Definition of Information	366
13.2.2	Irreversible Computation	367
13.2.3	Reversible Computation	367
13.2.4	Information Carriers	368
13.3	Quantum Mechanics and Qubits	368
13.3.1	Bit versus Qubit	369
13.3.2	Qubit States	370
13.3.3	Entanglement	371
13.3.4	Physical State	371
13.3.4.1	Measurement	372
13.3.4.2	No-Cloning Theorem	372
13.4	Operation Scheme	372
13.4.1	Quantum Algorithms: Initialization, Execution and Termination	373
13.4.2	Quantum Gates	374
13.5	Quantum Decoherence and Error Correction	374
13.6	Qubit Requirements	375
13.7	Candidates for Qubits	375
13.7.1	Nuclear Magnetic Resonance (NMR)-Based Qubits	376
13.7.2	Advantages of Solid-State-Based Qubits	376
13.7.3	Kane Quantum Computer	377
13.7.4	Quantum Dot	378
13.7.5	Superconducting Qubits	378
13.7.5.1	Charge Qubits	379
13.7.5.2	Flux Qubits	379
13.7.5.3	Fractional Flux Qubits	380
13.8	Perspectives	382
	References	382
	Index	385