Contents

Preface *XV*
Obituary *XVII*
List of Contributors *XXI*
Introduction *XXV*

Part One Technologies *1*

A. Adhesive and Anodic Bonding *3*

1 Glass Frit Wafer Bonding *3*
Roy Knechtel
1.1 Principle of Glass Frit Bonding *3*
1.2 Glass Frit Materials *4*
1.3 Screen Printing: Process for Bringing Glass Frit Material onto Wafers *5*
1.4 Thermal Conditioning: Process for Transforming Printed Paste into Glass for Bonding *8*
1.5 Wafer Bond Process: Essential Wafer-to-Wafer Mounting by a Glass Frit Interlayer *11*
1.6 Characterization of Glass Frit Bonds *14*
1.7 Applications of Glass Frit Wafer Bonding *15*
1.8 Conclusions *16*
References *17*

2 Wafer Bonding Using Spin-On Glass as Bonding Material *19*
Viorel Dragoi
2.1 Spin-On Glass Materials *19*
2.2 Wafer Bonding with SOG Layers *21*
2.2.1 Experimental *21*
2.2.2 Wafer Bonding with Silicate SOG Layers *22*
2.2.3 Wafer Bonding with Planarization SOG *28*

2.2.4 Applications of Adhesive Wafer Bonding with SOG Layers *29*
2.2.5 Conclusion *30*
References *31*

3 Polymer Adhesive Wafer Bonding *33*
Frank Niklaus and Jian-Qiang Lu
3.1 Introduction *33*
3.2 Polymer Adhesives *34*
3.2.1 Polymer Adhesion Mechanisms *34*
3.2.2 Properties of Polymer Adhesives *36*
3.2.3 Polymer Adhesives for Wafer Bonding *38*
3.3 Polymer Adhesive Wafer Bonding Technology *42*
3.3.1 Polymer Adhesive Wafer Bonding Process *43*
3.3.2 Localized Polymer Adhesive Wafer Bonding *50*
3.4 Wafer-to-Wafer Alignment in Polymer Adhesive Wafer Bonding *52*
3.5 Examples for Polymer Adhesive Wafer Bonding Processes and Programs *54*
3.5.1 Bonding with Thermosetting Polymers for Permanent Wafer Bonds (BCB) or for Temporary Wafer Bonds (mr-I 9000) *54*
3.5.2 Bonding with Thermoplastic Polymer (HD-3007) for Temporary and Permanent Wafer Bonds *56*
3.6 Summary and Conclusions *57*
References *58*

4 Anodic Bonding *63*
Adriana Cozma Lapadatu and Kari Schjølberg-Henriksen
4.1 Introduction *63*
4.2 Mechanism of Anodic Bonding *64*
4.2.1 Glass Polarization *64*
4.2.2 Achieving Intimate Contact *65*
4.2.3 Interface Reactions *66*
4.3 Bonding Current *67*
4.4 Glasses for Anodic Bonding *68*
4.5 Characterization of Bond Quality *69*
4.6 Pressure Inside Vacuum-Sealed Cavities *70*
4.7 Effect of Anodic Bonding on Flexible Structures *71*
4.8 Electrical Degradation of Devices during Anodic Bonding *71*
4.8.1 Degradation by Sodium Contamination *72*
4.8.2 Degradation by High Electric Fields *73*
4.9 Bonding with Thin Films *75*
4.10 Conclusions *76*
References *77*

B. Direct Wafer Bonding *81*

5 **Direct Wafer Bonding** *81*
Manfred Reiche and Ulrich Gösele
5.1 Introduction *81*
5.2 Surface Chemistry and Physics *82*
5.3 Wafer Bonding Techniques *84*
5.3.1 Hydrophilic Wafer Bonding *84*
5.3.2 Hydrophobic Wafer Bonding *86*
5.3.3 Low-Temperature Wafer Bonding *88*
5.3.4 Wafer Bonding in Ultrahigh Vacuum *89*
5.4 Properties of Bonded Interfaces *90*
5.5 Applications of Wafer Bonding *93*
5.5.1 Advanced Substrates for Microelectronics *93*
5.5.2 MEMS and Nanoelectromechanical Systems *95*
5.6 Conclusions *95*
References *96*

6 **Plasma-Activated Bonding** *101*
Maik Wiemer, Dirk Wuensch, Joerg Braeuer, and Thomas Gessner
6.1 Introduction *101*
6.2 Theory *102*
6.2.1 (Silicon) Direct Bonding *102*
6.2.2 Mechanisms of Plasma on Silicon Surfaces *103*
6.2.3 Physical Definition of a Plasma *104*
6.3 Classification of PAB *104*
6.3.1 Low-Pressure PAB *105*
6.3.2 Atmospheric-Pressure PAB *106*
6.4 Procedure of PAB *107*
6.4.1 Process Flow *107*
6.4.2 Characterization Techniques *108*
6.4.3 Experiments and Results *110*
6.5 Applications for PAB *111*
6.5.1 Pressure Sensor *112*
6.5.2 Optical Microsystem *112*
6.5.3 Microfluidics Packaging *113*
6.5.4 Backside-Illuminated CMOS Image Sensor *113*
6.5.5 CMOS Compatibility of Low-Pressure PAB *114*
6.6 Conclusion *115*
References *115*

C. Metal Bonding *119*

7 **Au/Sn Solder** *119*
Hermann Oppermann and Matthias Hutter
7.1 Introduction *119*

7.2 Au/Sn Solder Alloy *120*
7.3 Reflow Soldering *127*
7.4 Thermode Soldering *130*
7.5 Aspects of Three-Dimensional Integration and Wafer-Level Assembly *132*
7.6 Summary and Conclusions *135*
References *136*

8 Eutectic Au–In Bonding *139*
Mitsumasa Koyanagi and Makoto Motoyoshi
8.1 Introduction *139*
8.2 Organic/Metal Hybrid Bonding *140*
8.3 Organic/In–Au Hybrid Bonding *142*
8.3.1 In–Au Phase Diagram and Bonding Principle *142*
8.3.2 Formation of In–Au Microbumps by a Planarized Liftoff Method *144*
8.3.3 Eutectic In–Au Bonding and Epoxy Adhesive Injection *146*
8.3.4 Electrical Characteristics of In–Au Microbumps *148*
8.4 Three-Dimensional LSI Test Chips Fabricated by Eutectic In–Au Bonding *149*
8.5 High-Density and Narrow-Pitch Mircobump Technology *152*
8.6 Conclusion *157*
Acknowledgment *157*
References *157*

9 Thermocompression Cu–Cu Bonding of Blanket and Patterned Wafers *161*
Kuan-Neng Chen and Chuan Seng Tan
9.1 Introduction *161*
9.2 Classification of the Cu Bonding Technique *162*
9.2.1 Thermocompression Cu Bonding *162*
9.2.2 Surface-Activated Cu Bonding *162*
9.3 Fundamental Properties of Cu Bonding *163*
9.3.1 Morphology and Oxide Examination of Cu Bonded Layer *163*
9.3.2 Microstructure Evolution during Cu Bonding *164*
9.3.3 Orientation Evolution during Cu Bonding *165*
9.4 Development of Cu Bonding *166*
9.4.1 Fabrication and Surface Preparation of Cu Bond Pads *166*
9.4.2 Parameters of Cu Bonding *167*
9.4.3 Structural Design *168*
9.5 Characterization of Cu Bonding Quality *169*
9.5.1 Mechanical Tests *169*
9.5.2 Image Analysis *170*
9.5.3 Electrical Characterization *171*
9.5.4 Thermal Reliability *171*

9.6 Alignment Accuracy of Cu–Cu Bonding *171*
9.7 Reliable Cu Bonding and Multilayer Stacking *172*
9.8 Nonblanket Cu–Cu Bonding *174*
9.9 Low-Temperature (<300 °C) Cu–Cu Bonding *176*
9.10 Applications of Cu Wafer Bonding *178*
9.11 Summary *178*
References *179*

10 Wafer-Level Solid–Liquid Interdiffusion Bonding *181*
Nils Hoivik and Knut Aasmundtveit
10.1 Background *181*
10.1.1 Solid–Liquid Interdiffusion Bonding Process *181*
10.1.2 SLID Bonding Compared with Soldering *182*
10.1.3 Material Systems for SLID Bonding *183*
10.2 Cu–Sn SLID Bonding *189*
10.2.1 Cu–Sn Material Properties and Required Metal Thicknesses *190*
10.2.2 Bonding Processes *191*
10.2.3 Pretreatment Requirements for SLID Bonding *195*
10.2.4 Fluxless Bonding *196*
10.3 Au–Sn SLID Bonding *199*
10.3.1 Au–Sn Material Properties and Required Metal Thicknesses *199*
10.3.2 Bonding Processes *199*
10.4 Application of SLID Bonding *201*
10.4.1 Cu–Sn Bonding *201*
10.4.2 Au–Sn Bonding *204*
10.5 Integrity of SLID Bonding *207*
10.5.1 Electrical Reliability and Electromigration Testing *207*
10.5.2 Mechanical Strength of SLID Bonds *207*
10.6 Summary *210*
References *212*

D. Hybrid Metal/Dielectric Bonding *215*

11 Hybrid Metal/Polymer Wafer Bonding Platform *215*
Jian-Qiang Lu, J. Jay McMahon, and Ronald J. Gutmann
11.1 Introduction *215*
11.2 Three-Dimensional Platform Using Hybrid Cu/BCB Bonding *217*
11.3 Baseline Bonding Process for Hybrid Cu/BCB Bonding Platform *220*
11.4 Evaluation of Cu/BCB Hybrid Bonding Processing Issues *222*
11.4.1 CMP and Bonding of Partially Cured BCB *222*
11.4.2 Cu/BCB CMP Surface Profile *223*

11.4.3 Hybrid Cu/BCB Bonding Interfaces *224*
11.4.4 Topography Accommodation Capability of Partially Cured BCB *227*
11.4.5 Electrical Characterization of Hybrid Cu/BCB Bonding *231*
11.5 Summary and Conclusions *232*
Acknowledgments *233*
References *233*

12 Cu/SiO_2 Hybrid Bonding *237*
Léa Di Cioccio
12.1 Introduction *237*
12.2 Blanket Cu/SiO_2 Direct Bonding Principle *239*
12.2.1 Chemical Mechanical Polishing Parameters *239*
12.2.2 Bonding Quality and Alignment *243*
12.3 Blanket Copper Direct Bonding Principle *245*
12.4 Electrical Characterization *251*
12.5 Die-to-Wafer Bonding *255*
12.5.1 Daisy Chain Structures *256*
12.6 Conclusion *257*
Acknowledgment *257*
References *258*

13 Metal/Silicon Oxide Hybrid Bonding *261*
Paul Enquist
13.1 Introduction *261*
13.2 Metal/Non-adhesive Hybrid Bonding–Metal DBI® *261*
13.3 Metal/Silicon Oxide DBI® *262*
13.3.1 Metal/Silicon Oxide DBI® Surface Fabrication *263*
13.3.2 Metal/Silicon Oxide DBI® Surface Patterning *264*
13.3.3 Metal/Silicon Oxide DBI® Surface Topography *264*
13.3.4 Metal/Silicon Oxide DBI® Surface Roughness *264*
13.3.5 Metal/Silicon Oxide DBI® Surface Activation and Termination *265*
13.3.6 Metal/Silicon Oxide DBI® Alignment and Hybrid Surface Contact *265*
13.3.7 Metal Parameters Relevant to DBI® Surface Fabrication and Electrical Interconnection *268*
13.3.8 DBI® Metal/Silicon Oxide State of the Art *270*
13.4 Metal/Silicon Nitride DBI® *271*
13.5 Metal/Silicon Oxide DBI® Hybrid Bonding Applications *273*
13.5.1 Pixelated 3D ICs *273*
13.5.2 Three-Dimensional Heterogeneous Integration *275*
13.5.3 CMOS (Ultra) Low-k 3D Integration *276*
13.6 Summary *276*
References *277*

Part Two Applications *279*

14 Microelectromechanical Systems *281*
Maaike M.V. Taklo
14.1 Introduction *281*
14.2 Wafer Bonding for Encapsulation of MEMS *282*
14.2.1 Protection during Wafer Dicing *282*
14.2.2 Routing of Electrical Signal Lines *282*
14.3 Wafer Bonding to Build Advanced MEMS Structures *284*
14.3.1 Stacking of Several Wafers *284*
14.3.2 Post-processing of Bonded Wafers *285*
14.4 Examples of MEMS and Their Requirements for the Bonding Process *286*
14.5 Integration of Some Common Wafer Bonding Processes *287*
14.5.1 Fusion Bonding of Patterned Wafers *287*
14.5.2 Anodic Bonding of Patterned Wafers *290*
14.5.3 Eutectic Bonding of Patterned Wafers: AuSn *293*
14.6 Summary *297*
References *297*

15 Three-Dimensional Integration *301*
Philip Garrou, James Jian-Qiang Lu, and Peter Ramm
15.1 Definitions *301*
15.2 Application of Wafer Bonding for 3D Integration Technology *303*
15.3 Motivations for Moving to 3D Integration *305*
15.4 Applications of 3D Integration Technology *307*
15.4.1 Three-Dimensional Applications by Evolution Not Revolution *307*
15.4.2 Microbump Bonding/No TSV *308*
15.4.3 TSV Formation/No Stacking *310*
15.4.4 Memory *312*
15.4.5 Memory on Logic *321*
15.4.6 Repartitioning Logic *322*
15.4.7 Foundry and OSAT Activity *323*
15.4.8 Other 3D Applications *323*
15.5 Conclusions *325*
References *325*

16 Temporary Bonding for Enabling Three-Dimensional Integration and Packaging *329*
Rama Puligadda
16.1 Introduction *329*
16.2 Temporary Bonding Technology Options *330*
16.2.1 Key Requirements *331*
16.2.2 Foremost Temporary Wafer Bonding Technologies *332*

16.3 Boundary Conditions for Successful Processing *337*
16.3.1 Uniform and Void-Free Bonding *337*
16.3.2 Protection of Wafer Edges during Thinning and Subsequent Processing *337*
16.4 Three-Dimensional Integration Processes Demonstrated with Thermomechanical Debonding Approach *338*
16.4.1 Via-Last Process on CMOS Image Sensor Device Wafers *338*
16.4.2 Via-Last Process with Aspect Ratio of 2 : 1 *341*
16.4.3 Via-Last Process with 50 μm Depth Using High-Temperature TEOS Process *341*
16.4.4 Die-to-Wafer Stacking Using Interconnect Via Solid–Liquid Interdiffusion Process *342*
16.5 Concluding Remarks *343*
Acknowledgments *344*
References *344*

17 Temporary Adhesive Bonding with Reconfiguration of Known Good Dies for Three-Dimensional Integrated Systems *347*
Armin Klumpp and Peter Ramm
17.1 Die Assembly with SLID Bonding *347*
17.2 Reconfiguration *348*
17.3 Wafer-to-Wafer Assembly by SLID Bonding *349*
17.4 Reconfiguration with Ultrathin Chips *351*
17.5 Conclusion *352*
Acknowledgments *353*
References *354*

18 Thin Wafer Support System for above 250 °C Processing and Cold De-bonding *355*
Werner Pamler and Franz Richter
18.1 Introduction *355*
18.2 Process Flow *356*
18.2.1 Release Layer Processing *357*
18.2.2 Carrier Wafer Processing *357*
18.2.3 Bonding Process *357*
18.2.4 Thinning *359*
18.2.5 De-bonding Process *360*
18.2.6 Equipment *361*
18.3 Properties *361*
18.3.1 Device Wafer Thickness *361*
18.3.2 Thickness Uniformity *361*
18.3.3 Stability *362*
18.4 Applications *362*
18.4.1 Bonding of Bumped Wafers *363*

18.4.2 Packaging of Ultrathin Dies 363
18.4.3 TSV Processing 364
18.4.4 Re-using the Carrier 364
18.5 Conclusions 364
Acknowledgments 365
References 365

19 Temporary Bonding: Electrostatic 367
Christof Landesberger, Armin Klumpp, and Karlheinz Bock
19.1 Basic Principles: Electrostatic Forces between Parallel Plates 367
19.1.1 Electric Fields and Electrostatic Forces in a Plate Capacitor 368
19.1.2 Electrostatic Attraction in a Bipolar Configuration 369
19.1.3 Johnsen–Rahbek Effect 370
19.2 Technological Concept for Manufacture of Mobile Electrostatic Carriers 371
19.2.1 Selection of Substrate Material 371
19.2.2 Selection of Thin-Film Dielectric Layers 372
19.2.3 Electrode Patterns: Materials and Geometry 374
19.2.4 Examples of Mobile Electrostatic Carriers 375
19.3 Characterization of Electrostatic Carriers 376
19.3.1 Electrical and Thermal Properties, Leakage Currents 376
19.3.2 Possible Influence of Electrostatic Fields on CMOS Devices 378
19.4 Electrostatic Carriers for Processing of Thin and Flexible Substrates 379
19.4.1 Handling and Transfer of Thin Semiconductor Wafers 379
19.4.2 Wafer Thinning and Backside Metallization 380
19.4.3 Electrostatic Carriers in Plasma Processing 380
19.4.4 Electrostatic Carriers Enable Bumping of Thin Wafers 380
19.4.5 Electrostatic Carriers in Wet-Chemical Environments 381
19.4.6 Electrostatic Handling of Single Dies 381
19.4.7 Processing of Foils and Insulating Substrates 381
19.5 Summary and Outlook 382
References 383

Index 385