

Contents

Volume 1

Preface *XVII*

List of Contributors *XIX*

1	Introduction to 3D Integration	1
	<i>Philip Garrou</i>	
1.1	Introduction	1
1.2	Historical Evolution of Stacked Wafer Concepts	3
1.3	3D Packaging vs 3D Integration	4
1.4	Non-TSV 3D Stacking Technologies	6
1.4.1	Irvine Sensors	6
1.4.2	UTCS (Ultrathin Chip Stacking) IMEC, CNRS, U. Barcelona	6
1.4.3	Fujitsu	7
1.4.4	Fraunhofer/IZM	9
1.4.5	3D Plus/Leti	10
1.4.6	Toshiba System Block Module	11
	References	11
2	Drivers for 3D Integration	13
	<i>Philip Garrou, Susan Vitkavage, and Sitaram Arkalgud</i>	
2.1	Introduction	13
2.2	Electrical Performance	13
2.2.1	Signal Seed	14
2.2.2	Memory Latency	17
2.3	Power Consumption and Noise	19
2.3.1	Noise	19
2.4	Form Factor	19
2.4.1	Non-Volatile Memory Technology: Flash	20

2.4.2	Volatile Memory Technology: SRAM and DRAM	21
2.4.3	CMOS Image Sensors	21
2.5	Lower Cost	22
2.6	Application Based Drivers	22
2.6.1	Microprocessors	22
2.6.2	Memory	22
2.6.3	Sensors	23
2.6.4	Fields Programmable Gate Arrays (FPGAs)	23
	References	23

3 Overview of 3D Integration Process Technology 25

Philip Garrou and Christopher Bower

3.1	3D Integration Terminology	25
3.1.1	Through Silicon Vias (TSVs)	25
3.1.2	Wafer Thinning	27
3.1.3	Aligned Wafer/IC Bonding	28
3.2	Processing Sequences	28
3.3	Technologies for 3D Integration	34
3.3.1	TSV Formation	34
3.3.2	Temporary Bonding to Carrier Wafer	38
3.3.3	Thinning	39
3.3.4	Alignment/Bonding	40
	References	43

I Through Silicon Via Fabrication 45

4 Deep Reactive Ion Etching of Through Silicon Vias 47

Fred Roozeboom, Michiel A. Blauw, Yann Lamy, Eric van Grunsven, Wouter Dekkers, Jan F. Verhoeven, Eric(F.) van den Heuvel, Emile van der Drift, Erwin (W.M.M.) Kessels, and Richard (M.C.M.) van de Sanden

4.1	Introduction	47
4.1.1	Deep Reactive Ion Etching as Breakthrough Enabling Through-Wafer Interconnects	47
4.1.2	State of the Art and Basic Principles in DRIE	48
4.1.3	Bosch Process	49
4.1.4	Alternatives for Via Hole Creation	50
4.2	DRIE Equipment and Characterization	54
4.2.1	High-Density Plasma Reactors	54
4.2.2	Plasma Chemistry	59
4.2.3	Plasma Diagnostics and Surface Analysis	60
4.3	DRIE Processing	62
4.3.1	Mask Issues	62
4.3.2	High Aspect Ratio Features	66
4.3.3	Sidewall Passivation, Depassivation and Profile Control	71

4.4	Practical Solutions in Via Etching	78
4.4.1	Undercut and Scallop Reduction	79
4.4.2	Sidewall Roughness Minimization	79
4.4.3	Loading Effects	80
4.4.4	Notching at Dielectric Interfaces	83
4.4.5	Inspection of Via Structures	83
4.4.6	<i>In Situ</i> Trench Depth Measurement	85
4.5	Concluding Remarks	86
	Appendix A: Glossary of Abbreviations	87
	Appendix B: Examples of DRIE Recipes	88
	References	89
5	Laser Ablation	93
	<i>Wei-Chung Lo and S.M. Chang</i>	
5.1	Introduction	93
5.2	Laser Technology for 3D Packaging	94
5.2.1	Advantages	94
5.2.2	Disadvantages	94
5.3	For Si Substrate	94
5.3.1	Difficulties	94
5.3.2	Results	95
5.4	Results for 3D Chip Stacking	100
5.5	Reliabilities	103
5.6	The Future	104
	References	105
6	SiO₂	107
	<i>Robert Wieland</i>	
6.1	Introduction	107
6.2	Dielectric CVD	107
6.2.1	Sub-Atmospheric CVD	109
6.2.2	Process Sequence of O ₃ -Activated SACVD Deposition	111
6.2.3	Conformal SACVD O ₃ TEOS Films for 3D Integration	111
6.3	Dielectric Film Properties	115
6.4	3D-Specifics Regarding SiO ₂ Dielectrics	116
6.4.1	Wafer Pre-Processing	116
6.4.2	Backside Processing Requirements on SiO ₂ Film Conformality in TSVs	117
6.4.3	SiO ₂ Film Deposition on Thinned Silicon Substrates	118
6.5	Concluding Remarks	119
	References	119
7	Insulation – Organic Dielectrics	121
	<i>Philip Garrou and Christopher Bower</i>	
7.1	Parylene	121

7.1.1	Parylene in TSVs	122
7.1.2	Limiting Aspects of Parylene	125
7.2	Plasma-Polymerized BCB	125
7.3	Spray-Coated Organic Insulators	126
7.4	Laser-Drilled Organics	128
7.5	Concluding Remarks	130
	References	130
8	Copper Plating	133
	<i>Tom Ritzdorf, Rozalia Beica, and Charles Sharbono</i>	
8.1	Introduction	133
8.2	Copper Plating Equipment	134
8.3	Copper Plating Processes	135
8.3.1	Copper Lining	138
8.3.2	Copper Full Fill With and Without Stud Formation	139
8.4	Factors Affecting Copper Plating	141
8.4.1	Via Profile and Smoothness	141
8.4.2	Insulator/Barrier/Seed Layer Coverage	142
8.4.3	Feature Wetting	143
8.5	Plating Chemistries	144
8.5.1	Acid Copper Sulfate Chemistry	144
8.5.2	Methane Sulfonic Acid Chemistry	145
8.5.3	Cyanide Chemistry	145
8.5.4	Other Copper Plating Chemistries	145
8.6	Plating Process Requirements	146
8.6.1	Suggested Mechanisms for Superconformal Deposition	146
8.6.2	Effect of Waveform and Current Density on Fill Performance	149
8.6.3	Effect of Deposition Waveform on Fill Performance	150
8.6.4	Impact of Feature Dimension on Fill Time	151
8.6.5	Impact of Feature Dimension on Overburden	152
8.6.6	Bath Analysis and Maintenance	153
8.7	Summary	153
	References	154
9	Metallization by Chemical Vapor Deposition of W and Cu	157
	<i>Armin Klumpp, Robert Wieland, Ramona Ecke, and Stefan E. Schulz</i>	
9.1	Introduction	157
9.2	Commercial Precursors	158
9.2.1	TiN Precursors	159
9.2.2	Copper Precursors	159
9.2.3	Tungsten Precursor	160
9.3	Deposition Process Flow	161
9.3.1	Barrier Deposition	162
9.3.2	Adhesion Layer	163

9.3.3	Copper Deposition	165
9.3.4	Tungsten CVD Application to TSV Fill	168
9.4	Complete TSV Metallization Including Filling and Etchback/CMP	169
9.4.1	W-CVD Metallization	169
9.4.2	Cu CVD Metallization	171
9.5	Conclusions	172
	References	173

II Wafer Thinning and Bonding Technology 175

10	Fabrication, Processing and Singulation of Thin Wafers	177
	<i>Werner Kröniger</i>	
10.1	Applications for Thin Silicon Dies	177
10.2	Principal Facts: Thinning and Wafer Bow	177
10.2.1	Where Does this Phenomenon Come From?	178
10.3	Grinding and Thinning	179
10.3.1	Grinding Parameters	180
10.3.2	Vice Versa Influences of Parameters	181
10.4	Stability and Flexibility	183
10.4.1	Measuring Breaking-Strength and Flexibility	184
10.4.2	Statistics and Evaluation	185
10.5	Chip Thickness, Theoretical Model, Macroscopic Features	186
10.5.1	Chip Thickness	186
10.5.2	Theoretical Model	187
10.5.3	Macroscopic Features: Chip Strength, Flexibility, Roughness and Hardness	188
10.5.4	From Blank to Processed Chips: Changes?	191
10.6	Stabilizing the Thin Wafer: Tapes and Carrier Systems	192
10.6.1	Special Tapes for Handling Wafers and Dies	193
10.6.2	Carrier Systems	193
10.7	Separating the Chips: Dicing Influencing the Stability	195
10.7.1	Classical Mechanical Dicing	195
10.7.2	Laser Dicing	199
10.7.3	Comparing Methods of Separation	201
10.8	Conclusions	206
10.9	Summary	206
	References	207
11	Overview of Bonding Technologies for 3D Integration	209
	<i>Jean-Pierre Joly</i>	
11.1	Introduction	209
11.2	Direct Bonding	210
11.2.1	Direct Bonding Principles	210

11.2.2	Surface Direct SiO/SiO Bonding	211
11.2.3	Metal Surface Activated Bonding	215
11.3	Adhesive and Solder Bonding	216
11.3.1	Polymer Bonding	217
11.3.2	Metal Soldering or Eutectic Bonding	218
11.4	Comparison of the Different Bonding Technologies	219
	References	221

12 **Chip-to-Wafer and Wafer-to-Wafer Integration Schemes** 223

Thorsten Matthias, Stefan Pargfrieder, Markus Wimplinger, and Paul Lindner

12.1	Decision Criteria for 3D Integration	223
12.1.1	Different Wafer Sizes	223
12.1.2	Different Fabs	224
12.1.3	Different Base Substrates	224
12.1.4	Different Chip Size	224
12.1.5	Number of Stacked Layers	224
12.1.6	Modular Design	225
12.1.7	Yield Issue	225
12.1.8	Throughput	226
12.1.9	Alignment	226
12.1.10	Cost	226
12.2	Enabling Technologies	227
12.2.1	Aligned Wafer Bonding	227
12.2.2	Bonding Methods	233
12.2.3	Temporary Bonding/Debonding	240
12.2.4	Chip to Wafer Bonding	242
12.3	Integration Schemes for 3D Interconnect	244
12.3.1	Face-to-Face Chip Stacking	244
12.3.2	Face-to-Back Chip Stacking	245
12.4	Conclusion	248
	References	248

13 **Polymer Adhesive Bonding Technology** 249

James Jian-Qiang Lu, Tim S. Cale, and Ronald J. Gutmann

13.1	Polymer Adhesive Bonding Principle	249
13.2	Polymer Adhesive Bonding Requirements and Materials	250
13.3	Wafer Bonding Technology Using Polymer Adhesives	252
13.4	Bonding Characterizations	253
13.4.1	Optical Inspection Using Glass Wafer	255
13.4.2	Bonding Strength Characterization Using Four-Point Bending	255
13.4.3	Adhesive Wafer Bonding Integrity	257
13.5	Conclusions	258
	References	258

14	Bonding with Intermetallic Compounds	261
	<i>Armin Klumpp</i>	
14.1	Introduction	261
14.2	Technological Concepts	261
14.2.1	Basic Material Selection	262
14.2.2	Principal Processing Scheme	263
14.2.3	Limiting Conditions for Applications	265
14.3	Conclusion	269
	References	269
	Volume 2	
III	Integration Processes	271
15	Commercial Activity	273
	<i>Philip Garrou</i>	
15.1	Introduction	273
15.2	Chip-on-Chip Activity	273
15.3	Imaging Chips with TSV	275
15.4	Memory	276
15.5	Microprocessors & Misc. Applications	283
16	Wafer-Level 3D System Integration	289
	<i>Peter Ramm, M. Jürgen Wolf, and Bernhard Wunderle</i>	
16.1	Introduction	289
16.2	Wafer-Level 3D System Integration Technologies	291
16.3	Reliability Issues	308
16.4	Conclusions	314
17	Interconnect Process at the University of Arkansas	319
	<i>Susan Burkett and Leonard Schaper</i>	
17.1	Introduction	319
17.2	TSV Process Flow	321
17.3	Chip Assembly	330
17.4	System Integration	333
17.5	Summary	334
	References	334
18	Vertical Interconnection by ASET	339
	<i>Kenji Takahashi and Kazumasa Tanida</i>	
18.1	Introduction	339
18.2	Fabrication Process Overview	341
18.3	Via Filling by Cu Electrodeposition	341

18.4	Handling of Thin Wafer	345
18.5	3D Chip Stacking	348
18.6	Thermal Performance of Chip Stack Module	363
18.7	Electric Performance of Vertical Interconnection	367
18.8	Practical Application of Through-vias	370
18.9	Conclusion	371
19	3D Integration at CEA-LETI	375
	<i>Barbara Charlet, Lèa Di Cioccio, Patrick Leduc, and David Henry</i>	
19.1	Introduction	375
19.2	Circuit Transfer for Efficient Stacking in 3D Integration	375
19.3	Non-Destructive Characterization of Stacked Layers	376
19.4	Example of 3D Integration Application Developments	380
19.5	Summary	390
20	Lincoln Laboratory's 3D Circuit Integration Technology	393
	<i>James Burns, Brian Aull, Robert Berger, Nisha Checka, Chang-Lee Chen, Chenson Chen, Pascale Gouker, Craig Keast, Jeffrey Knecht, Antonio Soares, Vyshnavi Suntharalingam, Brian Tyrrell, Keith Warner, Bruce Wheeler, Peter Wyatt, and Donna Yost</i>	
20.1	Introduction	393
20.2	Lincoln Laboratory's Wafer-Scale 3D Circuit Integration Technology	394
20.3	Transferred FDSOI Transistor and Device Properties	402
20.4	3D Circuit and Device Results	406
20.5	Summary	409
21	3D Integration Technologies at IMEC	413
	<i>Eric Beyne</i>	
21.1	Introduction	413
21.2	Key Requirements for 3D-Interconnect Technologies	415
21.3	3D Technologies at IMEC	418
22	Fabrication Using Copper Thermo-Compression Bonding at MIT	431
	<i>Chuan Seng Tan, Andy Fan, and Rafael Reif</i>	
22.1	Introduction	431
22.2	Copper Thermo-Compression Bonding	431
22.3	Process Flow	434
22.4	Discussion	442
22.5	Summary	445
23	Rensselaer 3D Integration Processes	447
	<i>James Jian-Qiang Lu, Tim S. Cale, and Ronald J. Gutmann</i>	
23.1	Introduction	447

- 23.2 Via-Last 3D Platform Using Adhesive Wafer Bonding and Cu Damascene Inter-Wafer Interconnect 447
- 23.3 Via-Last 3D Platform Feasibility Demonstration: Via-Chain Structure with Key Unit Processes of Alignment, Bonding, Thinning and Inter-wafer Interconnection 449
- 23.4 Via-First 3D Platform with Wafer-Bonding of Damascene-Patterned Metal/Adhesive Redistribution Layers 451
- 23.5 Via-First 3D Platform Feasibility Demonstration: Via-Chain Structure with Cu/BCB Redistribution Layers 453
- 23.6 Unit Process Advancements 454
- 23.7 Carbon Nanotube (CNT) Interconnect 458
- 23.8 Summary 460

- 24 3D Integration at Tezzaron Semiconductor Corporation 463**
Robert Patti
- 24.1 Introduction 463
- 24.2 Copper Bonding 463
- 24.3 Yield Issues 464
- 24.4 Interconnect Density 465
- 24.5 Process Requirements for 3D DRAM 466
- 24.6 FaStack Process Overview 467
- 24.7 Bonding Before Thinning 467
- 24.8 Tezzaron's TSVs 467
- 24.9 Stacking Process Flow Details (with SuperContacts) 472
- 24.10 Stacking Process Flow with SuperVias 473
- 24.11 Additional Stacking Process Issues 474
- 24.12 Working 3D Devices 481
- 24.13 Qualification Results 481
- 24.14 FaStack Summary 485
- 24.15 Abbreviations and Definitions 486

- 25 3D Integration at Ziptronix, Inc. 487**
Paul Enquist
- 25.1 Introduction 487
- 25.2 Direct Bonding 489
- 25.3 Direct Bond Interconnect 497
- 25.4 Process Cost and Supply Chain Considerations 501

- 26 3D Integration ZyCube 505**
Makoto Motoyoshi
- 26.1 Introduction 505
- 26.2 Current 3D-LSI—New CSP Device for Sensors 505
- 26.3 Future 3D-LSI Technology 512

IV	Design, Performance, and Thermal Management	517
27	Design for 3D Integration at North Carolina State University	519
	<i>Paul D. Franzon</i>	
27.1	Why 3D?	519
27.2	Interconnect-Driven Case Studies	521
27.3	Computer-Aided Design	525
27.4	Discussion	526
28	Modeling Approaches and Design Methods for 3D System Design	529
	<i>Peter Schneider and Günter Elst</i>	
28.1	Introduction	529
28.2	Modeling and Simulation	530
28.3	Design Methods for 3D Integration	565
28.4	Conclusions	571
29	Multiproject Circuit Design and Layout in Lincoln Laboratory's 3D Technology	575
	<i>James Burns, Robert Berger, Nisha Checka, Craig Keast, Brian Tyrrell, and Bruce Wheeler</i>	
29.1	Introduction	575
29.2	3D Design and Layout Practice	575
29.3	Design and Submission Procedures	578
30	Computer-Aided Design for 3D Circuits at the University of Minnesota	583
	<i>Sachin S. Sapatnekar</i>	
30.1	Introduction	583
30.2	Thermal Analysis of 3D Designs	584
30.3	Thermally-Driven Placement and Routing of 3D Designs	586
30.4	Power Grid Design in 3D	594
30.5	Conclusion	596
31	Electrical Performance of 3D Circuits	599
	<i>Arne Heitmann and Ulrich Ramacher</i>	
31.1	Introduction	599
31.2	3D Chip Stack Technology	607
31.3	Electrical Performance of 3D Contacts	613
31.4	Summary and Conclusion	618
32	Testing of 3D Circuits	623
	<i>T.M. Mak</i>	
32.1	Introduction	623
32.2	Yield and 3D Integration	624

32.3	Known Good Die (KGD)	627
32.4	Wafer Stacking Versus Die Stacking	629
32.5	Defect Tolerant and Fault Tolerant 3D Stacks	632
33	Thermal Management of Vertically Integrated Packages	635
	<i>Thomas Brunschwiler and Bruno Michel</i>	
33.1	Introduction	635
33.2	Fundamentals of Heat Transfer	637
33.3	Thermal-Packaging Modeling	639
33.4	Metrology in Thermal Packaging	640
33.5	Thermal Packaging Components	641
33.6	Heat Removal in Vertically-Integrated Packages	644
V	Applications	651
34	3D and Microprocessors	653
	<i>Pat Morrow and Sriram Muthukumar</i>	
34.1	Introduction	653
34.2	Design of 3D Microprocessor Systems	654
34.3	Fabrication of 3D Microprocessor Systems	661
34.4	Conclusions	670
35	3D Memories	675
	<i>Mark Tuttle</i>	
35.1	Introduction	675
35.2	Applications	675
35.3	Redistribution Layer	679
35.4	Through Wafer Interconnect	681
35.5	Stacking	684
35.6	Additional Issues	686
35.7	Future of 3D Memories	688
36	3D Read-Out Integrated Circuits for Advanced Sensor Arrays	689
	<i>Christopher Bower</i>	
36.1	Introduction	689
36.2	Current Activity in 3D ROICs	690
36.3	Conclusions	700
37	Power Devices	703
	<i>Marc de Samber, Eric van Grunsven, and David Heyes</i>	
37.1	Introduction	703
37.2	Wafer Level Packaging for Discrete Semiconductor Devices	704
37.3	Packaging for PowerMOSFET Devices	704
37.4	Chip Size Packaging of Vertical MOSFETs	707

37.5 Metal TWI Process for Vertical MOSFETs 711
37.6 Further Evaluation of the TWI MOSFET CSPs 718
37.7 Outlook 720

38 Wireless Sensor Systems – The e-CUBES Project 723

Adrian M. Ionescu, Eric Beyne, Thierry Hilt, Thomas Herndl, Pierre Nicole, Mihai Sanduleanu, Anton Sauer, Herbert Shea, Maaïke Taklo, Co Van Veen, Josef Weber, Werner Weber, Jürgen M. Wolf, and Peter Ramm

38.1 Introduction 723
38.2 e-CUBES Concept 725
38.3 Enabling 3D Integration Technologies 727
38.4 e-CUBES GHz Radios 731
38.5 e-CUBES Applications and Roadmap 735
38.6 Conclusion 745

Conclusions 747

Phil Garrou, Christopher Bower, and Peter Ramm

Index 749