1 Introduction to Nanoionic Elements for Information Technology

Rainer Waser, Daniele Ielmini, Hiro Akinaga, Hisashi Shima, H.-S. Philip Wong, Joshua J. Yang, and Simon Yu

This chapter provides the basic definitions of nanoionic redox-based resistive switching elements, their main switching modes, and their most important performance parameters. Furthermore, it sketches the scope of this book, which spans from nanoscale physics and chemistry of the switching phenomenon to devices, technology, and application areas. Three types of redox-based resistive switching elements are introduced, and a brief history of the phenomenon and the designated device application is given. This is followed by a discussion of the performance requirements and the specific themes of the application in memories and of the application in logic circuits, concluding with prospects and challenges.

1.1 Concept of Two-Terminal Memristive Elements

1.1.1 Classifications Based on Behavior, Mechanisms, and Operation Modes

Resistive switching denotes reversible phenomena of two-terminal elements, which change their resistance upon electrical stimuli in a nonvolatile fashion [1]. The *reversibility* is achieved by repeated applications of suitable stimuli, which control the resistance value between two or more levels. *Nonvolatility* means that the resistance change remains for a (long) retention time after the stimulus has been released. Phenomenologically, the stimulus affects an internal state variable of the element, which controls the resistance. For this reason, the resistance values are memorized by the elements, which are, therefore, also called *memristive elements* or *devices* [2]. The required switching speed and the retention times depend on the area of application and will be discussed later.

The fundamental physical principles of resistive switching and, hence, the nature of the internal state variable can be manifold. In a coarse-grained classification, one can distinguish between nanomechanical phenomena [3],

Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications, First Edition. Edited by Daniele Ielmini and Rainer Waser.
© 2016 Wiley-VCH Verlag GmbH & Co. KGaA. Published 2016 by Wiley-VCH Verlag GmbH & Co. KGaA.

magnetoresistive effects such as spin-transfer torque (STT) [4], electrical effects such as leakage current through flash gate stacks in which trapping/detrapping phenomena occur [5], phase change between amorphous and crystalline phases [6], and *nanoionic redox phenomena* [7]. This book exclusively covers the last one, that is, ionic motion over nanoscale dimensions in two-terminal elements, which leads to local redox phenomena and, in turn, affects the resistance of the elements. Purely thermal resistance changes, which rely on the heat capacity of the elements after a temperature increase due to an electrical stimulus (as, e.g., in PTC thermistors), are not typically called resistive memories because the retention times related to the time constant of the temperature relaxation are too short.

Throughout this book, we will often use the term *redox-based resistive switching random access memory* (usually called *ReRAM*), in particular, if binary elements (i.e., elements that utilize *two* logic levels) are addressed, despite the fact that these elements may be used for functions beyond pure memory, that is, in the area of logic functions in various computational concepts. The term *memristive* will preferentially be used to describe the general characteristics of these elements and for applications of multilevel or analog features. In a more general sense, we will use the terms: resistive switching or memristive phenomena, elements, cells, devices.

Depending on the specific type of ReRAM, different operation modes have to be used. Figure 1.1 shows schematically characteristic current–voltage ($I-V$) diagrams recorded by periodic voltage sweeps (left) and pulse sequences with voltage pulse excitation and current responses (right). By far, the most device applications will use the *pulse mode*. However, the *I-V sweep mode* is helpful for obtaining an overview of the characteristics and for determining the (very) approximate threshold voltages V_{th} for the pulse operation. The resistance states of a ReRAM cell are called high resistance state (*HRS*) or *OFF state* and low resistance state (*LRS*) or *ON state*. For multilevel operation, intermediate resistance states are utilized as well. We assign the logic “0” state to the HRS and the logic “1” state to the LRS. A *write operation* changing a ReRAM cell from the HRS to the LRS is called a *SET operation*, while the opposite write operation is called a *RESET operation*. It should be noted that ReRAM cells often need an *electroforming* (short: forming) step prior to their first write/read operation. This electroforming step involves different voltage and current level than the write/read operations.

Most ReRAM systems reported in the literature are operated in the *bipolar resistive switching* (*BRS* or *BS*) mode (Figure 1.1a). Starting in the HRS, a SET process can be triggered by a voltage $V_{SET} > V_{th1}$, which leads to the LRS. Often, a current compliance (cc) is used for the SET operation in order to avoid damage to the cell and to optimize the operation. A read operation is performed at a much smaller voltage magnitude V_{rd} to detect the current while avoiding a detectable change of the state. A voltage signal V_{RES} of opposite polarity and an amplitude $V_{RES} < V_{th2}$ is used for the RESET process to switch the cell back into the HRS.

The *unipolar resistive switching* (*URS* or *US*) mode (Figure 1.1b) is characterized by the fact that all write and read operations can be performed with only one voltage polarity. Starting in the HRS, the SET process takes place at a voltage

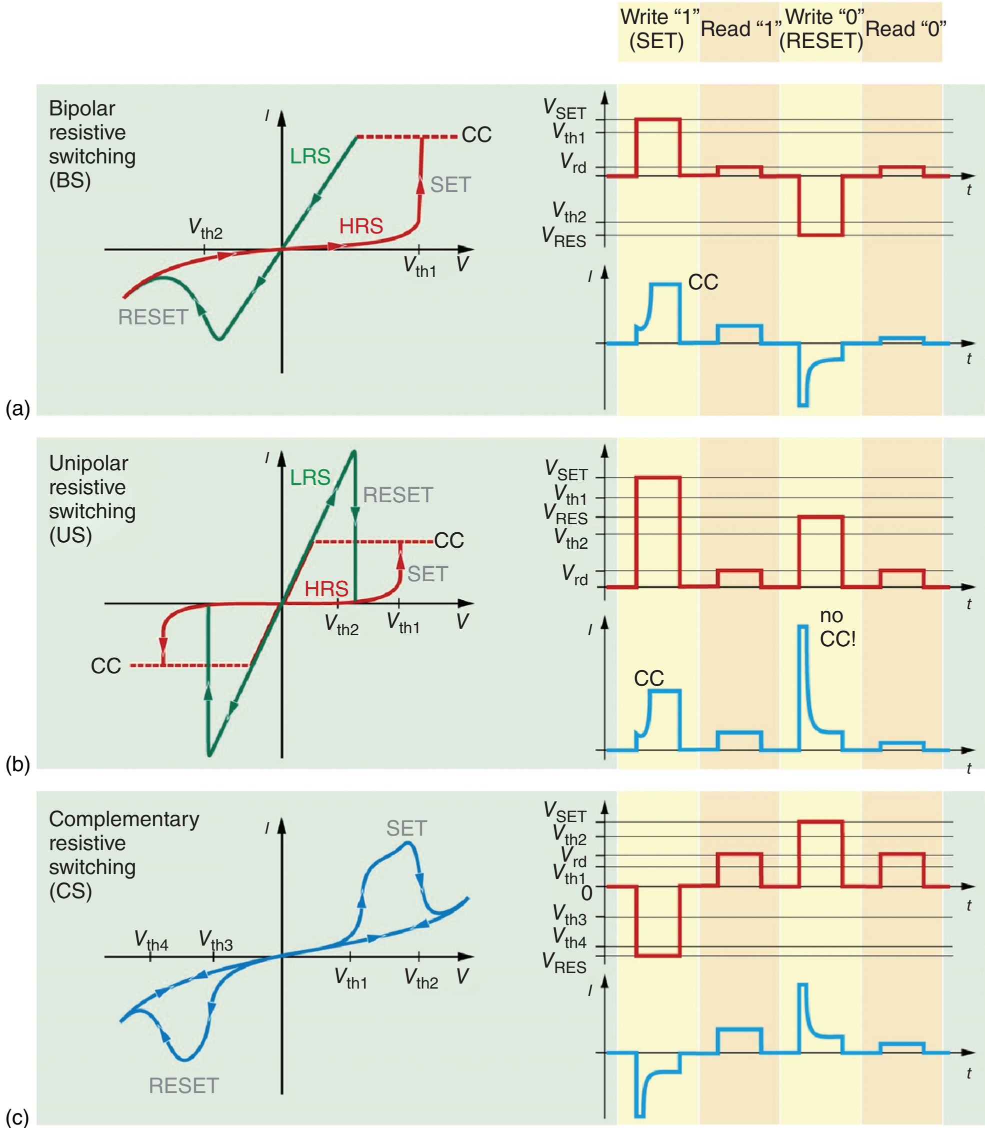


Figure 1.1 The three most common operation modes of different types of ReRAM elements shown for the *I-V* sweep operation (left) and the pulse operation (right). Details are described in the main text. Please note that the elements are nonvolatile. At first glance, the CS (CRS) mode resembles the so-called threshold switching, which shows a hysteresis above a certain voltage bias but which disappears at voltages below this bias. The difference is the fact that the information is lost in the case of a threshold bias while it is maintained in a CRS cell and can be read out in the indicated manner. (From Ref. [8].)

$V_{SET} > V_{th1}$, with a LRS current limited by a cc. It is important that the cc is released in the RESET process with $V_{RES} > V_{th2}$, so that the current can exceed the cc value, which leads to changing back into the HRS. The read operation is performed at a small voltage V_{rd} as in the bipolar operation.

The *complementary resistive switching* (*CRS* or *CS*) mode (Figure 1.1c) can be obtained by connecting two BRS-type ReRAM cells in an antiserial manner as suggested by Linn *et al*. [9]. In some cases, such a CRS behavior is also obtained by suitable processing and operation of single ReRAM cells [10]. Typically, the state of a CRS cell cannot be read at small voltages because the cell then always appears to be in a HRS. The state of the cell is only recognized at voltages $V > V_{th1}$. A read voltage $V_{rd} > V_{th1}$ will lead to a higher current (upper *I-V* trace in Figure 1.1c, left) in the case of a logic "1" state and to a lower current (lower *I-V* trace in Figure 1.1c, left) in the case of a logic "0" state. The write "0" is obtained by a positive voltage $V_{wr} > V_{th2}$, and a write "1" is obtained by a negative voltage $V_{wr} < V_{th4}$. Because of the relative high read voltage amplitude $V_{rd} > V_{th1}$ and the corresponding currents, the internal state is affected by the read operation, that is, the read voltage may destroy the logic state (the so-called destructive readout, DRO). As a consequence, the last logic state needs to be rewritten into the cell after every read operation. This is the same situation as in the case of the standard (volatile) dynamic random access memory (DRAM) cells.

The major performance parameters of ReRAM devices are:

- *Resistance Values*: R_{LRS} and R_{HRS} (or: R_{ON} and R_{OFF}) and the resistance ratio R_{HRS}/R_{LRS}.
- *SET and RESET Voltages*: V_{SET} and V_{RES}, respectively.
- *Write Currents*: in particular, the current in the ON state, at a voltage amplitude just above V_{SET}.
- *Write Speed*: the shortest electrical pulse able to change the resistive state.
- *Retention Time*: the time for which a resistive state is maintained without a voltage applied to the cell.
- *Endurance*: the number of switching cycles before the resistance ratio fatigues to an inacceptable value.
- *Operation Energy per Bit*: the energy required to write a cell, that is, to change its resistive state.
- *Scalability*: the geometrical size to which a cell can be miniaturized before it encounters inherent (physical) limits.
- *Stackability*: the option to stack several layers of cell on top of one another by fabrication technology.
- *Multilevel Storage*: the option to store more than one bit of information in one cell.

A *microscopic analysis* of ReRAM cells reveals that the electrodes and, in particular, the material "I" between the metal electrodes M in the metal–insulator–metal (MIM) structure of the cell participate in a different manner in the resistive switching process. Typically, MIM structures are sandwich stacks. But, additionally, lateral MIM structures on surfaces and metal electrodes

are used as scanning probe tips, in particular for research purposes. Without addressing the physics and chemistry of the switching at this point, one can distinguish the categories of the locations of the switching event in a MIM stack. Along the path from one electrode to the other (which we will call the vertical direction), one can distinguish the switching locations:

- at/near one of the electrode interfaces
- at the (approximate) center between the electrode interfaces
- involving the entire path between the electrode interfaces.

In the perpendicular direction, that is, in the plane of cross section of the cell (which we will call the lateral direction), one can distinguish:

- *filamentary switching*, that is, switching by the formation and dissolution of a single *conducting filament* (CF),
- *area-proportional switching*, that is, a switching event that takes part over the entire cross section of the cell so that the currents become proportional to the cross-sectional area of the cell. Because this switching typically occurs close to one electrode, it is also called *interface-type switching*.

Figure 1.2 illustrates these scenarios schematically. Of course, this brief description represents a very simple, coarse-grained classification only. In reality, many intermediate cases have been reported, such as multiple filament switching or switching areas that are relatively extended spots without spreading over the entire cross section of the cell. It should further be pointed out that these categories and combinations thereof do not occur equally. The most frequent resistive switching described in the literature is filamentary switching (with evidence provided, for example, in Refs. [11–25]). If the cell shows a bipolar operation, there are usually clear indications that the switching is localized both laterally (filamentary) and vertically (near one of the electrode interfaces).

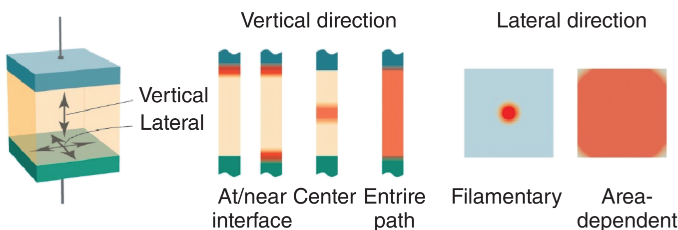


Figure 1.2 Geometrical location of the switching event in a ReRAM cell. In the vertical direction, the switching may happen close to one or both electrodes, in the center between the electrodes, or over the entire path between the electrodes. In the lateral direction, we distinguish between a localized filamentary switching and a switching that involves the entire cross section. For example, a bipolar filamentary resistive switch constituting the majority of ReRAM devices reported to date combines a localized event in the lateral direction at/near an electrode interface in the vertical direction. Still, of course, the geometries shown here are limiting cases and intermediate situations may be encountered too.

The simple ReRAM concept might resemble that of a switch, which can be settled in two different configurations to allow a current flow or not. Although apparently simple, the explanation of the physical processes responsible for the switching has not been completely unveiled at the time of publication of this book, not to mention the high complexity to achieve a working technology based on the ReRAM concept, for example, a crossbar nonvolatile memory or a logic circuit outperforming the existing technologies. The purpose of this book is to address the fundamental physics and chemistry concepts as well as the technology, circuit, and architecture-related issues of the redox-based memristive phenomena and ReRAM devices.

1.1.2
Scope of the Book

Figure 1.3 is a sketch of the book topics and structures, covering the concept, the materials involved, processes in generic cells, the types of ReRAM cells, aspects of technology, and applications.

A phenomenological introduction of ReRAM cells in the context of two-terminal devices as dynamical systems will be provided in Chapter 2.

The material properties, described in Chapters 3–6, provide the basis for understanding the *physics and chemistry* of the processes that occur during redox-based resistive switching. These chapters cover the atomic and electronic structures with an emphasis on metal oxides used for ReRAM cells (Chapter 3), the lattice disorder and defect chemistry of these materials (Chapter 4), the ionic transport mechanisms (Chapter 5), and the electronic transport properties (Chapter 6). Transport properties in fact dominate resistive switching, since, microscopically, the switching is due to the electrical and ionic transport phenomena. For instance, electrical transport is essential in the read operation, where the conductance state of the memory is probed. On the other hand, ionic transport is responsible for the change of the chemical composition profile, leading to resistance switching. Electrical and ionic transport are essential in dictating the switching time, the switching energy, and the scale of the switching phenomena, which are key parameters in assessing the potential application space of ReRAM within memory and computing circuits [26, 27].

For a more detailed description of redox-based resistive switching, however, we need to peer inside the cell, where the mass transport and chemical composition change leads to the memory effect. In this book, the fundamental phenomena taking place within a generic cell are grouped according to quantum point contact (QPC) transport (Chapter 7), controlled dielectric breakdown (Chapter 8), and several microscopic processes responsible for resistive switching such as phase formation, space-charge formation, electron transfer at electrochemical interfaces, electromotive force (emf) formation, and kinetic demixing (Chapter 9). In most cases, device operation relies on an initial forming operation, which is introduced in Chapter 10. A universal switching behavior for filamentary-type

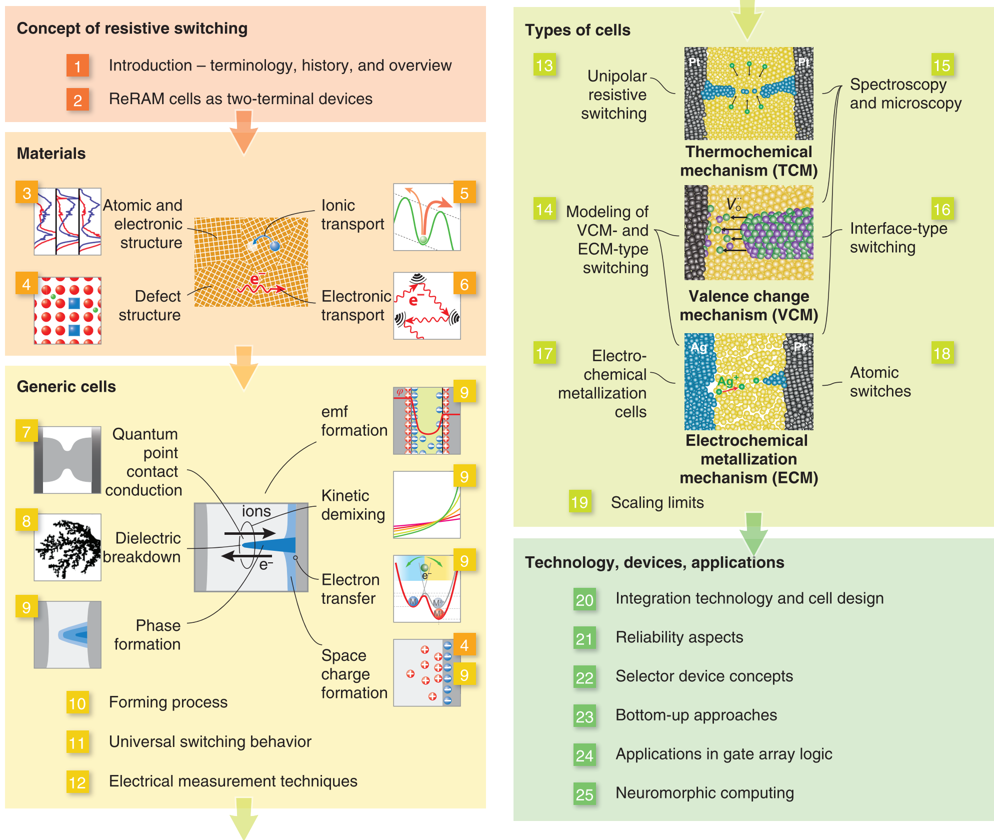


Figure 1.3 Synopses of the ReRAM concepts, materials, generic cells, ReRAM cell types, and ReRAM technology and applications. The numbers indicate the chapters in this book.

switching is introduced in Chapter 11, while an overview of the electrical techniques for device characterization is given in Chapter 12.

ReRAM cell can be classified by their basic nanoionic switching mechanism, covered in Chapters 13–16. The three main *ReRAM types* are electrochemical memory (ECM), valence change memory (VCM), and thermochemical memory (TCM). Please note that the same resistive switching material, and even the same cell, might show more than one switching behavior, for instance, the coexistence of VCM and TCM behaviors was demonstrated in TiO_2 [28] and HfO_2 [29]. This indicates that the switching behavior is dictated not only by the material type but also by the electrical operation and the type of electrodes. In general, all of the three ReRAM types display *filamentary* switching, except for VCM, which might, in addition, take place as area-dependent *interface-type* switching (Chapter 16) or even in a uniform *bulk-type* switching [30] and forming [31].

Unipolar switching in TCM devices (Chapter 13) typically takes place in metal oxides such as NiO [32] and TiO_2 [33]. Electrodes are generally inert, for example, Pt or TiN, and a forming process is needed to first initialize the ReRAM operation. SET and RESET processes are induced by applying voltage signals of the same polarity. For this reason, TCM is believed to result from purely chemical redox transitions, where a metal-rich CF is formed by local reduction of the metal oxide, while the CF is then dissolved by local oxidation, possibly in combination with a surface tension controlled Rayleigh instability of the CF. Both reduction and oxidation are accelerated by the high temperature developed at the CF by Joule heating [34, 35].

Microscopic models to describe the two BRS mechanisms, the VCM-type and the ECM-type switching, are presented in Chapter 14. VCM cells are based on metal oxides sandwiched between metal electrodes of different oxygen affinity and/or work functions. Similarly to TCM, the cells must typically first be initialized by the forming process, consisting of a controlled dielectric breakdown that generates active ionic defects and typically leads to the formation of a reduced oxygen-deficient CF phase with a valence change in the cations and a corresponding increase in the electronic conductivity. The ionic defects can then migrate over nanoscale distances in response to an applied voltage, allowing for the formation and disruption of the CF under bipolar voltage operation. The VCM process is investigated by spectroscopical and microscopical methods (Chapter 15). Cases of an interface-type VCM mechanism are covered in Chapter 16.

In ECM cells, the MIM stack includes at least one electrochemically active metal electrode, of which the most typical case is Ag or Cu. Under a positive applied voltage, the active electrode can oxidize and release cations in the "I" layer, also known as the solid electrolyte. Cations (Ag^+, Cu^{z+}) then migrate to the negatively biased counter electrode, where they get reduced back to the neutral state and grow as a CF or bridge. In the literature, the ECM devices are also called Conductive Bridge RAM, short: CBRAM. The formation of the CF corresponds to the SET process. The bridge can then be electrochemically dissolved under a negative voltage applied to the active electrode as the RESET process. The general form of ECM cells is covered in Chapter 17, whereas those that emphasize the atomic contact of the metallic CF and conductance quantization are called *atomic switches*, described in Chapter 18.

All ReRAM types are subject to scaling rules and ultimate physical limits of scaling, which are discussed in Chapter 19.

To achieve functional and cost-effective electronic circuits, ReRAM must be integrated with complementary MOS (CMOS) digital circuits by process technology and designed to match the specifications of certain applications. Cell design and integration technology based on top-down approaches, such as optical lithography, as well as 3-D integration concept for further increasing the device density per area on the chip are covered in Chapter 20. Highly important topics in the ReRAM area are the reliability with respect to endurance, retention, random telegraph noise, and disturb error as well as variability (Chapter 21). A main advantage of ReRAM for memory applications, compared to CMOS

technology, is the two-terminal architecture, which allows a small device area of only $4F^2$ (F is the lithographically defined minimum feature size) in the crossbar array [36]. However, implementation of ReRAM in the crossbar array requires that each resistive switching device is accompanied by a selector (Chapter 22), to prevent inevitable interference during read and program between array cells [9]. Besides the top-down integration technology described in Chapter 20, there are techniques based on bottom-up approaches utilizing chemical and physical methods of self-assembling and self-aligning of structures (Chapter 23).

Beyond memory applications, ReRAM devices have been proposed for the use in logic circuits. One area is the logic based on field-programmable gate arrays (FPGAs) where ReRAM devices can be employed in the configuration array and for routing switches (Chapter 24). Finally, ReRAM devices hold the promise that they can be used for artificial synapses in neuromorphic computing circuits (Chapter 25).

1.1.3
History

From a historical point of view, resistive switching has been studied in various solid-state materials since the early 1960s. Most typically, very early reports on resistive switching emphasized the negative differential resistance occurring in the I-V characteristics of MIM structures. The "I" in the MIM stack can be one of the various binary and multinary oxides, chalcogenides, as well as group-IV, III–V, and II–VI semiconductors. In 1962, Hickmott reported a large negative resistance in MIM stacks with oxide insulator, such as SiO_x, Al_2O_3, Ta_2O_5, ZrO_2, and TiO_2 [37]. The negative resistance effect in oxide-based MIM structures was explained by a space-charge-limited current in the oxide layer. In insulators, the trapping of electrons in localized states influences the space-charge-limited current [38]. A double injection model was proposed by considering that the lifetimes for the injected electrons and holes were different in insulators and vary with injection level [39]. This model explained the curve of the negative resistance and showed the possibility of spontaneous oscillations under the application of an appropriate DC voltage or an apparent breakdown at some critical voltage followed by a marked hysteresis in the current with decreasing voltage after the breakdown.

Bistable resistance switching was reported in 1964 in NiO thin films on Ni substrate, where the switching was believed to be due to the formation and rupture of a nickel metallic filament in the NiO layer sandwiched by two electrodes [40]. Later in 1965, bistable resistive switching between two stable resistance states was shown in Nb_2O_5 [41]. Figure 1.4 shows the reported *I-V* curves Bi/Nb_2O_5(125 nm)/Nb, measured after formation (dielectric breakdown) of the initially insulating stack. Upon a first positive voltage sweep, the device is in an LRS (a). Application of a negative voltage leads to a RESET transition to high resistance (b), while application of a positive voltage causes the SET transition to the initial LRS (c). The bipolar switching is bistable in that both states are stable.

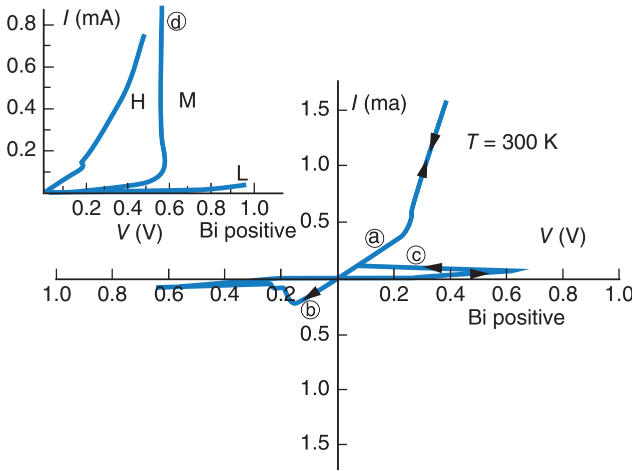


Figure 1.4 Measured *I-V* characteristics for an Nb–Nb_2O_5–Bi MIM stack showing bistable resistive switching. The device is initially in a low resistance state (a) due to the previous forming operation. Reset transition to the high resistance is shown for negative applied voltage (b), while set transition to the low resistance appears at positive voltage (c). The inset shows the *I-V* curves of three stable states: a high resistance state H, a low resistance state L, and an intermediate state M (d). (Redrawn after Ref. [41].)

Studies on bistable resistive switching have also been reported for thin films of Ta_2O_5 [42], SiO [43], TiO_2 [44], and Al_2O_3 [45] and for ZnSe–Ge heterostructures [46]. The first report on what we today classify as ECM-type switching dates back to 1976 when Hirose and Hirose observed Ag dendrites being formed and dissolved between the Ag and Au electrodes in a bipolar operation mode of lateral Ag/As_2S_3/Au cells [47]. This early period of research faded in the late 1970s. Obviously, the interest in this area decreased because of the overwhelming progress of the Si-based integrated circuit technology, in particular, the Flash memories. In 1967, Kahng and Sze invented the floating gate MOSFET as a nonvolatile three-terminal device [48], which was developed into an EPROM (erasable programmable read-only memory) in the 1970s and into a flash memory in the 1980s. Flash memories have developed into dominant nonvolatile solid-state storage since the turn of the millennium. Another reason for the decrease in research on metal oxides and related compounds was presumably the lack of progress in understanding and controlling the resistive switching phenomena possibly due to insufficient analytical tools at that time. This period has been reviewed comprehensively by Dearnaley *et al.* [49], Oxley [50], and Pagnia and Sotnik [51].

A new era in research on resistive switching gradually started in the mid-1990s. The Tokura group found electrically triggered resistive switching in $Pr_xCa_{1-x}MO_3$ (PCMO) while investigating the magnetoresistive properties of this material [52], and Zhuang *et al.* used this material to fabricate the first integrated ReRAM memory, a 64-bit array, using a 500 nm CMOS technology [53]. In 2000, the

IBM Zurich lab reported the resistive switching of perovskite-type zirconates, including many properties that are essential to non-volatile memory (NVM) applications [54]. In the ECM-type area, Kozicki, Mitkova *et al.* started to study the Ag-GeSe systems in the late 1990s [55], while the Aono group published their first report on the so-called atomic switches in 2001 [56]. These devices make it possible to control the electrochemical formation and dissolution of, for example, an Ag atomic bridge in a nanogap between a mixed electronic–ionic conducting Ag^+ electrolyte and a metal electrode with the precision of Landauer conductance quantization [57]. In 2004, Samsung successfully demonstrated a high-density ReRAM chip using a 180 nm technology. It was based on unipolar switching Pt/NiO/Pt cells with an endurance of 10^6 SET/RESET cycles. These and related papers have been the beginning of an unprecedented rise of R&D activities, which led to the mega-trend that we encounter in the 2010s.

While there has been a basic understanding of the ECM mechanism from the beginning, a broad spectrum of mechanisms have been suggested as the underlying mechanisms of resistive switching in various metal oxide systems. In 2006, Waser's group was able to clarify the effect as a motion of oxygen ions and a coupled valence change in the cation sublattice on the nanometer scale at structural defects in the crystal lattice of the metal oxides near one electrode [58]. For this reason, the term VCM effect was suggested for bipolar metal oxide systems [59], extending the more detailed classification of the nanoionically driven, redox-process-based resistive switching memories [60]. The first spectroscopic evidence for the valence change was published for the dopants of Cr-doped $SrTiO_3$ by Janousch *et al.* [61] and for the host cation in TaO_x-based cells by Z. Wei *et al.* [62]. The filamentary nature of an oxygen-deficient phase generated during the forming process was shown by Kwon *et al.* [63] using high-resolution transmission electron microscopy. In 2008, Williams' group at the Hewlett-Packard Labs discovered that the electrical characteristics of resistive switching elements can be described in terms of the theory of memristive devices [64]. This theoretical concept was published in 1976 by Kang and Chua [2] as a generalized version of the theory of memristors introduced by Chua in 1971 [65], and this link led to a further increase in the international research activities.

Further historical notes will be given in the forthcoming part of this introduction and, in particular, in the individual chapters of this book. The technological realization has advanced to the point that a VCM-type 32 GB ReRAM chip was presented by Sandisk and Toshiba in 2013 [66], and an ECM-type 16 GB ReRAM chip was introduced by Micron and Sony in 2014 [67].

As a guidance for a further understanding of the nanoionic redox-based resistive switching elements covered in this book, it should be mentioned that there are other two-terminal resistive switching material systems based on different switching mechanisms: (i) Ferroelectric Schottky diodes were proposed as bipolar switching memory devices by Esaki *et al.* in 1971 [68]. A first realization based on epitaxial $PbTiO_3$ films grown on electronically conducting oxides was reported by Blom *et al.* 1994 [69]. These activities led to resistively switching ferroelectric and multiferroic tunnel junctions, briefly covered in Chapter 15. (ii) Ovshinsky

described a unipolar, thermally driven switching between the amorphous and the crystalline phase of Ge-Te-based compositions in 1966 [70, 71], which became important for rewritable optical storage media in the 1990s and as phase-change memories (PCMs) in the mid-2000s. (iii) For several decades, there have been reports on *organic* materials that show resistive switching (see e.g., Ref. [72]). In some prominent cases, it was discovered later that the switching, in fact, takes place in an oxide layer formed on an electrode metal used to contact the organic material. For example, Cu : TCNQ films sandwiched between Cu and Al electrodes [73] were found to switch resistively because of an ECM effect in the Al_2O_3 layer built during the processing of the system [74]. A similar situation was encountered for rose Bengal films between Al and Zn or indium tin oxide (ITO) electrodes [75] for which the resistive switching presumably is caused by a VCM-type effect in the metal oxide layer of one of the electrodes [76]. (iv) Nanosized dispersions of electronically conductive phases, for example, metals such as Pt, in insulators such as SiO_2 have also shown pronounced BRS effects if sandwiched between asymmetric electrode materials (e.g., Pt/SiO_2 : Pt/Mo) and if the film thickness is close to the percolation threshold [77]. These systems have been described in terms of a purely electronic trap charging/discharging model for which, however, the origin of the highly nonlinear switching kinetics (see Section 1.2.1) needs to be further clarified. A clear electronic trap mechanism is found in the bipolar MemFlash cells, which are conventional flash memory cells with the source and gate contacts connected in order to obtain a two-terminal device [78]. Although this concept inheres the properties of flash cells with respect to write speed and write voltages, it may be further developed in order to match the requirements of neuromorphic devices [79]. (v) For narrowband-gap Mott insulator compounds AM_4X_8 (A = Ga, Ge; M = V, Nb, Ta; X = S, Se), a URS effect has been reported, which is apparently related to a Mott insulator – metal transition triggered by an electronic avalanche effect above a critical field strength. This effect may be described as an electronic phase-change effect in the crystalline phase in combination with local strain [80]. There are further reports about other purely electronic resistive switching mechanisms based on electron correlation, for example, the unipolar switching of NiO [81]. Further clarification of these effects is subject to ongoing research at the time of the publication of this book.

1.2 Memory Applications

1.2.1 Performance Requirements and Parameter Windows

This section reports on the major parameters of ReRAM devices for various types of memory applications and, in some aspects, also for logic concepts. The demonstrated and the expected performance of ReRAM devices are compared to the performance of alternative nonvolatile device technologies.

The development of oxide-based VCM-type ReRAM has progressed rapidly since the mid-2000s. In particular, binary oxides using materials that are familiar to the semiconductor industry have seen intense research and development in both industry and academia. The objective of an oxide ReRAM is a non-volatile memory that is fast, high-density, and compatible by integration with conventional silicon CMOS technology. The early ReRAM had large device areas ($\gg \mu m^2$), large programming currents (> mA), long programming times (> μs), and low endurance ($<10^3$ cycles). Over the years, many of these drawbacks have been overcome.

Great *scalability* is a major differentiator of ReRAM from other competing technologies, including commercialized technologies such as Flash, SRAM, and DRAM, as well as some prototype and niche technologies such as magnetoresistive memory (e.g., STT-MRAM) and ferroelectric memory (FeRAM). Device sizes down to $10\,nm \times 10\,nm$ have been demonstrated [82]. The scalability into the single-digit nanometer regime arises from the fact that the resistance change in ReRAM is usually associated with ionic motions within a much more localized structure, which could be as small as a nanometer or less [58, 83]. This is one of the reasons that makes ReRAM a highly promising technology.

Reading of ReRAM devices is *nondestructive* (nondestructive readout, short: NDRO). This differs from other memories, such as FeRAM, where every read operation changes the information stored in the device and requires a restore cycle. The *resistance ratio* (also called: resistance window) is usually fairly large for ReRAM, usually between 10 and >1000. Presumably, this is because a small change in ion positions may induce exponentially large changes in the electronic conductance of the cell. Compared with the resistance window of magnetic RAMs (MRAMs), which is typically less than 5, the large R_{HRS}/R_{LRS} ratio of ReRAM offers a larger sensing margin.

The absolute values of the R_{HRS} and, in particular, of the R_{LRS} are of importance too when it comes to the design of ReRAM circuits. They have to be compared to the bit line resistance R_{BL} and the resistance of the select device R_{SD}, such as a transistor in the ON state in the case of an active matrix. The bit line capacitance C_{BL} has to be taken into account as well. For example, if one considers a 512×512 matrix and an $F = 10\,nm$ technology, then C_{BL} and $(R_{BL} + R_{SD})$ are in the range of 30 fF and $1-10\,k\Omega$, respectively. For a read voltage of 0.3 V and a read speed of $t_{rd} < 100\,ns$, one can estimate a read current of >100 nA and a maximum R_{LRS} of approximately 300 kΩ. Please note that, as a consequence, the current density across the $10\,nm \times 10\,nm$ ReRAM cell will be as high as $10^5\,A/cm^2$. For a reasonable sense voltage margin, the minimum R_{HRS} needs to be approximately 500 kΩ. The minimum value of R_{LRS} is obtained by the write operation in which a sufficiently large voltage must drop over the cell, that is, $R_{LRS} > (R_{BL} + R_{SD})$ should be fulfilled. Details are provided, for example, in Refs. [26, 84, 85].

These resistance values and the current density should be kept in mind, when possible switching mechanisms are compared and also, for example, when promises made in the literature concerning the scalability of area-proportional, interface-type ReRAM concepts are to be judged.

The write speed of ReRAM is typically in the order of nanoseconds or tens of nanoseconds, which is orders of magnitude faster than the write speed of Flash cells. In dedicated studies, ReRAM devices have been observed to switch as fast as 100 ps [86] and potentially even faster. One possible reason for the ultrahigh speed is that the distance for the ionic species to move during switching is likely to be fairly short, approximately a nanometer or less. The other key reason is that the nanoscale active region inside the switching oxide material is under very high electric field for enhanced ion mobility [87] and is heated up during switching by Joule heat [88], which greatly increases the mobility of the ionic species and enables fast switching. Upon removing the switching electrical pulse, the heated region cools down very quickly, probably within a nanosecond, and the mobility of the ionic species drops to a very low level again. This leads to a great *retention* at relatively low electrical bias and temperature. Long retention times are kept under read voltage bias, because a low voltage bias avoids any temperature and field acceleration of the ions and, hence, their mobility stays very low.

The required *ultrahigh nonlinearity of the switching kinetics*, that is, nanosecond switching types for a certain write voltage and many years of retention even if constantly read out at, for example, 1/10th of the write voltage, represents a challenge for many proposed mechanisms. In many papers, purely electronic switching mechanisms have been suggested based on the idea of trapping/detrapping charges in the “I” layer of the MIM stack of ReRAM cell, obviously inspired by the flash memory. However, in contrast to the gate dielectrics, the “I” layer in a ReRAM cell is highly conductive. Hence, excess charges stored by trapping or detrapping can only be kept for an extremely short retention time. In a very coarse approach, this can be compared to the idea of storing excess charge on a very leaky capacitor in which the RC time of the device determines the retention time. Details are provided in Ref. [89].

The reports on the maximum number of switching cycles, the *endurance* of ReRAM cells vary a lot. An endurance of 10^{12} cycles has been reported for a TaO_x-based VCM cell [90]. Typically, 10^6-10^8 cycles are reported, which by far excels highly dense NAND flash, which shows 10^3-10^5 cycles.

Another key parameter for any nanoelectronic device is the *operation energy per bit*. The energy consumption in reading memory cells is normally not a concern since it is usually much lower than that of write operation. There is not much ability to reduce energy by reducing switching voltages because the switching voltages are close to each other even for different ReRAM types. In contrast, the switching current can be significantly reduced by reducing the device size or optimizing the switching materials. Furthermore, it varies tremendously by the ReRAM types. While TCM devices often need switching currents in the milliampere range, ECM cells can be tuned to switch at currents below 1 nA (with low retention). As an example of VCM, TaO_x-based nanodevices (50 nm × 50 nm) can switch at sub 2 ns times under sub 2 V with less than 10 μA, resulting in a sub pJ/bit operation energy [91].

In many ReRAM devices, the device resistance can be switched to any value in between HRS and LRS, displaying an analog behavior. This analog switching

behavior can be utilized for *multilevel storage*, that is, to store more bits per cell [92, 93]. Landauer conductance steps may be regarded as natural levels for ultimately scaled devices, as demonstrated by ECM-type atomic switches [57]. Multilevel storage serves as the basis for analog computing and neuromorphic computing [94, 95].

There are no exotic materials or processes involved in many of the ReRAM device concepts. The fabrication processes and the materials are *CMOS compatible*, which allows for the integration of these devices with CMOS chips in a normal CMOS fabrication. Because of the materials involved, *stackability* is feasible for most of the ReRAM types. The device stack may be as simple as a conductor/insulator/conductor trilayer, and all the layers can be polycrystalline or even amorphous. The practical limitation of the number of layers that can be stacked is the alignment and the electrical addressability of these stacked layers. Some details are sketched in Section 1.2.3, and more details in Chapter 20.

In comparison with ReRAM, three prototypical memories, parameters for FeRAM, STTRAM, and Phase change RAM (PCRAM), are summarized in Table 1.1. While FeRAM was the first to be commercialized, its difficulties in scalability make it a poor candidate for high-density memory applications, despite its excellent latency, power, and endurance characteristics. STTRAM is a very promising candidate to reduce the power consumption of the memory system, particularly for embedded applications, coming from the highest performance among emerging memories in terms of speed and endurance. On the other hand, the complexity of the materials involved and their scalability including the thermal stability, the low write power, and the resistance distributions (e.g., the low ON/OFF ratio) are current challenges. PCRAM has a certain advantage regarding the 3D integration, because PCRAM requires only unipolar selection device in passive arrays, instead of bipolar selectors for ECM- and VCM-type ReRAM (see Section 1.2.2 and Chapter 22). Overall, ReRAM shows many advantages, also in comparison with the flash technology. In Table 1.1, the major performance parameters are outlined for the three types of ReRAM for 2009 and 2015.

While ReRAM has the potential to be a *stand-alone*, high-capacity, nonvolatile memory technology, it may be even more suitable for *embedded applications.* This is because it offers the low programming voltage that flash does not provide in combination with a speed that is comparable to that of DRAM. For example, an 8T2R nonvolatile SRAM (static random access memory) cell with two ReRAMs at two storage nodes of SRAM has been demonstrated for dynamical power management [97]. The ability to position a ReRAM at the contact vias of the MOSFET without extensive process steps [98] is also an attractive device feature, especially for embedded applications where only a low memory capacity, multiple-time programmable, nonvolatile memory is required. Therefore, there is an enormous opportunity to completely rethink the design of the system to gain new functionalities and even orders of magnitude improvements in speed and/or power consumption. In 2013, Panasonic released the first microcontroller with embedded ReRAM [99].

Table 1.1 Potential of the current and emerging nonvolatile memory candidates.

Parameter	FeRAM	STTRAM	PCRAM	ReRAM			
					Year	ECM (CBRAM)	VCM (Bipolar redox)	TCM (Unipolar redox)
Maturity	◎	◎	◎	◎	2015	Product	Product	Research
					2009	Prototype	Research	Research
Scalability/CMOS process compatibility	▲	●	◎	◎	2015	20 nm	5 nm	35 nm
					2009	90 nm	180 nm	180 nm
3D integration	▲	●	◎	◎	2015	–	Demonstrated	–
					2009	–	–	–
Endurance	●	◎	●	●	2015	$>10^{10}$	$>10^{12}$	$>10^{6}$
					2009	$>10^{9}$	$>10^{6}$	$>10^{6}$
Retention	●	●	●	◎	2015	>10 years	>10 years	>10 years
					2009	>10 years	>8 months	–
Latency	◎	◎	◎	◎	2015	<1 ns	<1 ns	5 ns
					2009	5 ns	10 ns	–
Power	◎	●	●	◎	2015	~1 pJ	~1 pJ	–
					2009	~1 pJ	~1 pJ	–
Variability	◎	●	●	●	2015	–	–	–
					2009	–	–	–

	▲	●	◎
Maturity	Research	Prototype	Product
Scalability	45 nm < F	10< F< 45	F< 10 nm
3D integration	Difficult	Possible	Feasible
Endurance	$\leq 10^{5}$	$\leq 10^{10}$	$>10^{10}$
Retention	< 1 year	< 10 years	>10 years
Latency	>10 μs	>100 ns	≤100 ns
Power	High	Medium	Low
Variability	Problematic	Reasonable	Low

Parameters for ReRAM show the situation for 2009 and 2015 to illustrate the progress in this area. Data are taken from Ref. [96] with modifications.

1.2.2
Device Isolation in Crossbar Arrays

At memory array level, one can distinguish between active arrays and passive arrays, by which the device density can be determined. In active arrays, every memory element is connected to a select transistor as in the DRAM or NOR flash architecture. Such cells are called 1 transistor – 1 resistor cells (1T1R). The 1T1R cell area ranges from $6F^2$ using aggressive DRAM-like design to approximately $18F^2$ for a very relaxed design.

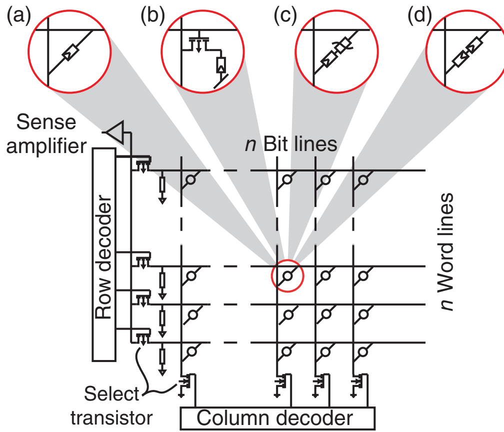


Figure 1.5 The cross-point memory architecture (a) without and (b–d) with cell selection elements. (b) Represents 1T1R cells, (c) cells with a diode or varistor type selector, and (d) a CRS cell. Details are provided in Chapter 22.

For high-density integration, a passive array with a cross-point architecture with $4F^2$ area is preferred. The simplest way is to connect the word and bit lines at each node by a ReRAM cell. A *sneak path problem* with this simple cross-point architecture may arise (Figure 1.5): if the cell to be read out happens to be in HRS with surrounding cells in LRS, the reading current can easily flow through the surrounding cells in the LRS, and, thus, an LRS data will be mistakenly read out. For further discussions about the sneak path problem and the interconnect effect on the cross-point architecture design, one can refer to Chapter 22 and Refs. [100–103]. The conclusions from these works indicate that in order to magnify the write/read margin of the memory array, larger ratio of the ReRAM resistance over the interconnect resistance is desired, thus increasing the LRS resistance is helpful. In order to further suppress the sneak paths, a cell *selection element* (also: *select device*, *selector*) with strong *I-V* nonlinearity should be added at each node. The cell selection element can be a diode for unipolar switching ReRAM as the 1 diode–1 resistor (1D1R) architecture, or a bidirectional selector (with a strong nonlinear *I-V* characteristics in both polarities, that is, a varistor or Z diode) for bipolar switching ReRAM as the 1 selector-1 resistor (1S1R) architecture. The diode or the selector effectively cuts off the leakage current paths at reversed bias or low bias, thus the interference between neighboring cells is prevented.

Here we briefly discuss the cell selection element materials. For unipolar switching, a p–n diode is the most common device for the cell selection element. Although a high-performance p–n diode is easily fabricated with the current epitaxial silicon technology for the planar device structures, it is not feasible to implement epitaxial silicon-based p–n diode with the ReRAM array at the back end of line (BEOL) in the fabrication process because it is difficult to grow epitaxial silicon on a metal layer and high processing temperatures are required.

On the other hand, amorphous silicon allows for lower processing temperatures. But it does not meet the requirement for current density for memory cell programming. Therefore, new materials need to be explored for the cell selection element, which should both allow for low processing temperatures and provide high current drivability. Compared with silicon p–n diode, oxide p–n diode is more attractive. It offers better flexibility in processing technology because it can be fabricated during BEOL processing even at room temperature. If the oxide material is oxygen-deficient with sufficient amount of oxygen vacancies (or cation interstitials), it is n-type; if the oxide material is metal-deficient with sufficient amount of metal vacancies, it is p-type. Thus, a combination of p-type oxide and n-type oxide essentially forms a p–n diode. Recently, several kinds of oxide p–n diodes [104], such as p-NiO/n-TiO_2, p-NiO/n-ZnO, p-NiO/n-InZnO, p-CuO/n-InZnO, have been demonstrated and stacked with Pt/NiO/Pt ReRAM in series, among which p-CuO/n-InZnO is regarded as the best candidate in terms of current drivability. Besides the p–n oxide diode, through oxide/electrode or oxide/oxide interface band engineering, unidirectional rectification of *I-V* for unipolar switching or bidirectional rectification of nonlinear I-V for bipolar switching can also be achieved. For examples, Schottky diode with Pt/TiO_2/Ti/Pt stack has been integrated with Pt/TiO_2/Pt unipolar ReRAM [105], Ni/TiO_2/Ni bidirectional selector has been integrated with Ni/HfO_x/Pt bipolar ReRAM [106], and Pt/TaO_x/TiO_2/TaO_x/Pt bidirectional selector has been integrated with Cu/HfO_x/Pt bipolar ReRAM [107]. A MIM tunnel diode based on atomic layer deposition (ALD)-processed Ta_2O_5 has been used for a bidirectional selector [108].

In addition, some materials with metal–insulator transition (MIT) such as VO_2, NbO_2, and Ti_2O_3 can be used for selectors as well. Unlike ReRAM devices, the resistive switching behavior in MIT materials is not bistable, and it is referred to as threshold switching. The threshold switching is not polarity dependent; thus, it is suitable for bipolar switching ReRAM. The sharp increase in current by orders of magnitude when reaching the threshold voltage shows an ideal behavior of a selector device. Pt/VO_2/Pt selector has been integrated with NiO unipolar ReRAM [109] and ZrO_x/HfO_x bipolar ReRAM [110]. However, VO_2 has a transition temperature of around 67 °C, beyond which the threshold switching behavior disappears [111], which is a major drawback for practical applications. Alternatively, NbO_2 has a transition temperature around 800 °C; thus, it is more attractive due to its thermal stability. W/NbO_2/Pt selector has been integrated with NbO_x [112] and a Pt/TaO_x/TiO_{2-x}/Pt with TiO_{2-x} [113] in bipolar ReRAM, respectively. The primary concern with this type of selector is operation energy since phase transitions in MIT materials are generally believed to be driven by Joule heating [114]. If the ReRAM device is in its LRS state, even a reading operation needs to turn on the negative differential resistance (NDR) device once. In addition, the endurance of NDR devices might also be a potential issue [115].

Alternatively, Cu ion motion in the Cu-containing mixed ionic electronic conduction (MIEC) materials also shows a good selector behavior for bipolar switching ReRAM [116].

Table 1.2 Representatives of selection devices for ReRAM in the literature.

Type	Stack	Voltage range (V)	Current drivability ($A\,cm^{-2}$)	Ratio
p–n diode	p-CuO/n-InZnO [104]	−2 to +2	3×10^4	3×10^4
Schottky diode	$Pt/TiO_2/Ti/Pt$ [105]	−2 to +2	3×10^5	2.4×10^6
Bidirectional selector	$Ni/TiO_2/Ni$ [119]	−4 to +4	10^5	10^3
Bidirectional selector	$Pt/TaO_x/TiO_2/TaO_x/Pt$ [107]	−2.5 to +2.5	3.2×10^7	10^4
MIT	$Pt/VO_2/Pt$ [110]	−0.5 to +0.5	6×10^6	50
MIT	$W/NbO_2/Pt$ [112]	−1.5 to +1.5	2×10^6	50
Bidirectional selector	MIEC [116]	−0.5 to +0.5	5×10^4 a)	3×10^3

The voltage range states the maximum voltage where the current density is measured. For diodes, the ratio is defined as the forward/reverse current at the maximum voltage. For bidirectional and MIT selectors, the ratio is defined as the current at maximum voltage over half of the maximum voltage.

a) MIEC has a higher current drivability $\sim50\times10^6\ A/cm^2$ at pulse mode (1.6 V).

Last but not least, two ReRAM devices can also be stacked antiserially (head-to-head) to form a CRS [9]. Under a switching voltage pulse, these two devices always have opposite voltage polarities and switch in opposite directions, thus limiting the current through the device pair since there is always one device in the OFF state in the pair. This CRS device concept can also be realized in a single ReRAM device with two instead of one switchable interface [117, 118]. The disadvantage of this scheme is that it becomes difficult to operate these switches as multilevel cells or analog devices. A destructive read is also much more in demand for device endurance in this scheme.

Table 1.2 compares several aforementioned selection element candidates in aspects of voltage range, current drivability, rectifying ratio. Although the reported diodes or selectors show a promising current drivability and rectifying ratio, many of them use Pt in the stacks, which is not CMOS fabrication process-friendly.

A detailed description of all relevant selector device concepts is given in Chapter 22.

1.2.3 3-D Technology

The primary target of ReRAM is to replace flash technology, as ReRAM has significant advantages in terms of speed and energy consumption and as flash is facing scaling limitations beyond 10 nm technology node [120]. For mass-storage application, a key challenge for ReRAM is to improve the integration density in terms of cost per bit (bit cost), so it can compete with the multibit storage NAND flash.

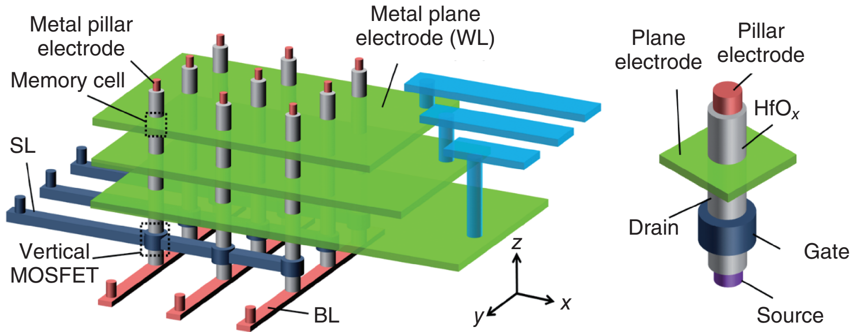


Figure 1.6 Schematic of the proposed 3D cross-point architecture using the vertical ReRAM cell. The vertical ReRAM cells are formed at the intersections of each pillar electrode and each plane electrode: the resistive switching oxide layer surrounds the pillar electrode and is also in contact with the plane electrode. To enable the random access of each memory cell, three-dimensional decoding is needed through WL (decoding in *z*-direction), BL (decoding in *y*-direction), and SL of the gate of the vertical MOSFET (decoding in *x*-direction). WL, BL, and SL denote the Word Line, Bit Line, and Select Line, respectively. (Reprinted with permission from Ref. [130].)

State-of-the-art NAND flash has been scaled down to sub-20 nm regime, and the 3D stackable NAND flash is emerging [121–123]. To achieve similar device density to that of the 3D NAND flash, a technology path toward the 3D stackable ReRAM is required. Two 3D integration approaches are available for ReRAM: one is the planar ReRAM stacked layer by layer [124]; however, it does not save lithography steps or masks because in each layer, a lithography step is needed to pattern the features, and, therefore, the bit cost remains high. The other one is the vertical ReRAM sandwiched between the pillar electrodes and multilayer plane electrodes [125–127], which requires only one critical lithography step or mask; thus, it is a more promising approach for reducing the bit cost. In 2012, Yu *et al.*, proposed a cost-effective technology path toward 3D integration (Figure 1.6) [128–130]. As a proof of concept work, a two-layer vertical HfO_x ReRAM structure was fabricated and characterized [128]. Programming schemes for random access in the 3D array were proposed and the 3D array operation was experimentally demonstrated [129]. Furthermore, the scaling trend of the 3D vertical ReRAM array was analyzed by experiments and 3D circuit simulation. More details and alternative approaches will be described in Chapter 20.

1.2.4 Memory Hierarchy

The pyramidal hierarchical structure of memories and the storage devices is shown in Figure 1.7 [96, 131]. The vertical arrows on the left and right side of the figure indicate the capacity (bit), access time (ns), and also the retention time of typical memories, respectively. Within this hierarchy, storage class memory

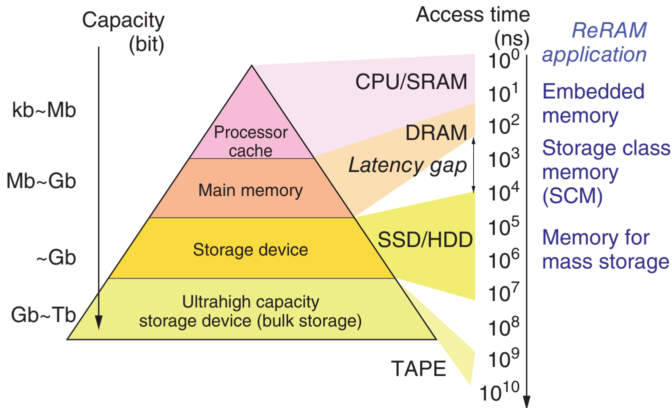


Figure 1.7 Pyramidal hierarchical structure of memories and the storage devices.

(SCM) bridges the latency gap between cache, main memories, and storage devices, such as hard disk drive (HDD) and solid-state drive (SSD). As mentioned earlier, ReRAM possesses two primary target application areas. One is the embedded application, such as microcontroller units with embedded ReRAMs [132, 133]. Another is the mass-storage application, in particular, SCM. Owing to the high possibility of the 3D integration, ReRAM is a candidate to replace the NAND flash technology [134]. As shown in Figure 1.7, the access time of DRAMs, which are used as the main memory, is 2 orders of magnitude faster than that of SSD, in which the NAND flash memory is utilized as a storage medium. Of course, architectural changes are required to utilize the advantages of SSD effectively, in terms of the low-power performance and durability. If circuit design adaption is realized, the use of SCM in mobile terminals improves the speed of data transfer within a network, enabling a marked reduction in the power consumption of the system as a whole [135, 136]. In summary, since the ReRAM technology has measured up the requirements with regard to the capacity and latency, ReRAM is the most promising candidate for SCM and beyond.

1.3 Logic Circuits

There are three main routes along which ReRAM devices are considered for application in logic operations in electronic circuits: (i) as nonvolatile switches in FPGA circuits, (ii) as logic gates, and (iii) as elements in neuromorphic circuits. These applications exploit the extreme scalability the nonvolatility of the ReRAM and also the fact that many ReRAM systems can be integrated in the so-called BEOL in the integration process, after any CMOS part is fabricated.

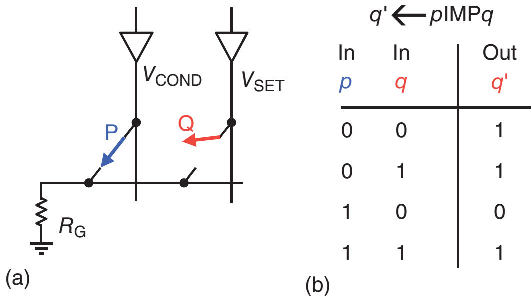
An *FPGA* consists of a logic-computing circuit where logic units are connected together by switch units, which can be reprogrammed to reconfigure the

connections and the functionality of the FPGA. In a conventional FPGA, logic cells are connected by volatile switches consisting of SRAM circuits. An SRAM circuit occupies a relatively large area of more than $100F^2$. To reduce the switch area in the FPGA, SRAM can be replaced by ReRAM devices with a minimum area of $4F^2$ [137]. In addition, ReRAM devices can be fabricated in the BEOL and, thus, can be stacked on top of the logic CMOS plane to further optimize the circuit area.

An early example of ReRAM-based FPGA is the so-called CMOL proposal, where CMOS is combined with switches that consist of molecular devices (hence the name) or any other type of ReRAM devices [138]. The crossbar array of reconfigurable nanoswitches is fabricated on top of the CMOS logic, displaying a tilted orientation with respect to the CMOS array. This peculiar architecture allows for the exact matching of the switch array size with the logic array size, to take advantage of the smaller ReRAM pitch F in order to achieve extremely high density in the switch array combined with a more relaxed pitch F_{CMOS} of the CMOS circuit. ReRAM–CMOS hybrid integrated circuits have been fabricated based on this concept. For example, ReRAM-based FPGA circuits have adopted a 1T2R architecture of the switch [139] or a complementary atom switch (CAS) structure, where two ReRAM switches are connected in parallel [140]. For application in FPGA circuits, the requirements of the ReRAM device are different from those expected for memory applications. First, the writing speed of ReRAM must be close to that of CMOS-based SRAM, which is capable of sub-nanosecond switching. Second, ReRAM resistance must be low to allow for low-voltage operation and for low RC parasitics. Finally, reliability with respect to tolerance against low-voltage disturbs must be ensured to avoid unwanted reprogramming during operation of the FPGA logic. More details are provided in Chapter 24.

Logic gates as fundamental elements for sequential binary computing have been realized by resistive switches. For instance, the Boolean function *material implication* (IMP) was implemented as a gate based on two memristive elements as shown in Figure 1.8. Here, switches P and Q are connected in parallel and initially contain the input logic states p and q. In the computational stage, pulse voltages of amplitude V_{set} and V_{cond} are applied to Q and P, respectively, where V_{set} is just above the threshold for SET transition, whereas V_{cond} is just below the same threshold. If p is 0, namely P has a high resistance, then the whole voltage V_{set} drops across Q, which thus unconditionally switches to the set state. If p is 1, namely P has a low resistance, then the voltage drop across q is just $|V_{set} - V_{cond}| \approx 0$, which cannot induce any change in q. The resulting truth table in Figure 1.8 demonstrates IMP functionality. All other logic operations can be achieved through iteration of IMP over successive cycles [141, 142], thus making it possible to achieve logic completeness. This concept has been extended to CRS cells [143, 144]. Switch-based logic gates can allow for a huge reduction of circuit area, thanks to the small size of the switch in a crossbar array, and a huge reduction in energy consumption, thanks to the nonvolatile behavior of resistance switches, which enables the normally off operation of digital circuits [145].

Another emerging application is using ReRAM cells as *artificial synaptic device* for the hardware implementation of *neuromorphic circuits* mimicking the



In p	In q	Out q'
0	0	1
0	1	1
1	0	0
1	1	1

Figure 1.8 Schematic illustration of the IMP gate implemented through two ReRAM switches (a) and the corresponding truth table (b). Memristive elements P and Q contain the input logic states p and q, respectively, then Q can conditionally switch to the output state q'. (Reprinted with permission from Ref. [141].)

biological neural operations and aiming at cognitive functionality. Neuromorphic circuits elaborate spiking neural signals through neural networks where CMOS neurons are connected by artificial synapses.

Biological neurons are formed by a cell body (soma), connected to other neurons through dendrites, which provide the input stimuli for neuron elaboration, and an axon, which transmits the output signal or “fire.” An output axon and an input dendrite are separated by an interfacial gap called synapse. Each synapse has a characteristic conductivity, or weight, describing the strength of the coupling between presynaptic and postsynaptic neurons. Therefore, neuron computation relies on both the input signals coming by the synapses and their corresponding weights. Traditionally, electronic neural networks have been developed by integration of CMOS circuits, playing the role of the neurons, with artificial synapses consisting of Si-based floating gate cells [146] or SRAM circuits [147]. Instead of the pure CMOS realization, ReRAM may take over the key functionality for artificial synapses (Figure 1.9), which is the weighted resistive connection of two neurons. ReRAM devices can be considered as binary, multilevel, or even analog switching devices, that is, the synapse conductance is changed continuously between low and high to configure the neural network. ReRAM is highly suitable for such application, since the resistance can be changed from the set state to the reset state and vice versa through a proper choice of the voltage and current. In fact, the resistance can be controlled by the maximum current during the set operation and by the maximum voltage during the reset transition [148]. Instead of voltage and current, however, the time delay between spikes is the parameter dictating the change in the synapse conductance in the biological system through the so-called spike-timing-dependent plasticity (STDP). Besides their functionality, another advantage of ReRAMs is the fact that they are two-terminal devices, that they can be strongly scaled in their size, and that they can be integrated on top of CMOS circuits in the BEOL process steps. It should further be noted that the requirements on the performance of ReRAM cell for neuromorphic

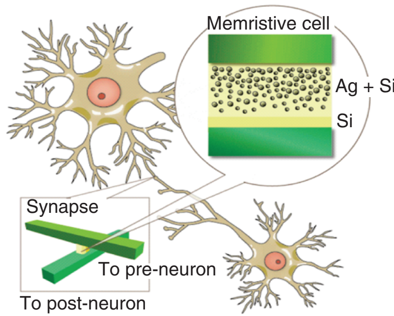


Figure 1.9 Schematic illustration of the natural (biological) and ReRAM-based artificial synapses. (Reprinted with permission from Ref. [95].)

computing such as the operation speed and the retention time may be significantly relaxed as compared to memory and FPGA applications. In addition to spiking concepts, there are also level-based concepts utilizing threshold gates, realizing, for example, content addressable memories [149] or single-layer perceptrons [150]. A common fingerprint of ReRAM-based neuromorphic systems is that they comprise hybrid analog–digital electronic circuits. Details about the different concepts of how to use ReRAM in neuromorphic computing are provided in Chapter 25.

The results published suggest that ReRAM might be able to emulate the functionalities of synapses and even entire neurons and become an essential ingredient in neuromorphic circuits, thus enlarging the spectrum of possible applications in the computing domain.

1.4 Prospects and Challenges

As described, due to their attractive properties, ReRAM devices are promising for numerous applications, including memory and storage as well as digital, analog, and neuromorphic computing. Accordingly, these applications set a variety of requirements for the devices. The device performance requirements for memory and storage applications are more demanding than, for instance, for neuromorphic applications with respect to speed, retention time, and device density. In the following, the promises of the ReRAM devices are briefly summarized. Then the focus is on the challenges and possible solutions to these challenges.

ReRAMs offer a great scalability, ultrafast switching speed, nonvolatility, large HRS/LRS window, analog resistance change, nondestructive reading, simple structures with common materials, 3D stackability, and great CMOS compatibility and manufacturability. Besides these great prospects, ReRAM devices face a number of challenges. These challenges are application dependent. The most critical issues include device isolation in crossbar arrays, device variability, and reliability.

ReRAMs face a challenge with respect to an intrinsic cycle-to-cycle variability, which is typically relatively large compared to other nonvolatile memory technologies, owing to the filamentary nature of the active region in the ReRAM and the stochasticity of the filament buildup on the atomistic scale. As a consequence, the effective memory window due to wide distributions of the LRS and HRS resistances may shrink below critical values. Of course, this strongly depends on the type of ReRAM cell, the material system, and the cell design. Another important reliability requirement is nonvolatility (retention). In general, higher resistive filaments (desired for low current operation) tend to show a reduced retention. Presumably, this is due to atomic-scale sized filaments and processes on the atomic scale affecting the filament properties, such as interdiffusion, phase formation, and interface reactions. More insights into the different reliability mechanisms are provided in Chapter 21.

In summary, based on the progress in the microscopic understanding of the electroforming and switching process, solutions to the challenges will come from a combination of materials engineering, device structure optimization, as well as innovations in addressing/readout circuitry and programming algorithm.

Acknowledgments

The authors are indebted to Stephan Menzel (FZ Jülich, Germany) for carefully reading the manuscript and for helpful discussions, to Eike Linn (RWTH Aachen, Germany) for in-depth discussions on neuromorphic computing, and to Yun-Leei Chiou (Temple Terrace, USA) for firsthand information on the history of ReRAM in the 1960s. RW would like to gratefully acknowledge the support from the Deutsche Forschungsgemeinschaft through the SFB 917 and the Leibniz Award 2014.

References

1. Waser, R. (2012) in *Nanoelectronics and Information Technology*, 3rd edn (ed R. Waser), Wiley-VCH Verlag GmbH, pp. 603–620.
2. Chua, L.O. and Kang, S.M. (1976) *Proc. IEEE*, **64** (2), 209–223.
3. Akarvardar, K. and Philip Wong, H.-S. (2012) in *Nanoelectronics and Information Technology*, 3rd edn (ed R. Waser), Wiley-VCH Verlag GmbH, pp. 375–387.
4. Dieny, B., Sousa, R., Nozieres, J.-P., Redon, O., and Prejbeanu, I.L. (2012) in *Nanoelectronics and Information Technology*, 3rd edn (ed R. Waser), Wiley-VCH Verlag GmbH, pp. 655–668.
5. Zhirnov, V. and Mikolajick, T. (2012) in *Nanoelectronics and Information Technology*, 3rd edn (ed R. Waser), Wiley-VCH Verlag GmbH, pp. 621–634.
6. Raoux, S. and Wuttig, M. (2012) in *Nanoelectronics and Information Technology*, 3rd edn (ed R. Waser), Wiley-VCH Verlag GmbH, pp. 669–682.
7. Waser, R., Bruchhaus, R., and Menzel, S. (2012) in *Nanoelectronics and Information Technology*, 3rd edn (ed R. Waser),

Wiley-VCH Verlag GmbH, pp. 683–710.

8. Menzel, S., Dittmann, R., and Waser, R. to be published in Adv. Physics (2015).
9. Linn, E., Rosezin, R., Kügeler, C., and Waser, R. (2010) *Nat. Mater.*, **9** (5), 403–406.
10. Nardi, F., Balatti, S., Larentis, S., Gilmer, D.C., and Ielmini, D. (2013) *IEEE Trans. Electron Devices*, **60** (1), 70–77.
11. Lee, M.-J. *et al.* (2009) *Nano Lett.*, **9**, 1476–1481.
12. Yang, J.J. *et al.* (2009) *Nanotechnology*, **20** (21), 215201.
13. Muenstermann, R., Menke, T., Dittmann, R., and Waser, R. (2010) *Adv. Mater.*, **22** (43), 4819–4822.
14. Kim, K., Jeong, D.S., and Hwang, C.S. (2011) *Nanotechnology*, **22** (25), 254002.
15. Liu, Q. *et al.* (2012) *Adv. Mater.*, **24** (14), 1844–1849.
16. Maehne, H. *et al.* (2012) *Solid-State Electron.*, **72**, 73–77.
17. Yao, J., Zhong, L., Natelson, D., and Tour, J. (2012) *Sci. Rep.*, **2** (00242), 1–5.
18. Chen, J. *et al.* (2013) *Nano Lett.*, **13**, 3671–3677.
19. Celano, U., Chen, Y.Y., Wouters, D.J., Groeseneken, G., Jurczak, M., and Vandervorst, W. (2013) *Appl. Phys. Lett.*, **102** (12), 121602/1–121602/3.
20. Park, G.-S. *et al.* (2013) *Nat. Commun.*, **4**, 2382/1–2382/9.
21. Calka, P. *et al.* (2013) *Nanotechnology*, **24** (8), 85706/1–85706/9.
22. Hsu, C.-W. *et al.* (2013) Proceedings of the 2013 VLSI Symposium on Technology.
23. Chen, Y.Y. *et al.* (2013) Electron Devices Meeting (IEDM), 2013 IEEE International.
24. Ninomiya, T., Wei, Z., Muraoka, S., Yasuhara, R., Katayama, K., and Takagi, T. (2013) *IEEE Trans. Electron Devices*, **60**, 1384–1389.
25. Kamaladasa, R.J. *et al.* (2015) *Microsc. Microanal.*, **21**, 140–153.
26. Zhirnov, V.V. *et al.* (2010) *Proc. IEEE*, **98** (12), 2185–2200.
27. Yang, J.J., Strukov, D.B., and Stewart, D.R. (2013) *Nat. Nanotechnol.*, **8** (1), 13–24.
28. Jeong, D.S., Schroeder, H., and Waser, R. (2007) *Electrochem. Solid-State Lett.*, **10** (8), G51–G53.
29. Nardi, F., Balatti, S., Larentis, S., and Ielmini, D. (2011) 2011 IEEE International Electron Devices Meeting (IEDM 2011), pp. 31.1.1–31.1.4
30. Aoki, Y. *et al.* (2014) *Nat. Mater.*, **5**, 3473/1–3473/9.
31. Kamaladasa, R.J. *et al.* (2013) *J. Appl. Phys.*, **113** (23), 234510/1–234510/7.
32. Baek, I.G. *et al.* (2004) Internat. Electron Device Meeting IEDM Technical Digest, pp. 587–590.
33. Choi, B.J. *et al.* (2005) *J. Appl. Phys.*, **98** (3), −33715-1-10.
34. Russo, U., Ielmini, D., Cagli, C., and Lacaita, A.L. (2009) *IEEE Trans. Electron Devices*, **56** (2), 186–192.
35. Ielmini, D., Bruchhaus, R., and Waser, R. (2011) *Phase Transitions*, **84** (7), 570–602.
36. Baek, I.G. *et al.* (2005) IEEE International Electron Devices Meeting (IEDM) 2005, Technical Digest, pp. 769–772.
37. Hickmott, T.W. (1962) *J. Appl. Phys.*, **33**, 2669–2682.
38. Lampert, M.A. (1956) *Phys. Rev.*, **103** (6), 1648–1656.
39. Lampert, M.A. (1962) *Phys. Rev.*, **125** (1), 126–141.
40. Gibbons, J.F. and Beadle, W.E. (1964) *Solid-State Electron.*, **7** (11), 785–790.
41. Hiatt, W.R. and Hickmott, T.W. (1965) *Appl. Phys. Lett.*, **6**, 106–108.
42. Chopra, K.L. (1965) *J. Appl. Phys.*, **36**, 184–187.
43. Simmons, J.G. and Verderber, R.R. (1967) *Radio Electron. Eng.*, **34**, 81–89.
44. Argall, F. (1968) *Solid-State Electron.*, **11** (5), 535–541.
45. Hickmott, T.W. (1969) *J. Vac. Sci. Technol.*, **6** (5), 828–833.
46. Hovel, H.J. and Urgell, J.J. (1971) *J. Appl. Phys.*, **42**, 5076–5083.
47. Hirose, Y. and Hirose, H. (1976) *J. Appl. Phys.*, **47** (6), 2767–2772.
48. Kahng, D. and Sze, S.M. (1967) *Bell Syst. Tech. J.*, **46**, 1288–1295.
49. Dearnaley, G., Stoneham, A.M., and Morgan, D.V. (1970) *Rep. Prog. Phys.*, **33** (3), 1129–1191.

50. Oxley, D.P. (1977) *Electrocomponent Sci. Technol.*, **3** (4), 217–224.

51. Pagnia, H. and Sotnik, N. (1988) *Phys. Status Solidi A*, **108** (1), 11–65.

52. Asamitsu, A., Tomioka, Y., Kuwahara, H., and Tokura, Y. (1997) *Nature*, **388** (6637), 50–52.

53. Zhuang, W.W. *et al.* (2002) IEEE Internat. Electron Device Meeting, Technical Digest IEDM, p. 193.

54. Beck, A., Bednorz, J.G., Gerber, C., Rossel, C., and Widmer, D. (2000) *Appl. Phys. Lett.*, **77** (1), 139–141.

55. Kozicki, M.N., Yun, M., Hilt, L., and Singh, A. (1999) *Electrochem. Soc.* Proceedings of Solid-State Ionic Devices **99**, Seattle, WA, May 02-07, 1999.

56. Terabe, K., Hasegaw, T., Nakayama, T., and Aono, M. (2001) *Riken Rev.*, **37**, 7–8.

57. Terabe, K., Hasegawa, T., Nakayama, T., and Aono, M. (2005) *Nature*, **433** (6), 47–50.

58. Szot, K., Speier, W., Bihlmayer, G., and Waser, R. (2006) *Nat. Mater.*, **5** (4), 312–320.

59. Waser, R., Dittmann, R., Staikov, G., and Szot, K. (2009) *Adv. Mater.*, **21** (25-26), 2632–2663.

60. Waser, R. and Aono, M. (2007) *Nat. Mater.*, **6** (11), 833–840.

61. Janousch, M., Meijer, G.I., Staub, U., Delley, B., Karg, S.F., and Andreasson, B.P. (2007) *Adv. Mater.*, **19**, 2232–2235.

62. Wei, Z. *et al.* (2008) IEEE Internat. Electron Device Meeting (IEDM), Technical Digest.

63. Kwon, D.-H. *et al.* (2010) *Nat. Nanotechnol.*, **5** (2), 148–153.

64. Strukov, D.B., Snider, G.S., Stewart, D.R., and Williams, R.S. (2008) *Nature*, **453** (7191), 80–83.

65. Chua, L.O. (1971) *IEEE Trans. Circuit Theory*, **CT-18** (5), 507–519.

66. Liu, T.-Y. *et al.* (2013) Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC 2013).

67. Fackenthal, R. *et al.* (2014) 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC).

68. Esaki, L., Laibowitz, R.B., and Stiles, P.J. (1971) *IBM Tech. Discl. Bull.*, **13** (8), 2161.

69. Blom, P.W.M., Wolf, R.M., Cillessen, J.F.M., and Krijn, M.P.C.M. (1994) *Phys. Rev. Lett.*, **73** (15), 2107–2110.

70. Ovshinsky, S.R. (1966) Symmetrical current controlling device, US Patent 3271591.

71. Ovshinsky, S.R. (1968) *Phys. Rev. Lett.*, **21** (20), 1450–1453.

72. Lee, T. and Chen, Y. (2012) *MRS Bull.*, **37**, 144–149.

73. Potember, R.S., Poehler, T.O., and Cowan, D.O. (1979) *Appl. Phys. Lett.*, **34** (6), 405–407.

74. Kever, T., Boettger, U., Schindler, C., and Waser, R. (2007) *Appl. Phys. Lett.*, **91** (8), 083506-1–083506-3.

75. Bandyopadhyay, A. and Pal, A.J. (2004) *Appl. Phys. Lett.*, **84** (6), 999–1001.

76. Karthaeuser, S. *et al.* (2006) *J. Appl. Phys.*, **100** (9), 94504-1–94504-6.

77. Choi, B.J., Chen, A.B.K., Yang, X., and Chen, I. (2011) *Adv. Mater.*, **23** (33), 3847–3852.

78. Ziegler, M., Oberlaender, M., Schroeder, D., Krautschneider, W.H., and Kohlstedt, H. (2012) *Appl. Phys. Lett.*, **101**, 263504.

79. Riggert, C., Ziegler, M., Schroeder, D., Krautschneider, W.H., and Kohlstedt, H. (2014) *Semicond. Sci. Technol.*, **29**, 1040011.

80. Stoliar, P., Rozenberg, M., Janod, E., Corraze, B., Tranchant, J., and Cario, L. (2014) *Phys. Rev. B: Condens. Matter*, **90** (4), 45146/1(R).

81. Xue, K.H., de Araujo, C.A.P., Celinska, J., and McWilliams, C. (2011) *J. Appl. Phys.*, **109**, 091602. 21st International Symposium on Integrated Ferroelectrics and Functionalities, Colorado Springs, CO.

82. Govoreanu, B. *et al.* (2011) 2011 IEEE International Electron Devices Meeting – IEDM '11, IEDM Technical Digest.

83. Zhirnov, V.V., Meade, R., Cavin, R.K., and Sandhu, G. (2011) *Nanotechnology*, **22** (25), 254027/1–254027/21.

84. Liang, J., Yeh, S., Wong, S.S., and Wong, H.-S.P. (2012) 2012 4th IEEE International Memory Workshop (IMW), p. 4.

85. Chen, A. (2013) *IEEE Trans. Electron Devices*, **60** (4), 1318–1326.

86. Torrezan, A.C., Strachan, J.P., Medeiros-Ribeiro, G., and Williams, R.S. (2011) *Nanotechnology*, **22**, 485203/1–485203/7.
87. Strukov, D.B. and Williams, R.S. (2009) *Appl. Phys. A: Mater. Sci. Process.*, **94** (3), 515–519.
88. Menzel, S., Waters, M., Marchewka, A., Böttger, U., Dittmann, R., and Waser, R. (2011) *Adv. Funct. Mater.*, **21** (23), 4487–4492.
89. Schroeder, H., Zhirnov, V.V., Cavin, R.K., and Waser, R. (2010) *J. Appl. Phys.*, **107** (5), 054517/1–054517/8.
90. Lee, M.-J. *et al.* (2011) *Nat. Mater.*, **10** (8), 625–630.
91. Miao, F. *et al.* (2011) *Adv. Mater.*, **23**, 5633–5640.
92. Russo, U., Kamalanathan, D., Ielmini, D., Lacaita, A.L., and Kozicki, M.N. (2009) *IEEE Trans. Electron Devices*, **56** (5), 1040–1047.
93. Chien, W.-C. *et al.* (2011) 2011 IEEE International Electron Devices Meeting – IEDM '11.
94. Ohno, T., Hasegawa, T., Tsuruoka, T., Terabe, K., Gimzewski, J.K., and Aono, M. (2011) *Nat. Mater.*, **10**, 591–595.
95. Jo, S.H., Chang, T., Ebong, I., Bhadviya, B.B., Mazumder, P., and Lu, W. (2010) *Nano Lett.*, **10** (4), 1297–1301.
96. The International Technology Roadmap for Semiconductors (ITRS) (2013).
97. Chiu, P.-F. *et al.* (2012) *IEEE J. Solid-State Circuits*, **47** (6), 1483–1496.
98. Lee, H.Y. *et al.* (2008) IEEE International Electron Devices Meeting 2008, Technical Digest, San Francisco, CA.
99. Panasonic (2013) press release.
100. Liang, J. and Wong, H.-S.P. (2010) *IEEE Trans. Electron Devices*, **57** (10), 2531–2538.
101. Flocke, A., Noll, T.G., Kugeler, C., Nauenheim, C., and Waser, R. (2008) Proceedings of the 8th IEEE Conference on Nanotechnology, pp. 319–322.
102. Liang, J., Yeh, S., Wong, S.S., and Wong, H.-S.P. (2013) *ACM J. Emerging Technol. Comput. Syst.*, **9** (1), 9:1–9:14.
103. Deng, Y. *et al.* (2013) *IEEE Trans. Electron Devices*, **60** (2), 719–726.
104. Lee, M.-J. *et al.* (2007) 2007 IEEE International Electron Devices Meeting – IEDM '07, IEDM Technical Digest.
105. Kim, G. *et al.* (2013) *Adv. Funct. Mater.*, **23** (11), 1440–1449.
106. Huang, J.-J., Tseng, Y.-M., Hsu, C.-W., and Hou, T.-H. (2011) *IEEE Electron Device Lett.*, **99**, 1–3.
107. Lee, W. *et al.* (2012) 2012 IEEE Symposium on VLSI Technology, pp. 37–38.
108. Govoreanu, B., Adelmann, C., Redolfi, A., Zhang, L., Clima, S., and Jurczak, M. (2014) *IEEE Electron Device Lett.*, **35** (1), 63–65.
109. Lee, M.-J. *et al.* (2007) *Adv. Mater.*, **19**, 3919–3923.
110. Son, M. *et al.* (2011) *IEEE Electron Device Lett.*, **32** (11), 1579–1581.
111. Ko, C. and Ramanathan, S. (2008) *Appl. Phys. Lett.*, **93** (25), 252101.
112. Kim, S. *et al.* (2012) 2012 IEEE Symposium on VLSI Technology, pp. 155–156.
113. Yang, J.J. *et al.* (2012) *Appl. Phys. Lett.*, **100** (11), 113501/1.
114. Pickett, M.D., Borghetti, J., Yang, J.J., Medeiros-Ribeiro, G., and Williams, R.S. (2011) *Adv. Mater.*, **23** (15), 1730.
115. Cha, E., Woo, J., Lee, D., Lee, S., and Hwang, H. (2014) 2014 IEEE International Symposium on Circuits and Systems, ISCAS 2014, Melbourne, VIC, Australia.
116. Gopalakrishnan, K. *et al.* (2010) Symposium on VLSI Technology (VLSIT), Honolulu, HI.
117. Yang, J.J., Borghetti, J., Murphy, D., Stewart, D.R., and Williams, R.S. (2009) *Adv. Mater.*, **21** (37), 3754–3758.
118. Shima, H., Zhong, N., and Akinaga, H. (2009) *Appl. Phys. Lett.*, **94** (8), 082905-1–082905-3.
119. Huang, J.-J., Tseng, Y.-M., Luo, W.-C., Hsu, C.-W., and Hou, T.-H. (2011) 2011 IEEE International Electron Devices Meeting – IEDM '11.
120. Goda, A., Parat, K., and January, M.T. (2012) IEEE International Electron Devices Meeting, pp. 13–16.
121. Tanaka, H. *et al.* (2007) IEEE Symposium on VLSI Technology, pp. 14–15.
122. Kim, W. *et al.* (2009) IEEE Symposium on VLSI Technology, pp. 188–189.
123. Jang, J. *et al.* (2009) IEEE Symposium on VLSI Technology, pp. 192–193.

124. Lee, M.J. *et al.* (2009) *Adv. Funct. Mater.*, **19** (10), 1587–1593.

125. Yoon, H.S. *et al.* (2009) 2009 Symposium on VLSI Technology, Digest of Technical Papers.

126. Baek, I. *et al.* (2011) Technical Digest - International Electron Devices Meeting, IEDM.

127. Chien, W. *et al.* (2012) 2012 IEEE Symposium on VLSI Technology, pp. 153–154.

128. Chen, H.-Y., Yu, S., Gao, B., Huang, P., Kang, J., and Wong, H.-S.P. (2012) 2012 IEEE International Electron Devices Meeting (IEDM 2012), pp. 20.7. 1–20.7. 4.

129. Yu, S. *et al.* (2013) 2013 Symposium on VLSI Technology, pp. T158–T159.

130. Yu, S., Chen, H.-Y., Gao, B., Kang, J., and Wong, H.-S.P. (2013) *Acs Nano*, **7** (3), 2320–2325.

131. Akinaga, H. (2013) *Jpn. J. Appl. Phys.*, **52** , 100001-1–100001-12.

132. Yamamoto, S., Shuto, Y., and Sugahara, S. (2010) *Jpn. J. Appl. Phys.*, **49**, 040209-1–040209-3.

133. Kawahara, A. *et al.* (2012) International Solid-State Circuit Conference (ISSCC), pp. 220–221.

134. Harari, E. (2012) International Solid-State Circuit Conference (ISSCC), pp. 10–15.

135. Fukuda, M., Higuchi, K., and Takeuchi, K. (2011) *Jpn. J. Appl. Phys.*, **50**, 04DE09-1–04DE09-7.

136. Takeuchi, K., Hatanaka, T., and Tanakamaru, S. (2012) *IEICE Electron. Express*, **9** (8), 779–794.

137. Kaeriyama, S. *et al.* (2005) *IEEE J. Solid-State Circuits*, **40** (1), 168–176.

138. Strukov, D.B. and Likharev, K.K. (2005) *Nanotechnology*, **16** (6), 888–900.

139. Liauw, Y.Y., Zhang, Z., Kim, W., Gamal, A.E., and Wong, S.S. (2012) IEEE International Solid-State Circuits Conference, pp. 406–408.

140. Miyamura, M. *et al.* (2012) IEDM Technical Digest, p. 247.

141. Borghetti, J., Snider, G.S., Kuekes, P.J., Yang, J.J., Stewart, D.R., and Williams, R.S. (2010) *Nature*, **464** (7290), 873–876.

142. Linn, E., Rosezin, R., Tappertzhofen, S., Böttger, U., and Waser, R. (2012) *Nanotechnology*, **23**, 305205.

143. You, T. *et al.* (2014) *Adv. Funct. Mater.*, **24**, 3357–3365.

144. Siemon, A. *et al.* (2015) *Adv. Funct. Mater*. (DOI: 10.1002/adfm.201500865)

145. Nikonov, D.E. and Young, I.A. (2012) *Nanotechnology*, **23**, 305205.

146. Diorio, C.J., Hasler, P.E., Mead, C.A., and Minch, B.A. (1996) *IEEE Trans. Device Mater. Reliab.*, **43**, 1972.

147. Rajendran, B. *et al.* (2013) *IEEE Trans. Electron Devices*, **60**, 246.

148. Yu, S., Wu, Y., Jeyasingh, R., Kuzum, D., and Wong, H.P. (2011) *IEEE Trans. Electron Devices*, **58**, 2729–2737.

149. Nielen, L., Siemon, A., Tappertzhofen, S., Waser, R., Menzel, S., and Linn, E. (2015) IEEE Journal on Emerging and Selected Topics in Circuits and Systems, pp. 1–9.

150. Prezioso, M., Merrikh-Bayat, F., Hoskins, B.D., Adam, G.C., Likharev, K.K., and Strukov, D.B. (2015) *Nature*, **521** (7550), 61–64.