1
3D IC Integration Since 2008

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In Volume 1, we covered some of the history of the development of the 3D integrated circuit (3D IC) concept and we direct you to that chapter for such content [1].

Since the first two volumes of the *Handbook of 3D Integration* appeared in 2008, significant progress has been made to bring 3D IC technology to commercialization. This chapter will attempt to summarize some of the key developments during that period.

We previously described 3D IC integration as "an emerging, system level integration architecture wherein multiple strata (layers) of planar devices are stacked and interconnected using through-silicon (or other semiconductor material) vias (TSV) in the *Z* direction" as depicted schematically in Figure 1.1a and in cross section in Figure 1.1b [1].

With the continued pressure to miniaturize portable products and the near universal agreement that scaling as we have known it is soon coming to an end [2], a perfect storm has been created. The response to this dilemma at both the device and the package level has been to move into the third dimension.

It is commonly accepted that chip stacks wire-bonded down to a common laminate base and stacked packages such as package-on-package (PoP) are categorized as "3D packaging." Transistor design has also gone vertical [3] as Intel [4] and others move to "finfet" stacked transistor structures at the 22 nm generation. These are compared pictorially in Figure 1.2.

In Figure 1.3, we compare system-on-chip (SoC), 3D packaging, and 3D IC with through-silicon via (TSV) in various performance categories [5].

1.1
3D IC Nomenclature

Since 2008 there have been attempts to further refine the nomenclature for 3D IC integration, although it has not yet been universally adopted in publications. In 2009 the International Technology Roadmap for Semiconductors (ITRS)

Handbook of 3D Integration: 3D Process Technology, First Edition.
Edited by Philip Garrou, Mitsumasa Koyanagi, and Peter Ramm.

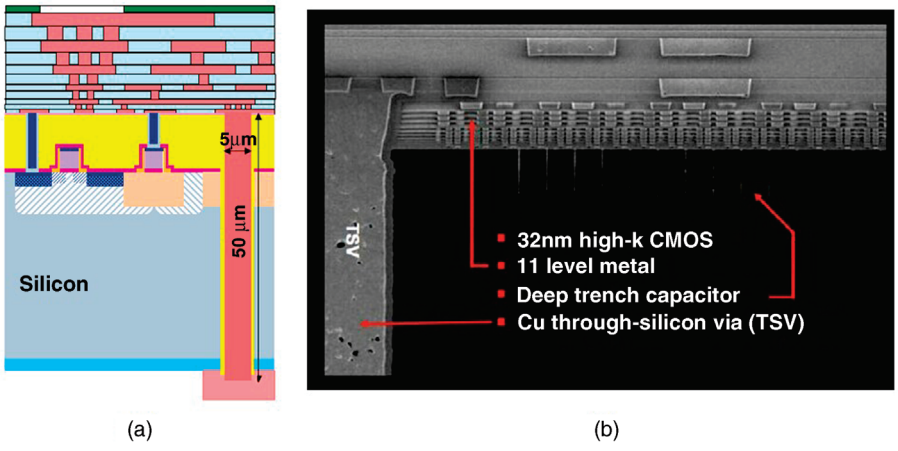


Figure 1.1 3D IC with TSV: (a) schematic (courtesy of IMEC) and (b) cross section (courtesy of IBM). Note that the IBM cross section is connected at a higher (fatter) on chip interconnect level.

proposed the following nomenclature in an attempt to define the possible different levels of connections possible as circuits are deconstructed onto separate strata (see Table 1.1) [6].

1.2 Process Standardization

3D IC requires three new pieces of technology: (1) insulated conductive vias through a thinned silicon substrate (i.e., TSV); (2) thinning and handling technology for wafers as thin as 50 µm or less; (3) technology to assemble and package such thinned chips.

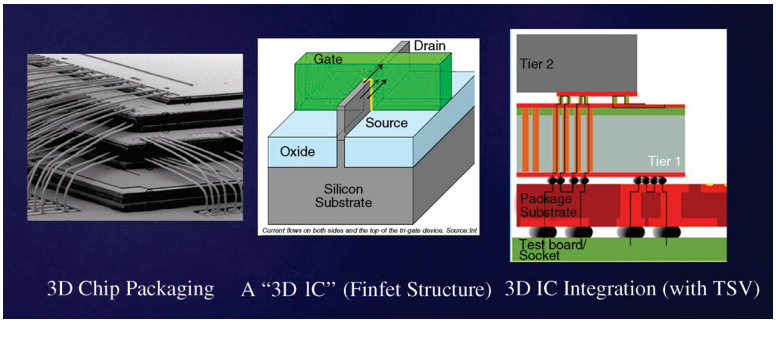


Figure 1.2 3D packaging, 3D finfet transistors, and 3D IC integration.

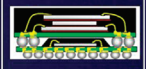
	On-chip SoC	PoP	WB stack	TSV stack
				
Memory capacity	-	++	++	++
Memory bandwidth	++	0	+	+++
Power consumption	++	0	+	+++
Form factor	0	+	++	+++
Cost	---	-	++	??

Figure 1.3 Comparison of SoC, 3D packaging, and 3D IC [5].

Table 1.1 2009 ITRS roadmap [6].

Level	Suggested name	Supply chain	Key characteristics
Package	3D packaging (3D-P)	OSAT assembly printed circuit board (PCB)	• Traditional packaging of interconnect technologies, for example, wire-bonded die stacks, package-on-package stacks • Also includes die in PCB integration • No through-Si vias
Bond-pad	3D wafer-level package (3D-WLP)	Wafer-level packaging	• WLP infrastructure, such as RDL and bumping • 3D interconnects are processed after the IC fabrication, "post IC passivation" (via-last process). Connections on bond-pad level • TSV density requirements follow bond-pad density roadmaps
Global	3D stacked integrated circuit/3D system-on-chip (3D-SIC/3D-SoC)	Wafer fab	• Stacking of large circuit blocks (tiles, IP blocks, memory banks), similar to an SoC approach but having circuits physically on different layers • Unbuffered I/O drivers (low C, little or no ISD protection on TSVs) • TSV density requirement significantly higher than 3D-WLP: Pitch requirement down to 4–16 μm

(*continued*)

Table 1.1 (*Continued*)

Level	Suggested name	Supply chain	Key characteristics
Intermediate	3D-SIC	Wafer fab	• Stacking of smaller circuit blocks, parts of IP blocks stacked in vertical dimensions • Mainly wafer-to-wafer stacking • TSV density requirements very high: Pitch requirement down to 1–4 μm
Local	3D IC	Wafer fab	• Sticking of transistor layers • Common back-end-of-line (BEOL) interconnect stack on multiple layers of front-end-of-line (FEOL) • Requires 3D connections at the density level of local interconnects

In the mid-2000s, practitioners were bewildered by the multitude of proposed technical routes to 3D IC. It has become clear, since then, that for most applications, the preferred process flow is what has been called a "via-middle" approach, where the TSVs are inserted after front-end transistor formation and early on during the on-chip interconnect process flow. This requires that TSVs are manufactured in back end of fab, not during or after the assembly process. This requires that TSV fabrication will be done by vertically integrated IDMs or foundries. TSV technology appears to be stabilized as depicted in Figure 1.4 and Table 1.2.

1.3 The Introduction of Interposers (2.5D)

Many believe the introduction of interposers (also known as 2.5D) was due to the failure of 3D IC, but this is not the case. Interposers were and are needed due to the lack of chip interface standardization and the need for a better thermal solution than is currently available for some 3D stacking situations.

The term "2.5D" is usually credited to Ho Ming Tong from Advanced Semiconductor Engineering (ASE), who in 2009 (or even earlier) declared that we might need an intermediate step toward 3D since the infrastructure and standards were not ready yet. The silicon interposer, Tong felt, would get us a major part of the way there, and could be ready sooner than 3D technology, thus the term "2.5D," which immediately caught on with other practitioners [7].

2.5D interposers resemble silicon multichip module technology of the 1990s, with the addition of TSV [8]. In today's applications, they provide high-density redistribution layers (RDLs), so the chips can be connected either through the interposer or next to each other on the top surface of the interposer as shown in

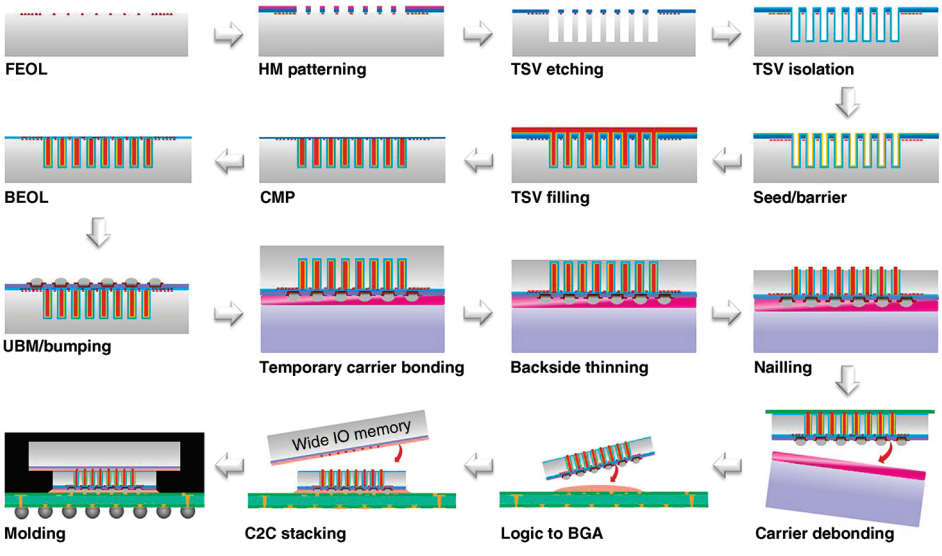


Figure 1.4 Standard 3D IC process flow. Courtesy of Yole Developpement.

Figure 1.5. The latter is the superior thermal solution since all chips can be attached to a heat sink for cooling.

Interposers will add cost and probably will not be a broadly accepted solution for low-cost mobile products, which would prefer straight 3D stacking [9].

Table 1.2 Standard 3D IC process flow options.

Process	Preferred option	Alternative options available			
TSV formation	Bosch deep reactive ion etching (DRIE)	Laser			
TSV Insulation	SiO_2	Polymer			
Conductor	Cu	W	pSi		
Process flow	Via-middle	Via-last (backside)[a)]	Via-first (for pSi)	Via-last (front side)	
Stacking Bonding	IMC	Cu–Cu	Oxide bonding	Polymer bonding	Hybrid bonding (oxide–metal or polymer–metal)
Thin wafer handling	On carrier	On stack			

a) Preferred flow for CMOS image sensors.

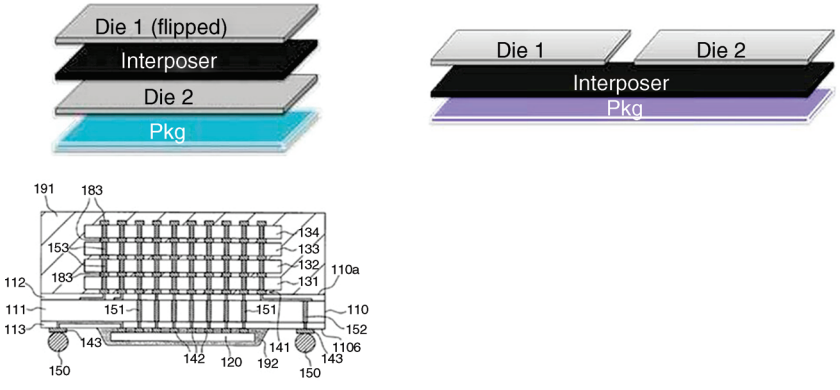


Figure 1.5 Interposer configurations.

1.4 The Foundries

1.4.1 TSMC

In October 2012, TSMC announced the readiness of their 2.5D CoWoS™ (chip-on-wafer-on-substrate) technology within their "Open Innovation Platform®" and made public their reference flows supporting CoWoS. Several EDA companies including Cadence, Mentor, Synopsys, and Ansys were announced as partners in the CoWoS reference flow [10]. Their first public CoWoS demonstrator vehicle (Figure 1.6) included logic and DRAM in a single module using the wide I/O interface [11].

Early TSMC customers reportedly included Xilinx, AMD, Nvidia, Qualcomm, Texas Instruments, Marvell, and Altera [12], with Xilinx being the first to production in late 2011.

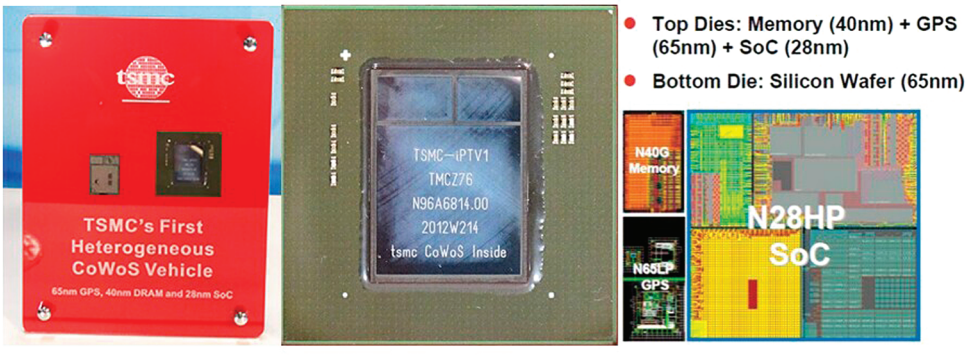


Figure 1.6 2.5D TSMC demonstrator vehicle [11].

Reportedly due to ". . . the numerous technical challenges that make the conventional collaboration infrastructure more difficult" for 2.5 and 3D IC, TSMC has taken the position of being responsible for the full process (chip design and fabrication through module test).

1.4.2 UMC

UMC announced in the spring of 2011 that it had acquired production equipment for TSV and other 3D IC technologies. In 2013 UMC and STATS ChipPAC announced a jointly developed TSV-enabled 3D IC chip stack consisting of a Wide I/O memory test chip stacked upon a TSV-embedded 28 nm processor test chip [13].

1.4.3 GlobalFoundries

GlobalFoundries (GF) announced installation of TSV production tools for 20 nm technology wafers in their Fab 8 New York facility. The first full-flow silicon with TSVs was expected to start running in the third quarter of 2012 [14].

In contrast to TSMC, which announced a one-stop-shop turnkey line that included all of the assembly and test steps traditionally handled by outsourced semiconductor assembly and test (OSAT) facilities, UMC and GlobalFoundries indicated a preference to work under the open ecosystem model where they would handle TSV fabrication (Cu, via-middle) and other front-end steps while chips from various vendors would be back-end processed (i.e., temporary bonding/debonding, thinning, assembly, and test by their OSAT partners).

1.5 Memory

DRAM performance is constrained by the capacity of the data channel that sits between the memory and the processor. No matter how much faster the DRAM chip itself gets, the channel typically chokes due to the lack of transfer capacity; that is, they require more bandwidth. Wide I/O memory has been developed as the solution to this bandwidth problem [15].

Also, as more and more memory is required for a given application, power consumption also becomes important to both portable products and server farms, which need special cooling to keep them from overheating. Samsung reports that TSV-based RDIMM shows a 32% decrease in power consumption versus LRDIMM at 1333 Mbps [16].

1.5.1 Samsung

In late 2010, Samsung, who first revealed 3D TSV stacked memory prototypes in 2006, announced 40 nm, 8 GB RDIMM based on 4 Gb, 1.5 V, 40 nm DDR3

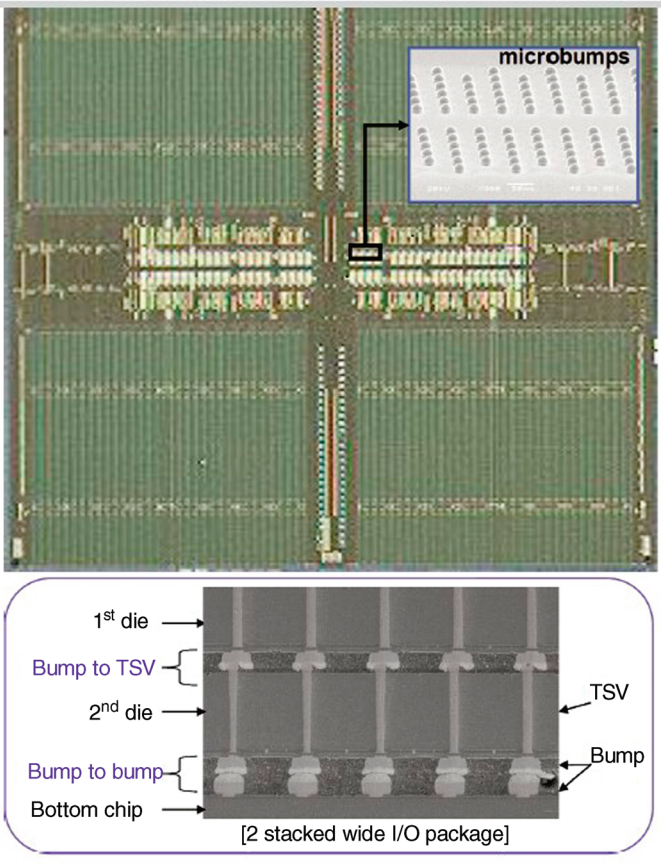


Figure 1.7 1.2 V 12.8 GB s^{-1} 2 Gb mobile wide I/O DRAM with 4 × 128 I/Os using TSV-based stacking [18].

memory chips operating at 1333 MHz and 3D TSV chip-stacking technology [17]. In 2011, they announced the development of wide I/O 1 Gb DRAM (Figure 1.7) [18]. Samsung has not announced any commercial memory products as of late 2013. Samsung is a member of the Micron hybrid memory cube consortium.

1.5.2 Micron

Micron developed a "hybrid memory cube" (HMC), which is a stack of multiple thinned memory dies sitting atop a logic chip bonded together using TSV (Figure 1.8). This greatly increases available DRAM bandwidth by leveraging the large number of I/O pins available through TSVs. The controller layer in the HMC allows a higher speed bus from the controller chip to the CPU and the thinned and TSV connected memory layers mean memory can be packed more densely in a given volume. The HMC requires about 10% of the volume of a DDR3 memory

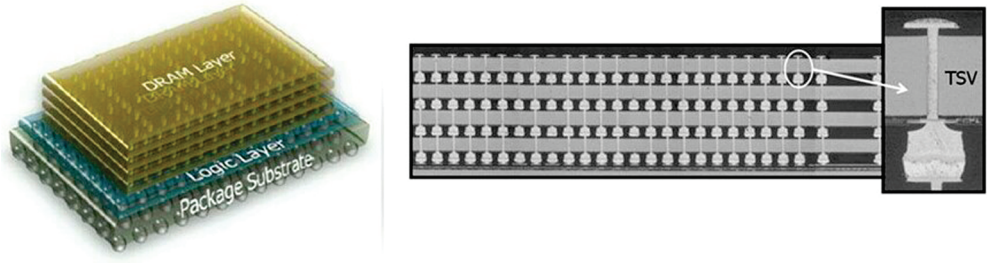


Figure 1.8 Micron hybrid memory cube (HMC) [19].

module. It is claimed that the technology provides 15× the performance of a DDR3 module, uses 70% less energy per bit than DDR3, and occupies 90% less space than today's RDIMMs. Micron has announced that they will be manufacturing the memory layers and have contracted IBM to manufacture the logic layer. Commercialization is scheduled for 2013–2014.

HMC electrical performance is compared to other DRAM modules in Table 1.3.

1.5.3 Hynix

Hynix reported that they expect "2 and 4 chip memory stacks with TSV to be in commercial production in 2014 and graphics solutions on interposers soon thereafter" [21].

1.6 The Assembly and Test Houses

Amkor was involved with commercial 3D IC assembly as part of their TSMC Xilinx program [22]. ASE, SPIL, and Powertech are all boosting 3D IC package and test capacity. SPIL (Siliconware) announced the instillation of dual damascene processing for high density interposers in 2013 [23]. Powertech, which has been in a 3D IC joint development program with Elpida (now Micron) and UMC for several years, announced volume production of 3D IC packaging and test capability in 2013.

Table 1.3 Comparison of Micron HMC to DDR memories [20].

Technology	VDD	BW (Gb s^{-1})	Power (W)
SDRAM PC133 1 Gb module	3.3	1.06	4.96
DDR-333 1 Gb module	2.5	2.66	5.48
DDR2-667 2 Gb module	1.8	5.34	5.18
DDR3-1333 2 Gb module	1.5	10.66	5.52
DDR4-2667 4 Gb module	1.2	21.34	6.60
HMC Gen 1 512 Mb cube	1.2	128.0	10.73

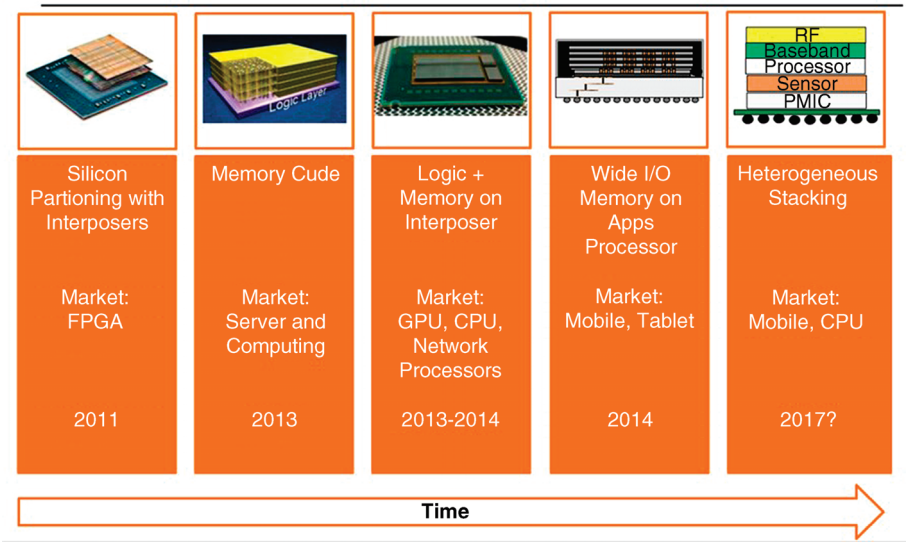
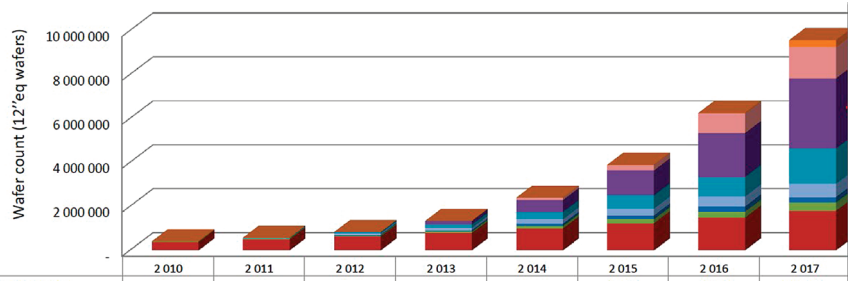


Figure 1.9 3D IC application timing. Courtesy of GlobalFoundries 2012.

1.7 3D IC Application Roadmaps

The first commercial application has been field-programmable gate arrays (FPGAs) with Xilinx (commercial) [22] and Altera (developing) [24] interposer-based solutions with TSMC.

Looking at the roadmap of GlobalFoundries in Figure 1.9, we see that 2.5D graphics processor modules and 3D application processors with baseband and/or memory should be coming soon.



	2 010	2 011	2 012	2 013	2 014	2 015	2 016	2 017
3D Stacked NAND Flash	-	-	-	-	-	8 877	20 130	318 072
3D Wide IO Memory	-	-	-	-	110 215	252 005	896 565	1 429 417
Logic 3D SiP / SoC	-	-	9 734	169 677	544 957	1 137 164	2 000 097	3 190 499
3D Stacked DRAM	-	7 977	50 563	146 200	324 563	593 361	878 729	1 596 526
MEMS / Sensors	92	29 396	76 298	116 305	208 910	323 314	461 323	616 799
LED	4 395	8 759	18 890	45 188	91 101	159 569	232 887	237 715
RF, Power, Analog & Mixed Signal	26 255	35 892	47 018	80 883	127 106	189 921	275 402	386 344
Imaging & Optoelectronics	387 126	503 821	635 468	787 345	996 423	1 240 691	1 492 479	1 801 534
TOTAL	417 868	585 845	837 971	1 345 597	2 403 275	3 904 902	6 257 613	9 576 906

Figure 1.10 TSV chip wafer forecast 2010–2017. Courtesy of Yole Developpement.

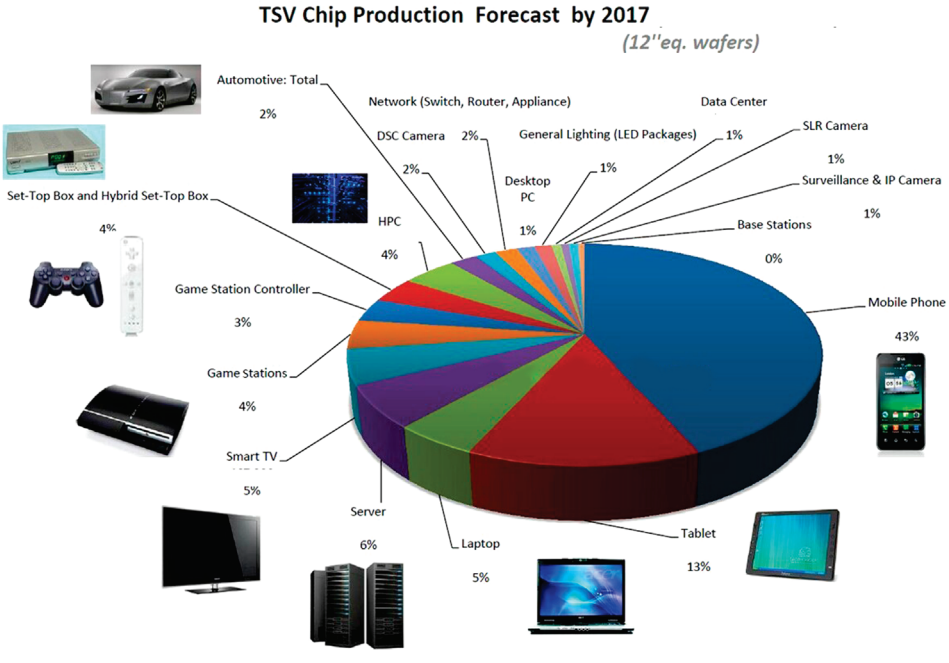


Figure 1.11 Global TSV chip end applications in 2017. Courtesy of Yole Developpement.

The latest projections by Yole Developpement are shown in Figures 1.10 and 1.11. 3D IC volume is expected to increase to nearly 10 MM wafers over the next 4 years with major increases in stacked memory, wide I/O DRAM, and logic plus memory system-in-packages (SiPs).

Examining 2.5/3D device product insertion, we see that most of these devices will eventually be incorporated in the smartphone and tablet markets.

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