

## Index

### a

- accumulation mode (AM) 104, 105
- advanced nanoelectronics
  - electronic confinement 55
  - 1D material properties 55
  - 2D geometry 55
- AlGaIn/GaN 2DEGs 242
- ambipolar property, of graphene 57–58
- arithmetic logic unit (ALU) 85, 86
- armchair nanotubes 122
- ATLAS-TFET 164, 165
- atomic layer deposition (ALD) 9, 98–101, 111, 124, 126, 142, 193
- axial and radial heterostructures 44, 45
- axial and radial junctions 44

### b

- Bayesian inference engines 204, 231
- binary phase-shift keying 72–73
- biochemical sensing 241
- biosensors
  - applications of 167
  - FET based 166, 168
  - sensitivity of 166, 170
  - TFET based 169
- bistable nanomagnet, writing bit information in
  - spin transfer torque 216–217
  - straintronics 224–231
  - voltage controlled magnetic anisotropy 220–224
- bit-cost scalable (BiCS) technology 12
- Blue Brain Project 19
- Boltzmann distribution 152, 165, 180

- Boltzmann tyranny effect 171, 174
- bulk semiconductors 56

### c

- capacitance, defined 182
- capacitor, defined 182
- carbon nanotubes (CNTs)
  - back-gated transistor 124
  - CMOS ROs 142
  - fundamentals of 122
  - solution processed 122
- central processing unit (CPU) 18, 19, 85
- charge-based devices
  - vs. spin-based devices 203–205
- charge neutrality level (CNL) 57, 92–93, 105
- chemical mechanical polishing (CMP) 9, 102
- chemical vapor deposition (CVD) 5, 61, 74, 76, 78, 102, 123, 129, 133, 138, 139
- chip-on-chip (CoC) bonding 10
- chip-on-wafer (CoW) bonding 10
- CNT field-effect transistors (CNTFET)
  - channel length scaling, in 127–131
  - circuit-level integration 142
  - contact engineering for CMOS logic 124–127
  - contact length scaling 132–138
  - sub-10 nm technology nodes 139
  - variability 140–142
  - with various gate structures 124, 125

- coefficient of thermal expansion (CTE)
    - 13
  - column chromatography 140, 141
  - complementary
    - metal-oxide-semiconductor (CMOS) technology 1, 180
  - conductive-bridging RAM (CBRAM) 15–17
  - conventional FETs (CFETs)
    - fundamental limitation in 151–153
    - vs. TFET based biosensors 170
  - core-shell-multigate geometry 43
  - cosine curve wavefunction 39
  - Cu metal-to-metal thermocompression bonding 10
  - current saturation 62–63, 65, 67, 79
  - CVD-grown CNT *vs.*
    - solution-processed CNT 138–139
- d**
- Dark silicon 180
  - Dennard scaling rules 33, 34
  - device optimization
    - current saturation 62–63
    - metal contact 63–64
    - mobility engineering 61–62
  - die stacking 8, 11, 12
  - digital switches 14, 204
  - dipole-coupled NAND gate 227
  - direct-coupled FET logic circuit 78–79
  - direct-coupled transistor logic (DCTL)
    - configuration 79
  - D-mode device 79
  - double-gate FETs (DGFET) 3
  - drain depletion pitch-off 63
  - drain-induced-barrier-lowering (DIBL) 2, 4, 8, 33, 34, 48, 120, 121, 194
  - Drude-model 246
- e**
- earth oxides into Germanium MOSFETs
    - lanthanum-based oxide, Ge 101
    - yttrium-based oxide, Ge 101
  - effective oxide thickness 35
  - electrografting 10
  - electron cyclotron resonance (ECR) 100
  - electronic properties of CNT 122, 123, 142
  - electron mass show quantization effects 39
  - electron probability density 40, 41
  - electron spin resonance (ESR) toolbox 21, 22
  - electron wavefunction 39, 93, 242
  - electrostatic field effect 37
  - E-mode device 79
  - enzyme-linked immunosorbent assay (ELISA) 166
  - equivalent oxide thickness (EOT) 4, 46–48, 92, 98–101
- f**
- Fermi level pinning (FLP) 77, 92–94, 102, 111
  - Fermi-tail cutting 171
  - ferroelectric (FE) material 109
    - charge-voltage characteristics 183
    - energy landscape of 184
    - Landau–Devonshire theory 185
    - negative capacitance 184, 186–188
  - field-effect transistor (FET) 36, 56, 102, 168, 240
  - filamentary RRAM (F-RRAM) 15, 17–18
  - fin effect 7
  - fin field-effect transistors (FinFET)
    - challenges and limitations 7–8
    - high mobility material channel 4–5
    - industrial state 6–7
    - Si channel 3–4
    - SOI *vs.* Bulk 5–6
    - TMD channel 5
    - type transistor, energy dissipation in 203
    - and UTB devices 35–37
  - flip-flop memory cell 82
  - fluxonium 21
  - Friis formula 238
  - fully-depleted ultra-thin body (FD-UTB) 103

**g**

- GaAs-based QCLs 254
- gallium nitride (GaN)
  - characteristics 242
  - drift velocity 245–246
  - high-electron-mobility-transistors (HEMTs) 249–252
    - calculated performance 252
    - device operation 249
    - electron–optical-phonon interaction 243
    - E-mode 250
    - injection velocity 244
    - two dimensional electron gas 246
  - mobility and injection velocity 242–245
  - negative differential resistance 245–246
  - transport properties 242
  - velocity field characteristics 245
- GaN-based terahertz devices
  - electron plasma wave based devices 254–256
  - high-electron mobility transistors 249–252
  - NDR and resonant tunneling devices 253
  - quantum-cascade lasers 254
- gate dielectric deposition 45
- gated semiconductor heterostructures, electron plasma waves in 246
- gate metallization 110
- gate-to-drain capacitance 63
- gating effect 166, 168, 171, 174
- GeO<sub>2</sub>-based gate stacks
  - HPO 100
  - PPO/OPO 100
- germanium complementary metal-oxide-semiconductor (Ge CMOS) 102
  - circuits 105–107
  - devices 102–105
- germanium MOS devices
  - Ge MOSFET, stack combination
    - GeO<sub>x</sub>-free gate stack, ALD high-κ 98
    - germanium (oxy)nitridation 99
    - silicon interfacial layer passivation 99
  - process integration
    - interface engineering issues 97
    - various gate stack combinations 97–101
- germanium nanowire CMOS devices 104
- germanium-on-insulator (GeOI) 101, 102
- germanium sub-oxides (GeO<sub>x</sub>) 98–100, 111
- germanium transistors 92, 100, 102
- giant spin Hall effect-assisted STT 217–219
- glycoprotein detector 241
- graphene ambipolar devices
  - binary phase-shift keying 72–73
  - graphene frequency mixers 70–71
  - graphene frequency multipliers 68–70
- graphene-based integrated circuits
  - graphene ambipolar devices
    - binary phase-shift keying 72–73
  - graphene frequency mixers 70–71
  - graphene frequency multipliers 68–70
- graphene electromechanical devices
  - 74–76
  - graphene oscillators 73
  - graphene RF receiver 73–74
- graphene electromechanical devices
  - 74–76
- graphene electromechanical switches 75
- graphene electronics, radio-frequency applications
  - GFET 64
  - graphene RF transistor 65–67
  - graphene transistors 65
- graphene field effect transistors (GFET) 57, 58, 60, 62–68, 70–74, 76
- graphene nanoribbons 63
- graphene oscillators 73

graphene RF receiver 73–74  
 graphene RF transistor 65–67  
 graphene transistors 65, 66  
 grating gate HEMT structure 255  
 grown-and-transferred method, for  
 CNT 138

**h**

HfO<sub>2</sub> based ferroelectrics, negative  
 capacitance phenomena 187  
 high bandwidth memory (HBM) 12  
 high-electron-mobility-transistors  
 (HEMTs) 65, 66, 240, 241,  
 243, 244, 246–250, 252,  
 254–256  
 high pressure oxidation (HPO) 100  
 horizontal nanowires 45, 46  
 Human Brain Project (HBP) 18  
 hybrid memory cube (HMC) 12  
 hybrid qubits 21

**i**

image processing functions,  
 nanomagnets 231  
 important figures of merit (FOM)  
 57–61  
 cutoff frequency, oscillation 59–60  
 $I_{\text{on}}/I_{\text{off}}$  ratio 58–59  
 maximum frequency, oscillation  
 59–60  
 minimum noise figure 60–61  
 subthreshold swing 59  
 in-plane magnetic anisotropy 220,  
 222  
 Intel<sup>®</sup> Core<sup>™</sup> i7-6700K processor 201  
 Internet of Things 107, 179  
 intraband transitions, in terahertz  
 devices 239  
 inverse magnetostriction effect 224  
 inversion mode (IM) 104, 105

**j**

junction formation, Ge MOS devices  
 CNL 92–93  
 metal/Ge contacts  
 FLP, alleviation of 93

metal/n-Ge contact 93–94  
 recessed contact formation 94–97  
 junctionless nanowire transistor 47

**l**

Landau–Devonshire theory 185  
 Landau theory of ferroelectricity 185  
 Larmor relation 207  
 logic gates 59, 62, 79–82, 85, 142,  
 211–213, 228  
 longitudinal-optical (LO) phonon  
 frequencies 239  
 long-term depression (LTD) 14, 15, 16  
 long-term potentiation (LTP) 14–16  
 low temperature oxygen annealing  
 (LOA) 100

**m**

magneto-tunneling junction (MTJ)  
 215, 216, 218–231  
 based straintronic NAND gate 227  
 maximum available gain (MAG) 59  
 maximum stable gain (MSG) 59  
 metal contact 63–64, 76, 79, 124,  
 126–128, 132–134, 136, 142, 162,  
 193  
 metal/Ge contacts  
 FLP, alleviation of 93  
 metal/n-Ge contact 93–94  
 recessed contact formation 94–97  
 metallic carbon nanotubes 122  
 metal-oxide-semiconductor  
 field-effect-transistor (MOSFET)  
 56  
 drain-induced barrier lowering effects  
 120, 121  
 physics 181  
 resistance and capacitance  
 components, in Si 119, 120  
 schematic and equivalent circuit  
 diagram 181  
 short-channel effects 120, 121  
 metal-semiconductor (MS) 43, 92  
 metamaterials 241  
 microfluids/gases, real time monitoring  
 of 241

- microprocessor architecture 86
  - minimum noise figure 60–61, 67
  - MIT Virtual Source (MVS) compact device model 189
  - mobility degradation 8, 40, 62, 97
  - mobility engineering 61–62
  - modified chemical vapor deposition (mCVD) 78
  - modular NCFET 191, 192
  - monolayer graphene resonators 75
  - monolithic approach 8, 12
  - monolithic integrated microwave integrated circuit (MMIC) 240, 249
  - Moore's law 1, 56, 91, 97, 107, 119, 120, 123, 180, 202, 203
  - More than Moore (MtM) 1, 91
  - MoS<sub>2</sub> devices, digital application
    - based integrated circuits
      - direct-coupled FET logic circuit 78–79
      - logic gates 79–82
      - microprocessor 85–86
      - ring oscillator 82–85
      - SRAM cell 82
    - TMDC 76
    - transistor 77–78
  - multi-level resistance modulation 18
  - multiple-gate FETs (MuGFETs) 2
  - multistage logic circuits 81
- n**
- NAND gate configuration 211, 212
  - nanomagnetic devices
    - reading stored bit information 215–216
    - single-domain 212
    - writing bit information 216–231
  - nanomagnetic NAND gate 213, 214
  - nanomechanical resonator 75
  - nanometer geometries 45
  - nanowire devices
    - III-V devices 46–49
    - silicon devices 45–46
  - nanowire growth
    - bottom up VLS growth
      - compound semiconductors 44
      - fabrication steps 44
      - fabrication techniques 43
      - liquid metal alloy seed 43
      - top-down oxidation 45
  - nanowires, limit of electrostatic control 37–38
  - negative capacitance field-effect transistors (NCFETs) 109, 180
    - device structure 180
    - different structures of 190
    - equivalent capacitive circuit model 189
    - experimental demonstration 190–195
    - modeling and simulation 188–190
    - negative output differential resistance 189
    - operation 181
    - properties 188–190
    - sub-60 mV/decade switching
      - characteristics 181–182
      - switching speed 195
  - negative capacitance FinFETs (NC-FinFETs) 192–195
  - negative capacitance, in ferroelectric capacitor
    - direct measurement 186–188
    - energy landscape description 186–188
  - negative capacitor
    - charge-voltage characteristics 183
    - ferroelectric materials as 182–185
  - negative differential resistance (NDR) effect, GaN 245–246
  - neuromorphic computing technology 2, 13
    - state-of-the-art nonvolatile memory
      - CBRAM 16–17
      - PCM 15–16
  - 9-stage Ge CMOS ring oscillator 105, 108
  - non-Boolean straintronic architectures 228–231
  - non-equilibrium Green's function (NEGF) formalism 156

- non-toggle memory 217, 225–226
- non-volatile logic 204
- non-volatile memory (NVM) 14, 15, 223
- non-von Neumann (VN) computing 1
- O**
- optical phonon energies, of
  - semiconductor materials 239
- oxidized at atmospheric pressure (APO) 100
- ozone post oxidation (OPO) 98, 100
- P**
- package-on-package (POP) 8
- parasitic delay 251
- passive-first active-last fabrication flow 74
- perpendicular magnetic anisotropy (PMA) 220–223
- phase change memory (PCM) 15, 16
- planar devices, scaling of
  - drive current 43
  - FinFET and UTB devices 35–37
  - nanowires, limit of electrostatic control 37–38
  - quantum effects 39–43
- planar processing 45
- plasma post oxidation (PPO) 98, 100
- polarization-electric field (P-E) loop 111
- polycrystalline graphene films 76
- positive capacitance, charge-voltage characteristics 183
- P-type Ge NCFETs 193
- purified-and-placed method, for CNT 138, 139
- Q**
- quantization effects 39, 43
- quantronium 21
- quantum-cascade lasers (QCLs) 239, 240, 249, 253, 254
- quantum computing 2
  - challenges and limitations 23
  - industry state 22–23
  - quantum bit requirement 20
  - spin-based qubits 20–21
  - superconducting circuits, quantum information 21–22
- quantum conductance 42
- quantum effects
  - electron probability density 39
  - electron wavefunction 39
  - quantum confinement effects 39
- quantum error correction algorithm 23
- R**
- radio-frequency (RF) 20, 23, 48, 58, 64–76, 238
- rapid thermal annealing (RTA) 111, 193
- recessed contact formation 94–97
- remnant polarization ( $P_r$ ) 111, 188, 193
- resistive computing 1
- resistive-RAM (RRAM) 15, 17–18
- resonant frequency 75, 241
- resonant tunneling diode (RTD)
  - based devices 240
  - gated plasma wave HEMTs 256
  - oscillators 253
- resonant tunneling, in GaN
  - heterostructures 253
- Reststrahlen bands 239, 248
- RF electronics 62, 68, 73
- S**
- scanning electron microscopic (SEM) 44, 45, 47, 74, 75, 94, 103, 104, 108, 129, 131, 134–137, 141
- Schottky barrier 63, 64, 77, 78, 92, 94, 124, 126, 156
- Schottky barrier heights (SBHs) 92
- Schrodinger's equation 39
- self-aligned quad patterning (SAQP) 7
- self-assembled monolayer (SAM) 11, 140
- semiconducting carbon nanotubes 122
- short-channel effects 33–35, 37, 120, 121

- SiGe-based semiconductors 65
  - silicon devices 21, 45–46
  - silicon interfacial layer passivation 99
  - silicon-on-insulator (SOI) 3, 35, 102, 119, 180
  - silicon two-qubit logic device 22
  - Si MOSFET, resistance and capacitance components 119, 120
  - single-domain nanomagnet
    - description 212
    - features 213
    - magnetization state 213
    - vs. single spins 214
  - single layer graphene (SLG) 93
  - single spin logic (SSL)
    - devices and circuits 209–212
    - operating temperature 211
  - SmartCut™ 102
  - smooth sidewalls 45
  - solid state terahertz sources, classes of 240
  - solution-processed CNT
    - vs. CVD-grown CNT 138–139
    - purity and placement of 140
  - source-to-drain current 57, 59, 208, 209
  - sp<sup>2</sup> carbon allotropes 122, 123
  - spike-timing-dependent-plasticity (STDP) 14–17
  - spin-based devices
    - vs. charge-based devices 204, 205
    - non-volatility 204
    - single spin logic devices and circuits 209–212
    - SPINFET 205–209
  - spin-based switches 204
  - spin field effect transistor (SPINFET) 205–209, 212, 232
  - spin Hall angle 218
  - spin-orbit coupling 20
  - spin transfer torque (STT)
    - advantages 217
    - defined 216
    - giant spin Hall effect 217–219
    - writing error 217
  - state-of-the-art technology 8, 65
  - static random-access memory (SRAM) 4, 18, 82
  - steep slope device 107–111
  - steep transistors 153, 169
  - stochastic Landau-Lifshitz-Gilbert simulation 226
  - straintronics
    - elliptical magnetostrictive nanomagnet, switching of 224
    - energy dissipation sources during write operation 226
    - logic 226–228
    - NAND gate 228
    - non-Boolean architectures 228–231
    - non-toggle memory 225–226
    - switching 226, 227
  - sub-band gap region 42
  - sub-micron CMOS technology 18
  - substoichiometric molybdenum trioxide 77
  - subthreshold slope (SS) 2, 36, 46–48, 107, 151, 180, 189, 193, 194
  - subthreshold swing (SS) 4, 36, 59, 100, 120, 151, 152, 154–156, 172–174, 181, 182, 191–194
  - superconducting circuits, quantum information 21–22
  - surface activated bonding (SAB) 11
  - system-in-package (SIP) 8
- t**
- terahertz biomedical sensor 241
  - terahertz emitters 240
  - terahertz frequency range 237, 239
  - terahertz imaging 238
  - terahertz photons 238–240
  - terahertz spectroscopy 238
  - terahertz technology 237–239, 242
  - terahertz waves vs. radio-frequency and microwaves 238
  - ternary content addressable memory (TCAM) 231
  - thermal management 9, 201
  - thermal sidewalls 9
  - 3D integrated circuit (IC) 1, 8–13
    - challenges and limitations 13

- 3D integrated circuit (IC) (*contd.*)
    - industrial state 12–13
    - research state
      - bonding 3D IC 10–12
      - test and yield 12
      - thermal management 9
      - TSV 9–10
  - 3D packaging 8, 9, 13
  - 3D stacking technology 8
  - threshold voltage ( $V_t$ ) roll-off 2
  - through-silicon-vias (TSV) 8–10
  - toggle memory 217, 225
  - top-gated CNTFETs 124, 125, 130, 131
  - total potential energy, of nanomagnet 220
  - transconductance variation 37
  - transistor 201
    - energy dissipation 202
    - SPINFET 202
  - transistor operation 180
  - transistor technology 56, 122, 195
  - transition-metal dichalcogenide (TMD) 5, 55, 57, 76, 78, 81, 162, 164
  - trap neutrality level (TNL) 104, 105
  - tri-gate FETs 3
  - triple-patterning technology 7
  - tunnel field effect transistors (TFET) 108
    - band diagram 153, 154
    - band-to-band tunneling probability and current, modeling for 156
  - based biosensor
    - biomolecule-receptor conjugation 170
    - modeling scheme 170
    - non-equilibrium Green's function 169
    - response time improvement 173–174
    - working mechanism 169
  - design considerations 161–162
  - fabricated TFET, status of 162–166
  - low-power electronic computational elements 166
  - scalability 162
  - schematic diagram 153, 154
    - single carrier tunneling barrier and subthreshold swing 154–156
    - source-channel and drain regions, doping of 162
    - working principle 153–154
  - tunneling magnetoresistance (TMR) 215, 216, 223, 226
  - two-dimensional (2D) geometry 55
  - 2D material transistor and device technology
    - ambipolar property, of graphene 57–58
    - 2D-material based FETs 57
  - 2D ultrathin bodies (UTB) 8
- u**
- ultra-thin body (UTB) 5, 8, 35–37, 102, 103
- v**
- Van-Hove singularities 39
  - vapor-liquid-solid (VLS) method 43–46
  - vertical nanowires 45
  - Villari effect 224
  - voltage controlled magnetic anisotropy (VCMA) 220–224
  - voltage-controlled magnet switching schemes 220
  - von Neumann (VN) *see* non-von Neumann (VN)
- w**
- wafer bonding method 102
  - wafer-on-wafer (WoW) bonding 10
  - wide bandgap semiconductors 242
  - winner-take-all (WTA) 17
  - wrap-around gated CNTFET 124
- x**
- X-on-insulator (XOI) 36
- y**
- Yttrium-based oxide, Ge 101
- z**
- zigzag nanotubes 122