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Wide-Bandgap Semiconductor Device Technologies for High-Temperature and Harsh Environment Applications

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CHAPTER MENU

1.1 Introduction

Silicon carbide (SiC) has become the preferred semiconductor material for harsh environment sensing applications, induction heating, photovoltaics, downhole oil development, and hybrid and electric vehicles because of its wide-bandgap energy (3.2 eV for 4H-SiC), excellent chemical and thermal stability, and high breakdown electric field strength (~2.2 MV cm^{-1}) [1–3]. Particularly in sensors and electronic systems which can operate in the temperature range 300–600 °C, are required for *in situ* monitoring of fuel combustion and subsurface reservoirs (i.e. deep well drilling), and for outer space exploration [3]. The use of semiconductor devices that can operate properly at such high temperatures would not only minimize the need for expensive and large cooling systems but also provide for improved system reliability [4]. SiC also has gained popularity as a material for both unipolar and bipolar power device applications under high-power, high-frequency and high-temperature conditions. Besides, high-temperature pressure sensors have been proposed and implemented using SiC-based piezoresistive devices and have demonstrated sensing capabilities

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between 350 and 600 °C [5]. Piezoresistive sensors, however, exhibit strong temperature dependence and suffer from contact resistance variations at elevated temperatures. Moreover, SiC has a longer lifetime, since it is an indirect bandgap material. The high lifetime yields a long diffusion length, and thus a high base transport factor. SiC is replacing Si as a semiconductor since SiC has the capability to be used in high-temperature, high-speed, and high-voltage applications. Most current SiC-based electronic devices are fabricated using either 4H- or 6H-SiC due to the aforementioned shortcoming of 3C-SiC. Between 4H- and 6H-SiC, 4H-SiC has substantially higher carrier mobility, shallower dopant ionization energies, and low intrinsic carrier concentration. Thus, it is the most favorable polytype for high-power, high-frequency, and high-temperature device applications. In addition, 4H-SiC has an intrinsic advantage over 6H-SiC for vertical power device configurations because it does not exhibit electron mobility anisotropy, while 6H-SiC does [6]. Indeed, many SiC device fabrication efforts have shifted toward 4H-SiC as it has become more readily available. For example, the unipolar 4H-SiC junction field-effect transistor (JFET) and the metal semiconductor field-effect transistor (MESFET) are seen as suitable structures for integrated circuit (IC) development since they do not suffer from gate oxide degradation.

Apart from SiC, gallium nitride (GaN) has gained much interest since it is naturally a high bandgap emitter. GaN not only has a higher bandgap, 3.4 eV, than SiC but it also has a high thermal conductivity, 1.3 $W\,cm^{-1}\,°C^{-1}$. GaN-based field-effect transistors (FETs) such as high-electron mobility transistors (HEMTs) and metal–oxide–semiconductor (MOS) channel HEMTs have shown outstanding properties in terms of achieving high breakdown voltage, low on resistance, and high switching frequency [7, 8].

In the field of light emitting diode (LED) devices, several trends are pushing research into new materials to improve their efficiency. LED efficiency is increasing by strain control of epitaxial films that compose the LED's active region structure [9]. Heterostructures of GaInN and GaN are used to produce a strain-relieving layer located beneath the active region [10]. Moreover, implementation of LED driver circuits using GaN-based FETs can potentially increase their efficiency and improve switching frequencies.

Wide-bandgap emitters are also bringing semiconductor technology to full color displays [11]. For the first time, all three primary colors can be generated using semiconductor technology, which promises to allow the reliability, compactness, and other desirable attributes of semiconductors to be applied to this important technological market [11]. Besides, diluted magnetic semiconductor (DMS) Ni^2: ZnO are ferromagnetic at high temperatures, which is attributed to the increase in domain volumes and the generation of lattice defects upon aggregation [12].

In this chapter, we focus on the crystal structures of SiC, GaN, and AlN. Then, we correlate their structures with their applications in JFET, metal oxide semiconductor field-effect transistor (MOSFET), MESFET, etc.

1.2 Crystal Structures and Fundamental Properties of Different Wide-Bandgap Semiconductors

1.2.1 Relevant Properties of GaN, SiC, and Si

Table 1.1 compares the relevant material properties of SiC and GaN with Si, the three most popular semiconductor device technologies for high-temperature applications. Most notable are the large thermal conductivities, breakdown voltages, and saturation velocities of SiC and GaN. The device maximum operating temperature parameter is calculated as the temperature at which the intrinsic carrier concentration equals 5×10^{15} cm^{-3} and is intended as a rough estimate of the bandgap limitation on device operation. More important for the eventual maximum operating temperature is the physical stability of the material.

1.2.2 Structure of SiC

1.2.2.1 Polytypism in SiC

SiC is the most prominent of a family of close-packed materials that exhibit a one-dimensional polymorphism called polytypism. The SiC polytypes are differentiated by the stacking sequence of the tetrahedrally bonded Si–C bilayers, such that the individual bond lengths and local atomic environments are nearly identical, while the overall symmetry of the crystal is determined by the stacking periodicity. Similar to silicon, SiC is a covalently bonded semiconductor. In the crystalline form, each silicon atom is covalently bonded to four neighboring carbon atoms to form a tetrahedron (Figure 1.1) and vice versa. There are two types of tetrahedrons in the SiC crystal. The first type is obtained by rotating another tetrahedron along its *c*-axis by 180°, and one type of tetrahedron is the mirror image of the other when the *c*-axis is parallel to the mirror. The *c*-axis denotes

Table 1.1 Comparison of important semiconductors properties for high-temperature electronics.

Property	Si	3C SiC (6H SiC)	GaN
Bandgap	1.1	2.2	3.39
Maximum operating temperature (K)	600	1200	
Melting point (K)	1690	Sublimes	
Physical stability	Good	Excellent	Good
Electron mobility (RT, cm^2 V^{-1} s^{-1})	1400	1000	900
Hole mobility (RT, cm^2 V^{-1} s^{-1})	600	40	150
Breakdown voltage (E_b, 10^6 V cm^{-1})	0.3	4	5
Thermal conductivity (c_T, W cm^{-1})	1.5	5	1.3

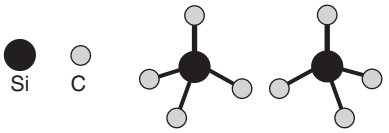


Figure 1.1 Two types of tetrahedrons forming the building blocks of all SiC crystals, with each tetrahedron consisting of one Si atom and four covalently bonded nearest-neighboring C atoms.

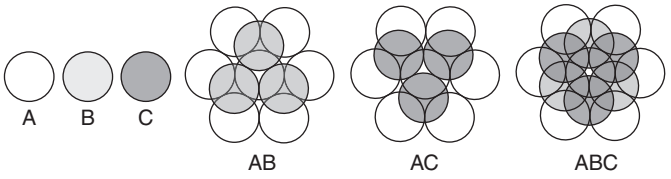


Figure 1.2 Three types (A, B, C) of Si–C double-atomic layer arrangement along the *c*-axis (stacking direction) through close-packed spheres. The *c*-axis is normal to the paper plane.

the direction normal to the Si–C double-atomic layers. In each layer, the silicon (or carbon) atoms have a close-packed hexagonal (HCP) arrangement. There are three types of sites (named A, B, C) in arranging the Si–C double-atomic layers, and each layer is normal to the *c*-axis (Figure 1.2).

A shorthand has been developed to catalog the literally infinite number of possible polytype crystal structures. Each SiC bilayer, while maintaining the tetrahedral bonding scheme of the crystal, can be situated in one of three possible positions with respect to the lattice. These are each arbitrarily assigned the notation A, B, or C. Depending on the stacking order, the bonding between Si and C atoms in adjacent bilayer planes is either of a zinc-blende (cubic) or wurtzite (hexagonal) nature. Zinc-blende bonds are rotated 60° with respect to nearest neighbors, while hexagonal bonds are mirror images (Figure 1.3). Each type of bond provides a slightly altered atomic environment, making some lattice sites inequivalent in polytypes with mixed bonding schemes and reducing the overall crystal symmetry. These effects are important when considering the substitutional impurity incorporation and electronic transport properties of SiC.

If the stacking is ABCABC…, the purely cubic zinc-blende structure, commonly abbreviated as 3C-SiC (or beta SiC), is realized (Figure 1.4). The number 3 refers to the three bilayer periodicity of the stacking, and the letter C denotes the overall cubic symmetry of the crystal. 3C-SiC is the only possible cubic polytype.

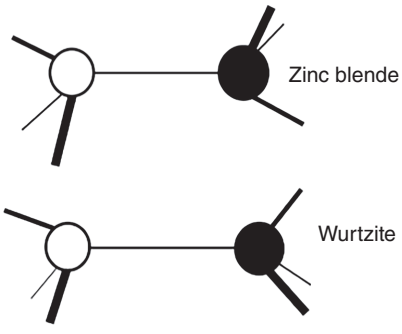


Figure 1.3 Zinc-blende and wurtzite bonding between Si and C atoms in adjacent planes. The three tetrahedral bonds are 60° rotated in the cubic case and mirror images in the hexagonal case.

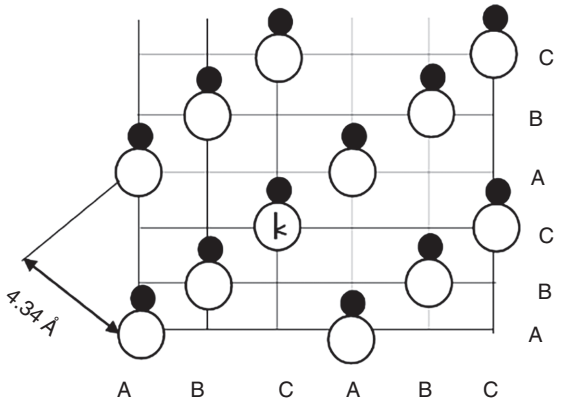


Figure 1.4 Crystal structure of the purely cubic 3C-SiC polytype: each lattice site (*k*, representing cubic symmetry) is equivalent.

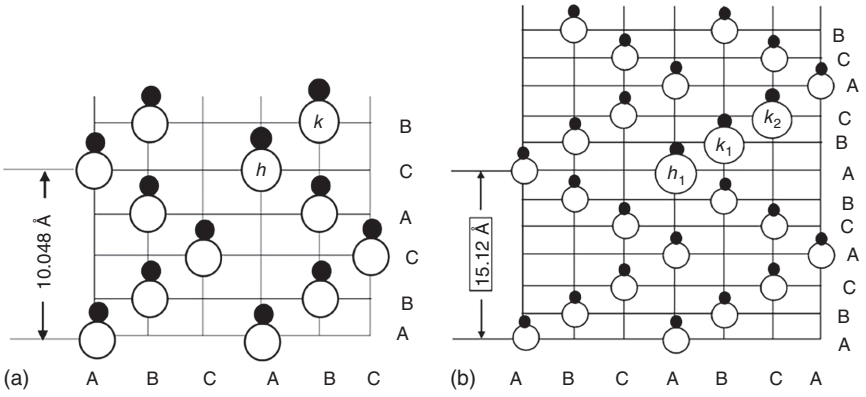


Figure 1.5 Crystal structure of (a) 4H-SiC polytype, where half of the atomic sites are hexagonally bonded (*h*), while half are cubic (*k*). (b) 6H-SiC polytype where the lattice is two-third cubic (k_1 and k_2) and one-third hexagonal (h_1). The two cubic sites are inequivalent and are expected to have slightly different binding energies for substitutional impurities.

All other polytypes are mixtures of the fundamental zinc-blende and wurtzite bonds.

Some common hexagonal polytypes with more complex stacking sequences are 4H- and 6H-SiC (Figure 1.5). 4H-SiC is composed equally of cubic and hexagonal bonds, while 6H-SiC is two-thirds cubic. Despite the cubic elements, each has overall hexagonal crystal symmetry. The family of hexagonal polytypes is collectively referred to as alpha SiC. Rhombohedral structures such as 15*R* and 21*R* have also been documented [13].

4H- and 6H-SiC are the only choices for wafer substrates since 3C-SiC wafers are not yet commercially available. Regardless of polytype, fabrication of devices directly on SiC wafers is hindered by lack of device quality wafers, inability to drive in surface doping, and poor electrical quality as a result of direct ion implantation into the substrate [14]. Therefore, the SiC electronics fabrication is mainly centered on epitaxial layers grown on these substrates. Currently, high-quality homoepitaxial layers of 4H- and 6H-SiC with different thicknesses and doping

levels are routinely produced. 3C-SiC is also gaining attention as it can be grown heteroepitaxially on various substrate materials. Furthermore, there has been significant progress in producing device-grade 3C-SiC epilayers in recent years. However, it is necessary to further reduce crystallographic structural defects in 3C-SiC epilayers before this polytype becomes a viable alternative to 4H- and 6H-SiC [15].

1.2.2.2 Modification of SiC Structures with Dopant

One of the major limitations in the development of wide-bandgap semiconductors has been finding suitable shallow dopants. Nitrogen is the most popular donor impurity, while Al is favored for p-type doping. Dopants may be introduced either during epitaxy or by ion implantation. In chemical vapor deposition (CVD), NH and triethylaluminum (TMA) have proved to be suitable dopant source gases for n- and p-type doping, respectively [16]. When N doping is introduced during the growth, carrier concentrations as high as 10^{18} cm^{-3} have been realized. Ion implantation with subsequent Ar annealing has yielded electron concentrations as large as 3×10^{19} cm^{-3} at an N volume concentration of 5×10^{20} cm^{-3} [17].

p-Type doping is a recognized problem in SiC, although considerable progress has been made. All of the acceptor impurities thus far investigated, namely, Al, B, Ga, and Sc, form deep levels and are difficult to activate, generally requiring a high-temperature anneal. Al is somewhat difficult to incorporate into the SiC lattice, and high carrier concentrations are difficult to achieve. p-Type carrier concentrations in the 10^{19}–10^{20} cm^{-3} range using TMA in a CVD process on the Si face of 6H SiC has been reported [18]. Growth on the C face resulted only in a hole concentration of 2×10^{8} cm^{3}. The carrier concentration was easily controllable down to the low $p = 10^{16}$ cm^{-3} range. On the upper end, the observed hole concentration became nonlinear as a function of TMA flow above 10^{19} cm^{-3}.

The dopants can occupy either hexagonal or cubic sites in the more complex SiC polytypes. These different environments give rise to different binding energies, and care must be taken when deconvolving the separate contributions from Hall data. Analyzing several samples, it was confirmed that the relative abundance of the various N dopant levels corresponded to the ratio of available binding sites. That is, in 4H-SiC, an equal number of donors occupy cubic sites and hexagonal sites. In 6H-SiC, the ratio is 2 : 1, reflecting the fact that two-thirds of the bonding is cubic. In 6H-SiC, the measured ionization energy of the hexagonal site was 85.5 meV, while the cubic sites were 125 meV (h and k_1, k_2, respectively, in Figure 1.5b). For 4H-SiC, the hexagonal and cubic binding energies were measured to be 45 and 100 meV, respectively. In 3C-SiC, a value of 48 meV for the lone cubic site was determined. Typical compensation values were 1–2 orders of magnitude below the observed electron concentration.

1.2.3 III–V Nitride-Based Structure

The III–V nitrides have long been viewed as a promising system for optoelectronic applications in the blue and ultraviolet (UV) wavelengths and, more recently, as a high-temperature, high-power semiconductor with electronic

properties potentially superior to SiC; however, progress in the nitrides has been much slower than that in SiC and ZnSe. Since GaN development presently lags behind that of ZnSe, many research groups have overlooked the long-term advantages of the nitrides for emitting and detecting applications.

The wurtzite nitride polytypes form a continuous alloy system whose direct room temperature (RT) bandgaps range from 6.2 eV in AlN to 3.4 eV in GaN. The high thermal conductivity and superior stability of the nitrides and their substrates should eventually allow higher power laser operation with less rapid degradation than ZnSe.

1.2.3.1 Fundamental Properties of GaN and AlN

GaN and AlN have a smaller lattice mismatch than that of any of the ZnSe alloys, which permits greater range and flexibility in heterostructure design. A comparison of some important properties of GaN and AlN semiconductors is shown in Table 1.2.

1.2.3.2 Nitride Crystal Growth

The earliest investigations of III–V nitrides were made on small crystals or powder samples. Johnson et al. [19], in what we believe to be the earliest report of GaN, first described the conversion of metallic Ga in a NH_3 stream into GaN via the reaction:

$$2Ga + 2NH_3 = 2GaN + 3H_2$$

The property of GaN produced by this technique was not up to the mark. Hence, nearly every crystal growth technique, substrate type, and orientation has been tried in an effort to grow high-quality III–V nitride thin films. Maruska and

Table 1.2 Some important properties of III–V nitride semiconductors.

	Wurtzite polytype	Zinc-blende polytype
GaN		
Bandgap energy	E_g, (200 K) = 3.39 eV	E_g (300 K) = 3.2–3.3 eV
Temperature coefficient	$dE_g/dT = -6.0 \times 10–4$ eV K^{-1}	
Lattice constant	$a = 3.189$Å $c = 5.185$ Å	$a = 4.52$ Å
Thermal expansion	$\Delta a/a = 5.59 \times 10^{-6}$ K $\Delta c/c = 3.17 \times 10^{-6}$ K	
Thermal conductivity	$K = 1.3$ W cm^{-1} K^{-1}	
AlN		
Bandgap energy	E_g (300 K) = 6.2 eV	E_g (300 K) = 5.11 eV
Lattice constant	$a = 3.112$Å $c = 4.982$ Å	$a = 4.38$ Å
Thermal expansion	$\Delta a/a = 4.2 \times 10^{-6}$ K $\Delta c/c = 5.3 \times 10^{-6}$ K	
Thermal conductivity	$K = 2$ W cm^{-1} K^{-1}	

Tietjen grew the first single-crystal epitaxial GaN thin films by vapor transport [20]. In their method, HCl vapor flowed over a Ga melt, causing the formation of GaCl, which was transported downstream. At the substrate, the GaCl mixed with NH_3, resulting in the following chemical reaction [21]:

$$GaCl + NH_3 = GaN + HCl + H_2$$

Maruska and Tietjens's approach was an early version of the modern-day metalorganic vapor-phase epitaxy (MOVPE) GaN growth technique. In MOVPE, trimethylgallium (TMG), TMA, and trimethylindium (TMI) react with NH_3, at a substrate which is heated to roughly 1000 °C [22].

A disadvantage of the MOVPE approach is the high substrate temperature necessary to thermally dissociate NH_3. Due to thermal mismatch with all of the available substrates, post-growth cooling introduces significant amounts of strain and defects into the nitride film.

In an effort to reduce substrate temperatures, many groups have begun exploring a molecular-beam epitaxy (MBE) approach in which the reactive nitrogen is supplied by microwave plasma excitation [23, 24]. This has been made possible by the commercial development of compact electron–cyclotron–resonance (ECR) microwave plasma sources such as the Wavemat MPDR 610 and ASTEX CECR. These sources use a coaxial or cylindrical cavity geometry to efficiently couple microwave energy (2.45 GHz) into the nitrogen discharge region. The plasma stream is diffusive and neutral, providing atomic, molecular, and ionic N radicals to the growth surface.

1.2.3.3 Polytypism in the III–V Nitrides

GaN and AlN are all most commonly observed as the wurtzite 2H polytype (Figure 1.6a), but each can also crystallize in a metastable zinc-blende 3C structure Figure 1.6b) [25, 26]. In general, wurtzite material grows on hexagonal substrates, while zinc blende can be grown on cubic substrates. The exception

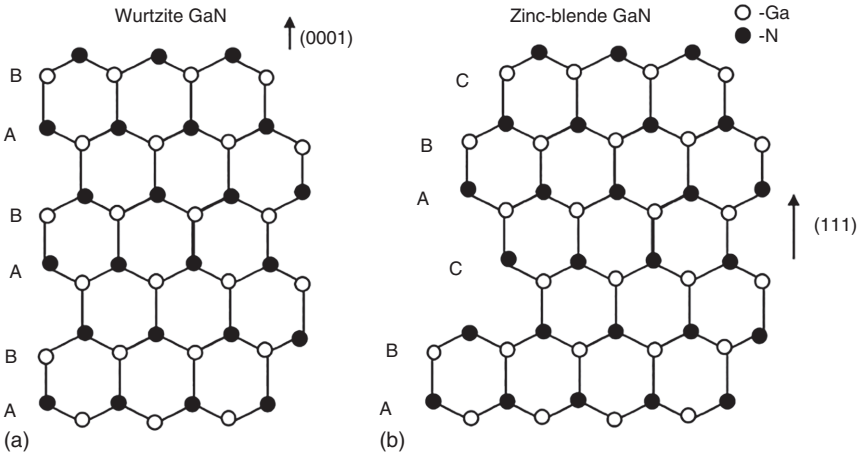


Figure 1.6 Crystal structures of the (a) GaN wurtzite (2H) and (b) zinc-blende (3C) polytypes.

is the sapphire (0001) and zinc-blende (111) faces, which are normal to the stacking direction, and are therefore polytype neutral.

1.2.3.4 Electrical Properties of Undoped Nitride Thin films

Using improved crystal growth techniques, researchers have succeeded in reducing the background electron concentration to 10^{16} cm^{-3}. High GaN bulk mobility of $\mu_m = 600$ and 1500 cm^2 V^{-1} s^{-1} at 300 and 77 K, was reported, respectively, in an unintentionally doped sample having $n = 4 \times 10^{16}$ cm^{-3}. AlN is always observed to be insulating, even when doped, almost certainly because its donor, acceptor, and defect levels all lie deep within the bandgap.

1.2.3.5 Properties of Doped GaN

Both p-type and n-type GaN doping has been the major catalyst of the rising interest in the nitrides. At first, Akasaki et al. [27] observed that compensated Mg-doped GaN could be converted into conductive p-type material by low-energy electron-beam irradiation (LEEBI). This result was improved by Nakamura et al. [28] to achieve GaN with $p = 3 \times 10^{18}$ cm^{-3} and a resistivity of 0.2 Ω cm. A model has been proposed [29] for describing H acceptor compensation in GaN in which Mg–H defect complexes are converted to conventional acceptor impurities by annealing or LEEBI. Due to the large binding energy (i.e. 150–200 meV) of Mg and possible residual H contamination, acceptor activation ratios of only 10^{-2}–10^{-3} are typically achieved. Thus, large amounts of Mg must be incorporated to obtain high doping levels in GaN. Work aimed at improving Mg activation or finding a better acceptor is needed.

It was reported that the carrier concentrations of Si-doped GaN grown by MOVPE were in the range of 10^{17} to 2×10^{19} cm^{-3}, while Ge doping produced material with electron concentrations of 7×10^{16} to 10^{19} cm^{-3} [30]. A linear variation in the electron concentration as a function of both the SiH_4 and GeH_4 flow rates was observed across the entire experimental range (Figure 1.7). Ge incorporation was roughly an order of magnitude less efficient than Si, as judged by the larger GeH_4 flow rates required to obtain similar electron concentrations.

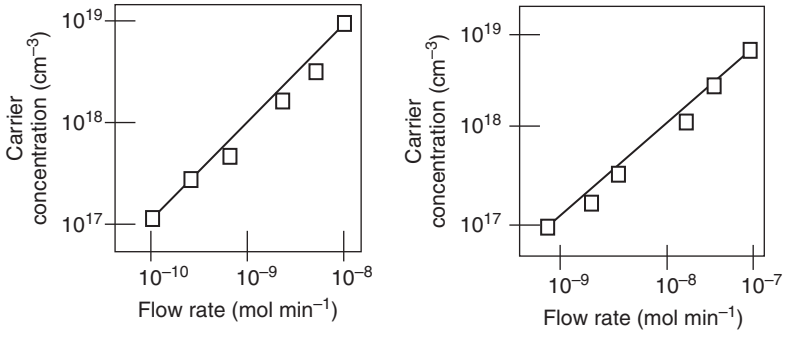


Figure 1.7 MOVPE (a) Si and (b) Ge incorporation rates as a function of gas flow. Both dopants are well behaved, with linear flow versus active donor incorporation rates; however, GeH_4, requires a factor of 10 higher flow to obtain the same doping level. Source: Nakamura et al. 1992 [30]. Redrawn with permission of IOP.

1.2.4 Alloys and Heterostructures

Most semiconductor devices are optimized by heterojunctions, which are commonly achieved through the use of alloys. GaN-based technology depends heavily on its alloys with AlN and possibly with InN.

1.2.4.1 GaInN

One of the major issues for better power efficiency is the strain control of epitaxial films that compose the LED's active region structure [9]. For example, having a strain-relaxed multiple quantum well (MQW) active region reduces the quantum-confined Stark effect (QCSE) in the quantum wells (QWs) and leads to a higher radiative efficiency [31]. An electron–hole recombination will proceed more rapidly if the coupling between the initial and final state is stronger. To control strain in LED structures, one typical method is to use a strain-relieving layer located beneath the active region [32]. A GaInN underlayer can reduce strain in QWs in a simple and effective way, resulting in a decrease in the QCSE [33]. Growing a GaInN layer underneath an MQW active region creates tensile strain in the following GaN quantum barrier (QB) and thus reduces the compressive strain in the GaInN. QW grown on top of the QB layer leads to a lower piezoelectric field in the QW and to enhance radiative efficiency. Research groups, having grown GaInN underlayers in GaInN LEDs, found several typical trends including (i) a decreased blueshift of the peak wavelength as the injection current increases, (ii) a reduced QCSE, and (iii) a reduced efficiency droop at high currents [32, 33].

1.3 Devices of Wide-Bandgap Semiconductors

1.3.1 SiC in Junction Field-Effect Transistors (JFETs)

There is growing interest in 4H-SiC because of its larger bandgap energy and higher electron mobility (950 $cm^2\,V^{-1}\,s^{-1}$ perpendicular to the *c*-axis and 1150 $cm^{-2}\,V^{-1}\,s^{-1}$ parallel to the *c*-axis) as compared with 6H-SiC, and its commercial availability in wafer sizes up to 6 in. in diameter. Depletion-mode 4H-SiC n-channel JFETs were designed for low-voltage and good characteristics at temperatures ranging from RT up to 600 °C in air [34]. The schematic of the device, shown in Figure 1.8, was a p-type 4H-SiC wafer substrate on which three epitaxial layers were grown: firstly a 5-μm-thick lightly doped p-type (p^-) layer, followed by a 300-nm-thick n-type (n) layer, and finally a 200-nm-thick heavily doped p-type (p^+) layer [34]. The p^+ layer is used to form the gate electrode, whereas the n layer comprises the channel region of the JFET. The thickness and dopant concentration of the n layer set the threshold voltage (V_T) of the transistor. Then a 1-μm-thick SiO_2 masking layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) and patterned to expose the source and drain regions to nitrogen implantation at 600 °C to form heavily doped n-type (n^+) regions required for practically ohmic metallic contacts. Subsequently, a multilayered stack of 50 nm titanium (Ti), 100 nm nickel (Ni), and 50 nm titanium–tungsten (TiW, 10% Ti, 90% W) was deposited and patterned via liftoff to form the metal contacts.

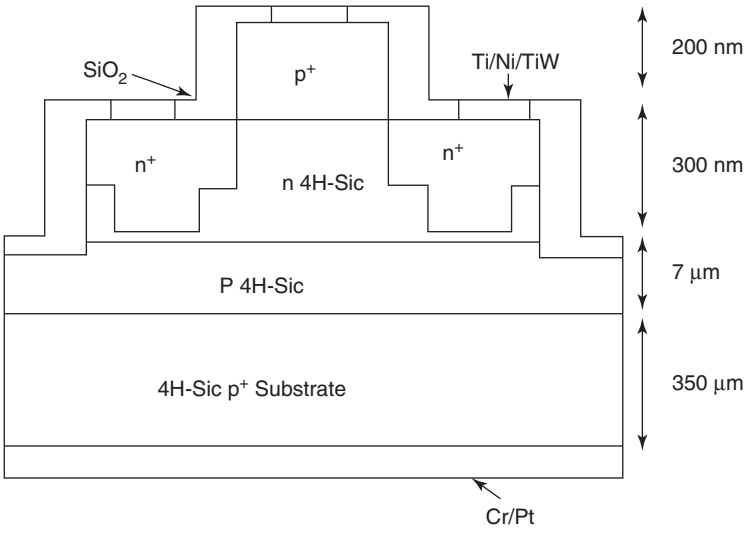


Figure 1.8 Schematic cross-section of 4H-SiC lateral JFET. Source: Redrawn from [34].

Ti/Ni/TiW metal stacks are used to form ohmic contacts to n-type 4H-SiC with specific contact resistance of $1.14 \times 10^{-3}\ \Omega\,\text{cm}^2$ at 600 °C. This contact is rectifying (i.e. a Schottky contact) and becomes ohmic after rapid thermal annealing (RTA).

1.3.1.1 Specific Contact Resistance (ρc)

Figure 1.9 shows how ρ_c depends on temperature. It decreases slightly with increasing temperature in the range from 25 to 400 °C due to the increasing average electron kinetic energy and hence current density [35]. However, it increases with increasing temperature in the range from 400 to 600 °C, due to thermal degradation of the metal contacts.

I–V Characteristics Figure 1.10a,b shows how the drain current versus drain-to-source voltage (I_{DS}–V_{DS}) curve for gate-source voltage (V_{GS}) equal

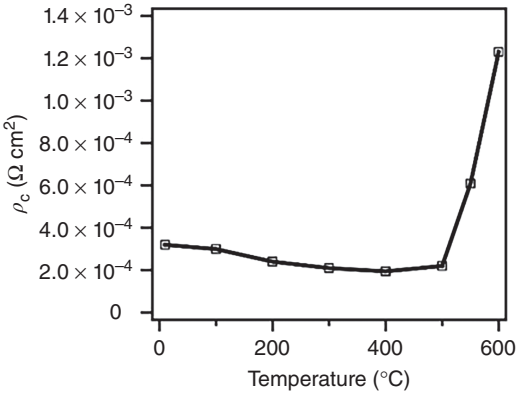


Figure 1.9 Temperature dependence of specific contact resistance (ρ_c) for a Ti/Ni/TiW metal stack on n+ 4H-SiC. Source: Chang et al. 1971 [35]. Redrawn with permission of Elsevier.

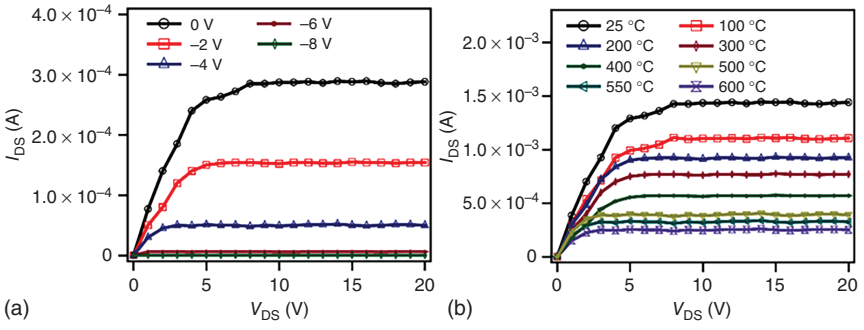


Figure 1.10 Measured I_{DS}–V_{DS} characteristics of 4H-SiC n-channel JFET with $W/L = 100/10$ µm. (a) At 600 °C, for different values of V_{GS}. (b) At various temperatures, for $V_{GS} = 0$ V.
Source: Malhan et al. 2009 [36]. Redrawn with permission of John Wiley & Sons.

to 0 V changes with temperature. Despite the built-in voltage decreases by approximately 0.5 V [36], the effective width of the channel becomes wider from 25 to 600 °C. A monotonic decrease in drain saturation current (I_{Dsat}) with increasing temperature is observed. This can be attributed to the decrease in electron mobility at elevated temperatures, which follows a power law [37]. This decrease also causes specific on resistance ($R_{on,sp}$) to increase to 280.2 mΩ cm^2 at 600 °C.

The off-state current (I_{off}) for $V_{GS} = -9$ V increases from 6.31×10^{-9} A to 1.97×10^{-7} A as the temperature increases from RT to 600 °C, due to increased intrinsic carrier concentration [37]. However, the increase in I_{off} is significantly larger than theoretically predicted, suggesting the presence of trap states (e.g. associated with crystalline defects caused by ion implantation). The saturation ($V_{DS} = 20$ V) on-current ($V_{GS} = 0$ V) to off-current ($V_{GS} = -9$ V) ratio I_{Dsat}/I_{off} is 2.66×10^5 at RT and decreases to 1.53×10^3 at 600 °C. This is in contrast to the 6H-SiC n-channel JFET with $W/L = 200/10$ µm reported by National Aeronautics and Space Administration (NASA), which initially exhibited I_{Dsat}/I_{off} of only ~50 at 500 °C and after hundreds of hours of "burn-in" (to make the Ti/$TaSi_2$/Pt metal contacts ohmic) improved I_{Dsat}/I_{off} to be more than 10^3 [38].

1.3.2 SiC in Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs)

1.3.2.1 1200-V, 60-A SiC Power Module MOSFET

In aerospace industries, having high power density is a critical design target for the converters to save the weight and volume of the whole power conversion system onboard. Generally, higher power density can be achieved by either increasing the switching frequency of the converter to reduce the sizes of passive components or by pushing the operating temperature of the semiconductor devices to save on the cooling system [39]. In more electric aircrafts, there even exists a trend to mount the embedded generators, together with their power electronics units, directly onto the engine shafts as a starter and a generator in order to replace the bulky and heavy mechanical parts. Under such conditions,

the power converter will not only be switched at a high frequency but also be exposed directly to the harsh engine compartment environment with an ambient temperature of 200–250 °C [40]. An example of such a high-temperature and high-frequency converter is a three-phase voltage-source inverter used to operate an embedded generator/starter in the more electric aircraft. A 1200-V, 60-A phase-leg module generally satisfies the electrical specifications of the system [41]. To achieve this power module, the two most critical elements are the semiconductor device with high-temperature and high-frequency capabilities and the module package supporting these operations. In terms of the device, the wide-bandgap, unipolar SiC MOSFET is one of the promising solutions, featuring its potential of operating over 200 °C [42], and switching at a much higher frequency than Si insulated gate bipolar transistors (IGBTs) [43]. Compared to the SiC JFET, the SiC MOSFET also possesses the advantages of being normally OFF, easier gate driver design, and commercial availability at the time of the work.

1.3.2.2 Design of the 1200-V, 60-A Phase-leg Module

Here, three SiC MOSFETs (Cree CPMF-1200-S080B) and three SiC Schottky diodes (Cree CPW4-1200-S010B, 1200 V, 10 A each) were paralleled in each switch position in the module. To evaluate the high-temperature operation of the designed package, the module was also operated continuously in buck topology. Under the conditions given in Figure 1.11, the top switch temperature reached only 145 °C.

To further push the device temperature, the DC bus voltage and switching frequency were increased to 560 V and 100 kHz, respectively. Figure 1.12a shows the test waveforms under this condition, and Figure 1.12b shows the thermal map of the module when the device temperatures came very close to thermal equilibrium. As seen, all three top MOSFETs are above 190 °C and the middle device reaches 200 °C successfully.

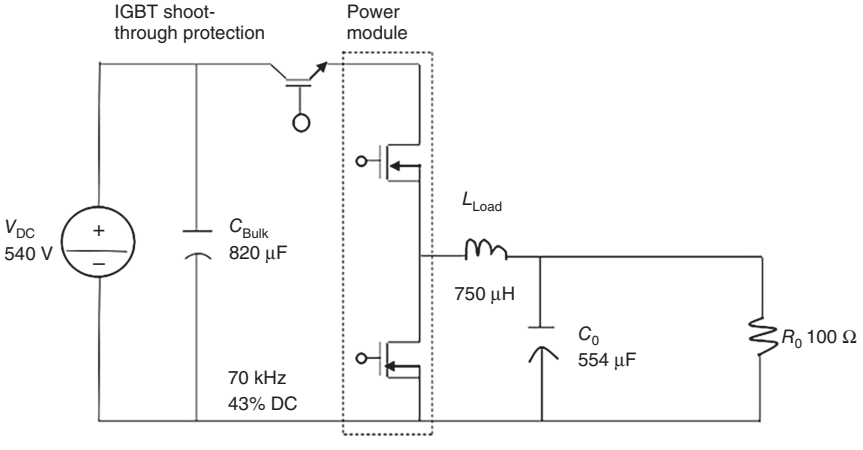


Figure 1.11 Circuit schematic of the continuous test. Source: Adapted from Chen et al. 2014 [41].

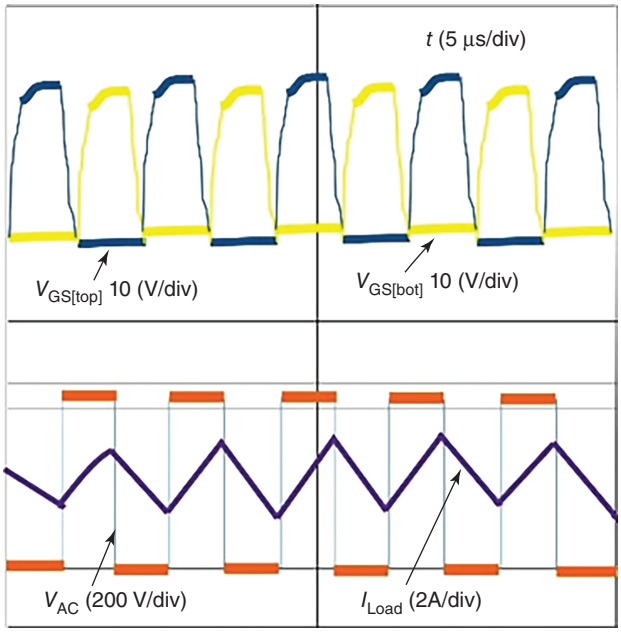


Figure 1.12 Test waveforms of the module at 560 V and 100 kHz. Source: Adapted from Chen et al. 2014 [41].

No shoot-through happened during the test and no thermal runaway was observed. The device temperatures still increased steadily even when approaching 200 °C. This verifies the previous device characterization results and indicates good performances of the SiC MOSFET at high temperatures. Temperature dependency characteristics of SiC MOSFET are also discussed [41].

1.3.2.3 Blocking Capability

Figure 1.13 depicts that I_{DSS} slightly increases with the temperature, and is measured below 10 µA at all temperature points. This indicates a very good blocking capability of the SiC MOSFET over a wide temperature range, especially

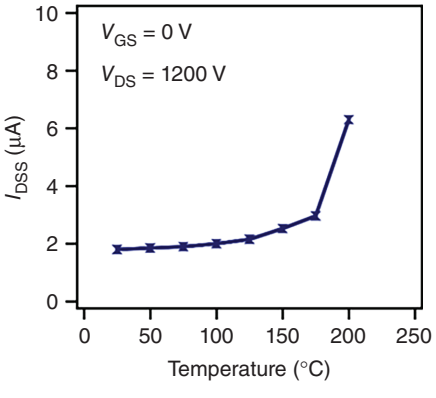


Figure 1.13 Leakage current versus temperature. Source: Adapted from Chen et al. 2014 [41].

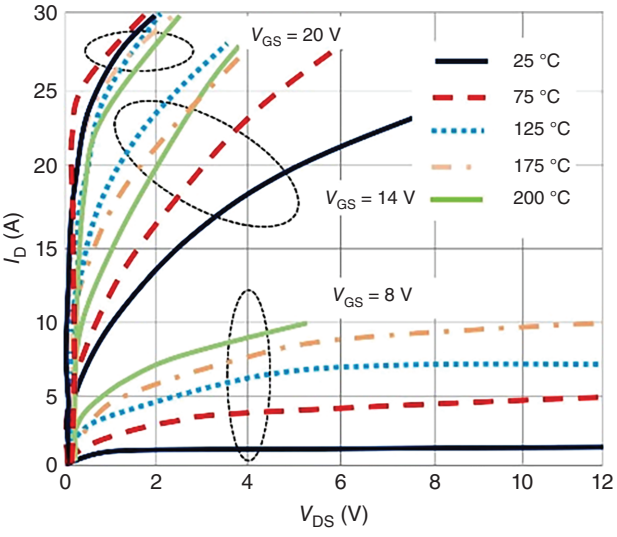


Figure 1.14 Temperature-dependent output characteristics. Source: Adapted from Chen et al. 2014 [41].

when compared to the conventional Si switches whose leakage currents usually increase significantly as the temperature goes above their maximum junction temperature (T_{Jmax}) around 150 °C [44].

1.3.2.4 Static Characteristics

The temperature dependence of the I–V curves is quite different from that of conventional Si MOSFETs, as shown in Figure 1.14. At low gate voltages (e.g. V_{GS} = 8 V), the slope of the I–V curve keeps increasing with the temperature, indicating a higher conductivity. At the full gate voltage of 20 V, on the contrary, the I–V curve always shifts to the right, showing a monotonously increasing drain resistance ($R_{DS(on)}$). There are also intermediate gate voltages (e.g. V_{GS} = 14 V) at which $R_{DS(on)}$ will first reduce and then increase. This special characteristic is due to the competing temperature dependences of the channel resistance R_{CH} and bulk resistance R_{Bulk} inside the device. For the temperature range up to 200 °C, the device channel mobility increases monotonously with the increasing temperature, resulting in a constantly decreasing R_{CH} at a given V_{GS}. The electron mobility in the drift region, however, decreases with the increasing temperature, causing R_{Bulk} to change in the opposite direction [45]. The temperature behavior of $R_{DS(on)}$ ($\approx$RCH + R_{Bulk}) can be determined by the ratio of R_{CH} and R_{Bulk} at the corresponding V_{GS}.

1.3.2.5 Transfer Characteristics

The device's transfer characteristics are shown in Figure 1.15. Similar to Si MOSFETs, a decreasing trend in the gate threshold voltage $V_{GS(th)}$ can be observed, causing the I–V curve to shift left. A more accurate measurement showed that $V_{GS(th)}$ dropped from 2.3 V at RT to only 1.4 V at 200 °C. Considering its fast

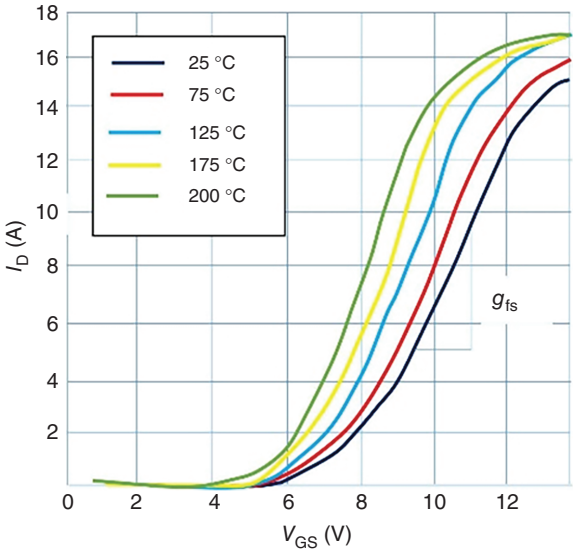


Figure 1.15 Temperature-dependent transfer characteristics. Source: Adapted from Chen et al. 2014 [41].

switching speed, the SiC MOSFET usually requires a negative turnoff bias to increase the threshold margin and dv/dt immunity, in order to avoid the false triggering in phase-leg operations.

Also note from Figure 1.15 that the MOSFET transconductance g_{fs}, i.e. the slope of the curve, increases slightly with the temperature, showing a trend opposite to that of Si MOSFETs. As $V_{GS(th)}$ and g_{fs} are closely related to the shape of the gate voltage waveform, and hence, the driving speed [46], the special static characteristics of the SiC MOSFET will cause its switching energies to exhibit quite different temperature dependence than Si.

1.3.2.6 Evaluation of the Gate Oxide Stability

Figure 1.16 shows the gate biasing test results up to 200 °C on two high-temperature modules. The $V_{GS(th)}$ changes under different temperatures are due to its temperature coefficient, whereas the changes over the time at each temperature indicates the characteristic degradation. As seen, for the first two 8 hours, no obvious change can be seen. However, at 175 °C, a maximum of 0.17 V positive shift can be observed from one of the samples, over a time span of 24 hours. For the subsequent soaking at 200 °C, the $V_{GS(th)}$ shift accelerates and increases by up to 0.3 V after 32 hours of stressing. From the trend in the figure, it can be inferred that the $V_{GS(th)}$ shift will continue but tends to saturate.

1.3.3 Six-Pack SiC MOSFET Modules Paralleled in a Half-Bridge Configuration

Paralleling helps achieve the required power level for induction heating, photovoltaics, and electric vehicles with today's available SiC power devices and also reduces the conduction loss [2]. Paralleling of the chips outside the module is

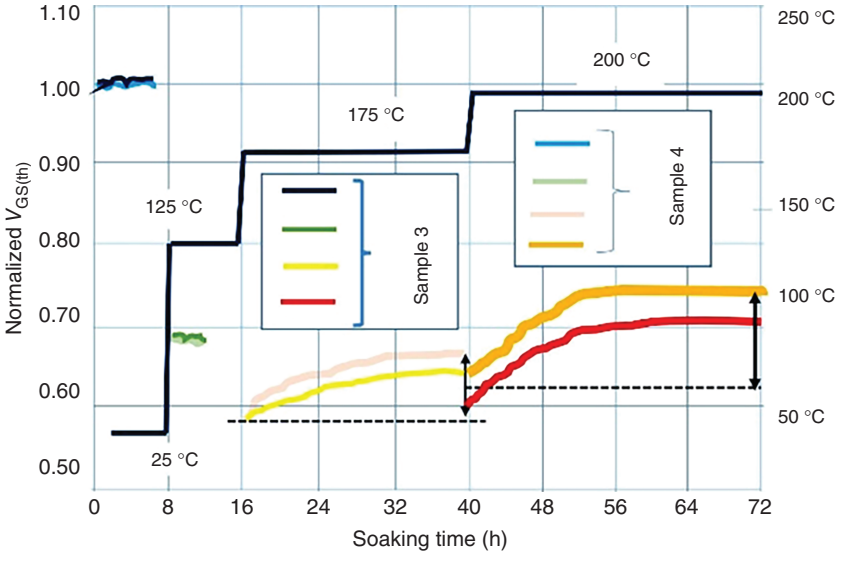


Figure 1.16 Normalized $V_{GS(th)}$ measured during the gate biasing test. Source: Adapted from Chen et al. 2014 [41].

mainly for achieving improved temperature performance compared to paralleling of the chips inside the module.

The switching performance of a SiC MOSFET module (CCS050M12CM2) is better than that of a Si IGBT module [47]. The standard double pulse test method is used to measure the switching performance. The total switching energy loss is nearly independent of the temperature for CCS050M12CM2.

Figure 1.17 depicts the turn-on and turn-off switching energy loss of CCS050M12CM2 at 600 V DC link voltage and varying load currents and junction temperatures. The measurement results show that the turn-on switching energy loss decreases slightly with increased junction temperature.

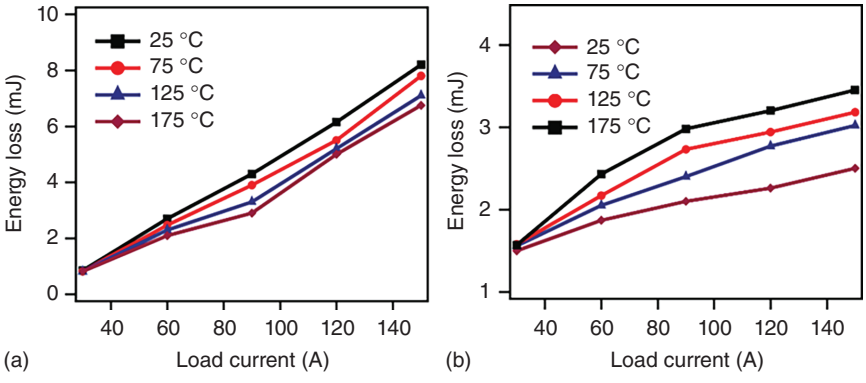


Figure 1.17 (a) Turn-on loss and (b) Turn-off loss of CCS050M12CM2 at 600 V. Source: Adapted from Tiwari et al. 2015 [47].

This can be explained by the fact that the threshold voltage decreases with higher junction temperature of the device under test, as shown in the datasheet of CCS050M12CM2. This results in faster turn-on of the device. On the other hand, the turn-off switching energy loss increases somewhat for higher temperatures, but with a slightly smaller amount than the decrease in turn-on switching energy loss.

1.3.4 4H-SiC Metal Semiconductor Field-Effect Transistor (MESFET) for Integrated Circuits (ICs)

Great efforts have been made in past few years in developing 4H-SiC MOSFETs by improving the SiO_2/SiC interface, although the gate oxide reliability still remains an issue. The unipolar JFET and the MESFET can be seen as suitable structures for IC development since they do not suffer from gate oxide degradation. The MESFET has quite a similar structure and operation as the JFET, the main difference relying on the gate terminal formation. Specially designed and fabricated 4H-SiC planar-MESFET is suitable for high-density SiC ICs [48].

1.3.4.1 Design of 4H-SiC MESFET

The isolation technique widely used in Si-ICs is the junction isolation technique, which is based on deep p^+ implant. This technique was typically used for the early design and fabrication technology of Si-ICs based on bipolar transistors [49]; thus, ensuring a better planarization of the wafer surface. Therefore, this typical Si-complementary metal–oxide–semiconductor (CMOS) isolation technique is practical for 4H-SiC individual device definition. Figure 1.18 shows the

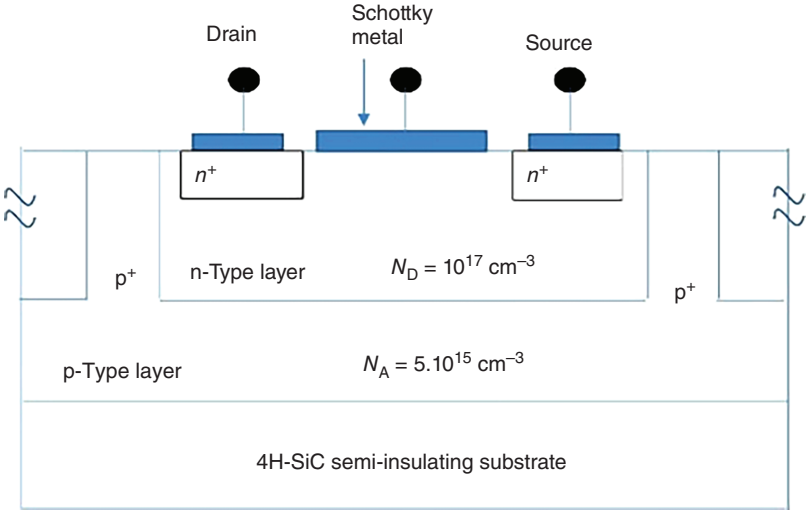


Figure 1.18 Schematic cross-section of the 4H-SiC planar-MESFET with p^+ implant isolation. Source: Adapted from Alexandru et al. 2013 [48].

schematic cross-section of the new planar-MESFET structure formed in n-type wells. The p^+-type impurities are deeply implanted into the n-epitaxial layers so that it reaches the p-type substrate, creating n-type islands.

1.3.4.2 *I–V* Characteristics

The high temperature measurements of the planar-MESFET reveals that drain current I_D shows a decreasing trend with increasing temperature, as depicted in Figure 1.19a. Moreover, the pinch-off voltage (V_P) does not depend on temperature, as shown in Figure 1.19b.

From 25 to 300 °C, the maximum drain current (I_{DSS}) at $V_G = 0$ V and the transconductance (g_m) decreases 66% approximately, fairly the same percentage for all three devices shown in Figure 1.20.

The subthreshold drain leakage current (I_R) evolution with temperature shows a linear behavior along the voltage range. Its average value increases

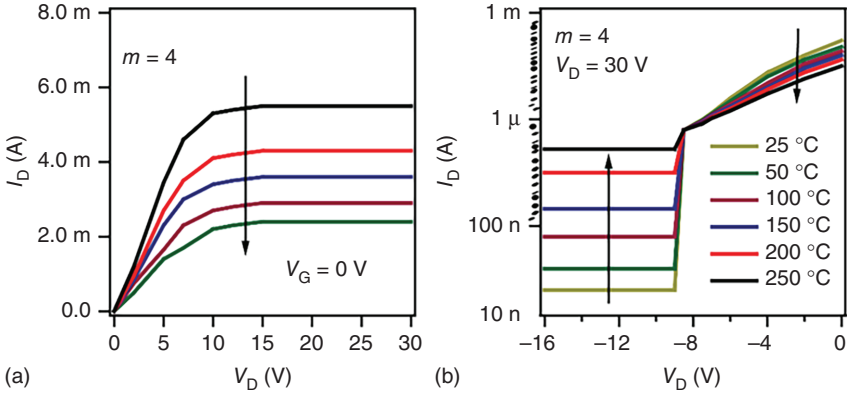


Figure 1.19 *I–V* characteristics of the 4H-SiC planar-MESFET ($m = 4$) versus temperature. Source: Adapted from Alexandru et al. 2013 [48].

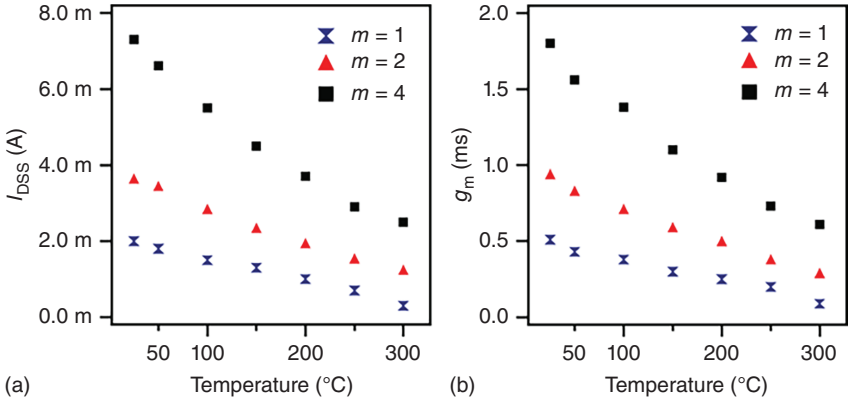


Figure 1.20 (a) The saturation drain current and (b) the transconductance evolution with temperature for all scalable 4H-SiC planar-MESFETs. Source: Adapted from Alexandru et al. 2013 [48].

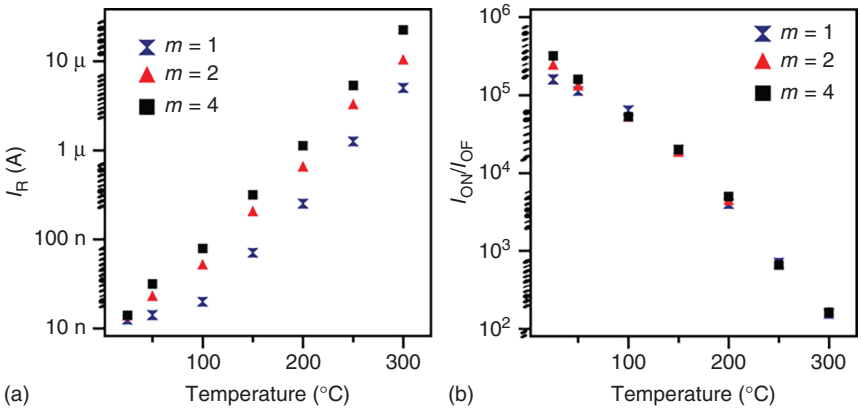


Figure 1.21 (a) The drain leakage current and (b) the I_{ON}/I_{OFF} ratio evolution with temperature for all scalable 4H-SiC planar-MESFETs. Source: Adapted from Alexandru et al. 2013 [48].

approximately 3 orders of magnitude at 300 °C with respect to 25 °C, as shown in Figure 1.21a. As a consequence, the I_{ON}/I_{OFF} ratio is strongly decreasing with temperature, as shown in Figure 1.21b.

Compared with the Si maximum working temperature (125 °C), SiC planar-MESFET I_{ON}/I_{OFF} ratio maintains a value above 10^4 for 150 °C, and approximately 5×10^3 at 200 °C, hence being in the Si CMOS logic range at 25 °C. For higher temperature operation, this ratio can be increased either by replacing the present Schottky metal with one having a higher barrier height or using JFETs instead of MESFETs. It may be noted that JFET shows lower subthreshold leakage current at high temperature than MESFET due to its higher gate barrier.

1.3.5 SiC Capacitive Pressure Sensor

High-temperature pressure sensors are critical for advanced industrial, automotive, and aerospace sensing applications. They have been proposed and implemented using SiC-based piezoresistive devices and have demonstrated sensing capabilities between 350 and 600 °C [5]. Piezoresistive sensors, however, exhibit strong temperature dependence and suffer from contact resistance variations at elevated temperatures, substantially degrading the sensor performance because the contact resistance variation is indistinguishable from the piezoresistance change caused by the pressure to be sensed.

Figure 1.22 presents a simplified cross-sectional view of capacitive pressure sensor [50]. The device consists of an edge-clamped circular 3C-SiC diaphragm suspended over a sealed cavity on a silicon substrate. The 3C-SiC film is grown epitaxially on a silicon substrate by atmospheric pressure CVD. The diaphragm deflects toward the substrate under an increasing external pressure, thus increasing the device capacitance value between the diaphragm and substrate. Once the diaphragm touches the substrate at a designed touch-point pressure (P_T), the sensor capacitance increases near linearly with pressure due to the linearly increasing touched area [51].

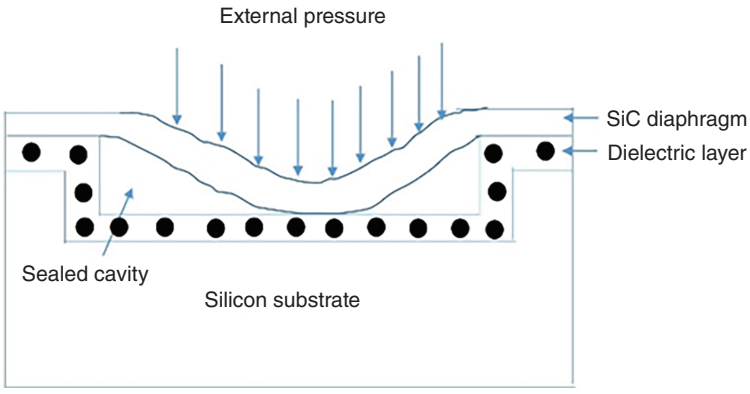
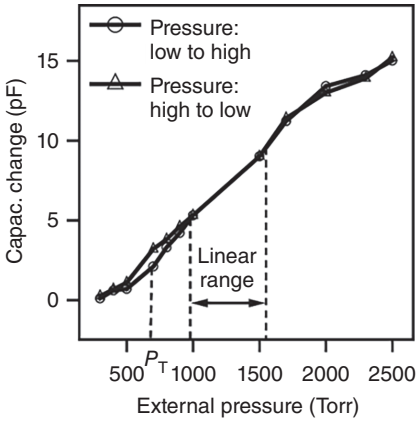


Figure 1.22 SiC pressure sensor cross-sectional view. Source: Adapted from Young et al. 2004 [50].

Figure 1.23 Sensor characteristic response at 200 °C. Source: Adapted from Young et al. 2004 [50].



1.3.5.1 Sensor Characteristics at High Temperature

Figure 1.23 presents the measured sensor capacitance change versus an externally applied pressure at 200 °C. The device exhibits a touch-point pressure of approximately 720 Torr with a total capacitance change of 13.5 pF over a pressure range from 295 to 2500 Torr. The sensor achieves a linear characteristic response between 900 and 1450 Torr with a sensitivity of 8.0 fF $Torr^{-1}$ and enters a saturation region with a reduced sensitivity beyond 1500 Torr due to the device geometry.

The high-temperature sensor performance has been demonstrated up to 400 °C, as shown in Figure 1.25. At 400 °C, the device exhibits an expected touch-mode behavior with a touch-point pressure of approximately 1000 Torr and achieves a linear characteristic response between 1100 and 1760 Torr with a sensitivity of 7.7 fF $Torr^{-1}$, a linearity of 2.1%, and a hysterisis of 3.7%. The measurement results indicate that the prototype capacitive pressure sensor is tolerant of contact resistance variations at elevated temperatures.

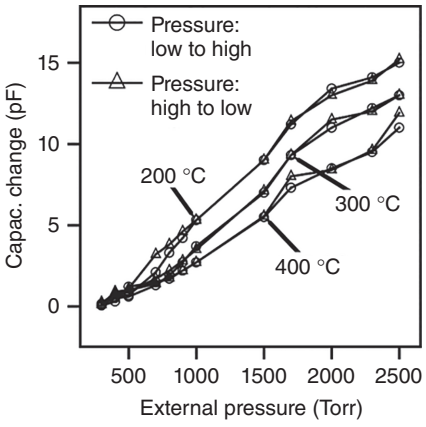


Figure 1.24 High-temperature sensor response. Source: Adapted from Young et al. 2004 [50].

However, the device exhibits separate characteristic curves at different temperatures, as shown in Figure 1.24, due to the trapped air inside the cavity. The trapped air causes the sensor touch-point pressure to increase near linearly with the temperature, thus resulting in separate characteristic curves. This temperature-dependent effect can be substantially minimized by eliminating the trapped air inside the cavity, which can be achieved by wafer bonding in vacuum. The device characteristics measured at the same temperature at different days show a maximum capacitance variation of 0.3 pF within the linear range, thus responding to a sensing repeatability of 39 Torr (52 mbar).

1.3.6 Ni^{2+}-doped ZnO as Diluted Magnetic Semiconductors (DMSs)

High-temperature ($T_c > 350$ K) ferromagnetism is reported in the DMS Ni^{2+}:ZnO [12]. This DMS is prepared from a solution at low temperatures. A modified synthetic procedure has been used: a suspension of LiOH in EtOH was added to an EtOH solution of $Zn(OAc)_2\ 2H_2O$ and Ni $(OAc)_2\ 4H_2O$ (~10 mol% Ni^{2+}) at 65 °C. After nucleation, nanocrystals were grown at 25 °C to the desired size. The nanocrystals are selectively precipitated, washed, and resuspended in EtOH to give a clear colloidal dispersion. An iso-crystalline core/shell procedure [52] involving epitaxial growth of ZnO shell layers on the nanocrystal surfaces is applied to internalize any surface-exposed Ni^{2+}. After further purification, the clear colloidal suspensions are concentrated and the nanocrystals are allowed to aggregate slowly over a period of two weeks. The aggregation is irreversible and the nanocrystals cannot be redispersed.

1.3.6.1 Saturation Magnetization (Ms) at High Temperatures

Figure 1.25 shows the high T_c ferromagnetism for Ni^{2+}-based DMSs at 350 K [12]. The temperature dependence of the saturation magnetization (M_s) for the hysteresis shows no evidence of a ferromagnetic phase transition (Figure 1.25 inset), indicating $T_c > 350$ K. At 350 K, an average saturation moment of ~0.057 μ_B/Ni^{2+} is determined. This value suggests that only a small fraction of the Ni^{2+} dopants gives rise to all of the observed ferromagnetism.

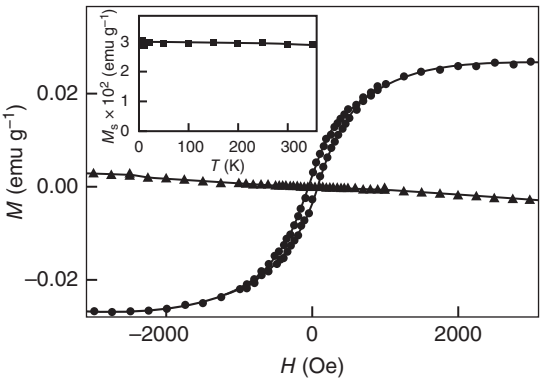


Figure 1.25 *M* versus *H* measurements of rapidly (▲) and slowly (●) aggregated 0 : 93% Ni^{2+}: ZnO nanocrystals at 350 K. Inset: Temperature dependence of M_s shown in inset. Source: Radovanovic and Gamelin 2003 [12]. Reproduced with permission of American Physical Society.

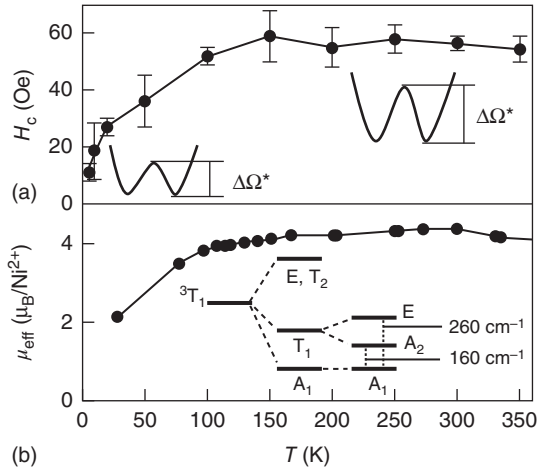


Figure 1.26 (a) Temperature dependence of H_c for 0 : 93% Ni^{2+}:ZnO nanocrystalline aggregates. The insets illustrate the change in the barrier to magnetization reversal ($\Delta\Omega^*$) as a function of temperature. (b) Temperature dependence of μ_{eff} for bulk 0.1% Ni^{2+}:ZnO [53]. The inset shows the spin–orbit (center) and trigonal (right) splitting pattern of the tetrahedral $Ni^{2+}3T_1$ (F) ground state (left). Source: Radovanovic and Gamelin 2003 [12]. Reproduced with permission of American Physical Society.

1.3.6.2 The Coercivity (Hc) and Effective Magnetic Moment (μeff) at High Temperatures

Figure 1.26a plots H_c as a function of temperature between 5 and 350 K. H_c increases with temperature up to 100 K and remains constant at higher temperatures. $M_r = M_s$ exhibits the same temperature dependence. Ferromagnetic ordering in ZnO DMSs is suggested to be charge-carrier mediated [54], in which case a temperature dependence of this type might potentially reflect thermally activated carrier detrapping. H_c can be associated with an activation barrier, $\Delta\Omega^*$, between local minima in the magnetization potential energy landscape, as illustrated in Figure 1.26a (inset).

The Ni^{2+} ion in DMS possesses both orbital and spin angular momentum in its electronic ground state, $^3T_1$(F). The $^3T_1$(F) multiplet is further perturbed by the trigonal ligand field provided by wurzite ZnO, resulting in the energy level splitting shown in Figure 1.26b (inset) [53]. The low-temperature ground state A_1 has no angular momentum ($J = 0$) and is perturbed by a magnetic field only in second order. The first sublevel of a low-symmetry split T_1 state possessing angular momentum ($J = 1$) and a nonzero first-order Zeeman

coefficient lies c. 160 cm^{-1} above the ground state. This electronic structure gives rise to a characteristic temperature dependence of the effective magnetic moment of paramagnetic Ni^{2+} ions ($\mu_{eff} = 2:828\,(\chi T)^{1/2}$), in which μ_{eff} increases with increasing temperature below 100 K due to thermal population of the T_1 sublevels. Experimental powder-averaged μ_{eff} data for bulk paramagnetic 0.1% Ni^{2+}:ZnO [53] are plotted as a function of temperature in Figure 1.26b. These data bear a remarkable similarity to the temperature dependence in H_c (Figure 1.26a). The temperature dependence of $\Delta\Omega^*$ can be attributed to temperature-dependent magnetic exchange interactions between the ferromagnetic domains and surrounding paramagnetic Ni^{2+} ions. Such interactions stabilize the magnetized domain against magnetization reversal and therefore increase $\Delta\Omega^*$ [55]. Increasing the temperature increases μ_{eff} of the paramagnetic ions, thereby increasing the exchange energy and, hence, also the coercivity. As a consequence, the same characteristic temperature dependence appears in both μ_{eff} and the hysteresis properties H_c and M_r. The insets of Figure 1.26a illustrate the change in $\Delta\Omega^*$ from low to high temperatures. In analogously prepared ferromagnetic Co^{2+}:ZnO aggregates, μ_{eff} of the paramagnetic Co^{2+} ions is temperature independent above ~10 K and the exchange interactions are therefore not evident [56].

1.3.7 Thermomechanical Stability of SiC, GaN, AlN, ZnO, and ZnSe

High-temperature mechanical properties (hardness) of the wide-bandgap semiconductors SiC, GaN, AlN, ZnO, and ZnSe have been reported [57] in comparison with those of other materials Si, GaAs, GaP, and a-sapphire. The hardness of single crystals α-SiC, GaN, AlN, ZnO, and ZnSe having 0.5 mm thickness at elevated temperatures is measured by the Vickers indentation method in the temperature range 20–1400 °C (Figure 1.27).

In the whole temperature range investigated, the hardness of SiC, GaN, AlN, and ZnO exhibits a gradual decrease from RT to around 600 °C, then something resembling a plateau in the range to around 1000 °C, and subsequently a steep

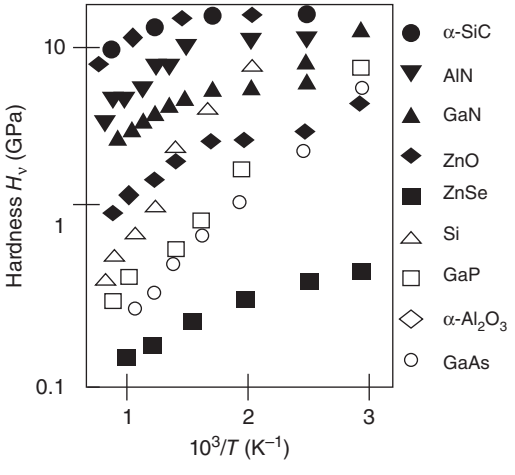


Figure 1.27 Vickers hardness of bulk single crystals α-SiC, AlN, GaN, ZnO, and ZnSe plotted against reciprocal temperature, with an applied load of 0.5*N* and dwell time of 30 seconds, together with those of Si, GaP, GaAs, and α-Al_2O_3. The hardness of α-Al_2O_3 obtained with an applied load of 2*N* and dwell time of 15 seconds is superimposed. Source: Radovanovic and Gamelin 2003 [12]. Reproduced with permission of American Physical Society.

decrease. This temperature-dependent tendency is common in semiconductors and sapphire, which have the HCP-based structure, although the temperature range and hardness magnitudes of SiC or α-Al_2O_3 are higher than that of AlN and GaN. The plateau may appear in relation to the operation of different slip systems in the crystal structure. It is found that in the whole temperature range investigated, the hardness magnitudes of ZnO are smaller than those of SiC, AlN, and GaN. At low-temperature regions, the hardness of GaN and AlN is comparable to, or a little lower than that of Si, although the hardness of Si may be affected by the phase transformation that occurs at a pressure of about 11.3 GPa beneath the indenter. It is surprising that up to about 1100 °C, GaN and AlN maintain their hardness and are harder than Si. Indeed, Si and GaAs exhibit a steep decrease in hardness from 500 and 200 °C, respectively, with an increase in the temperature, which indicates the beginning of macroscopic dislocation motion and plastic deformation. The present results indicate that this macroscopic dislocation motion and plastic deformation of SiC, GaN, and AlN may start at around 1100 °C. Over the whole temperature range investigated, ZnSe is known to be most unstable thermomechanically in the materials. From the results it is found that SiC, GaN, and AlN are of higher thermomechanical stability against deformation during device processing at elevated temperatures as compared with Si, GaP, GaAs, ZnSe and possibly other III–V and II–VI compounds with the sphalerite structure.

1.4 Conclusion

This chapter provides a brief overview of recent advances in wide-bandgap semiconductors capable of operating in harsh atmospheres. We have placed emphasis on how the unique electronic and thermal properties of these materials affect the functions and operational principles of electronic devices.

However, the technology of these materials is not yet mature. Significant technology challenges remain to be overcome for SiC- and GaN-based devices. The development of high-quality substrates for homoepitaxial growth is a constant challenge, although the most serious difficulty lies in the achievement of high doping levels and reproducible ohmic and Schottky contacts. Considering the maturity of the fabrication technology, large bandgap (larger than SiC) and thermomechanical material properties, GaN appears to be the best choice. The material quality and impurity doping issues associated with SiC make it presently unusable for high-temperature bipolar devices. However, because 4H-SiC has a bandgap close to GaN, it appears closer to beneficial high ambient temperature functionality.

SiC- and III-nitride-based devices have already been commercialized for applications such as fire sensors, engine control, or environmental monitoring. The success of these materials in the market will depend on the reproducibility and reliability of the devices. Wide-bandgap semiconductor electronics can be classified as a niche market technology that will offer a unique potential to cover a place market for high-temperature and harsh environment applications.

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