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Overview

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Micro-electro mechanical systems (MEMS) have been used for versatile components as sensors and are called microsystems. This technology is based on advanced arts of microfabrication developed for integrated circuit (IC) on a Si (silicon) wafer. The microfabrication uses patterning with photolithography by which many patterns on a photomask are transferred on the surface of the Si wafer. This batch transfer enables to fabricate10 billion transistors on a chip by using the latest technology, which corresponds to one trillion transistors on a 12 in. (300 mm) diameter Si wafer. We can fabricate thick (2.5 dimensional) structures by extending the microfabrication with etching and deposition. The extended technologies of microfabrication is called micromachining. The MEMS that have versatile components and circuits on a chip play important roles in advanced systems for user interface, wireless communication, Internet of things (IoT), and so on. This book *3D and Circuit Integration of MEMS* deals with various configurations of MEMS as shown in Figure 1.1. There are two kinds of MEMS. One is monolithic type called system on chip (SoC) MEMS and the other is hybrid type called system in package (SiP) MEMS. The former SoC MEMS means that MEMS and circuits can be fabricated on the same chip. This will be explained from Chapter 2 to Chapter 10. The SoC MEMS reduces interconnection complexity and enables arrayed active matrix MEMS; on the other hand it reduces the freedom of MEMS processes because of restrictions such as thermal budget limited by the circuits. The latter SiP MEMS means that MEMS and circuits are fabricated on different chips and assembled in a package as will be discussed later using Figure 1.5.

The bulk micromachining in Figure 1.1 will be described in Chapter 2, which uses etching of the bulk Si wafer to make MEMS structures. The surface micromachining in Figure 1.1 is shown in Figure 1.2a. Sacrificial layer is deposited and patterned followed by the deposition and patterning of structural layer. The sacrificial layer is selectively etched out, and the remained structural layer is used for the components of MEMS.

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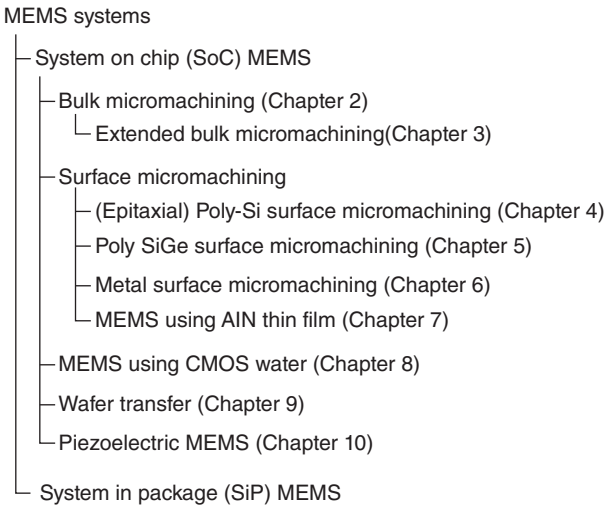

Figure 1.1 Various configurations of MEMS.

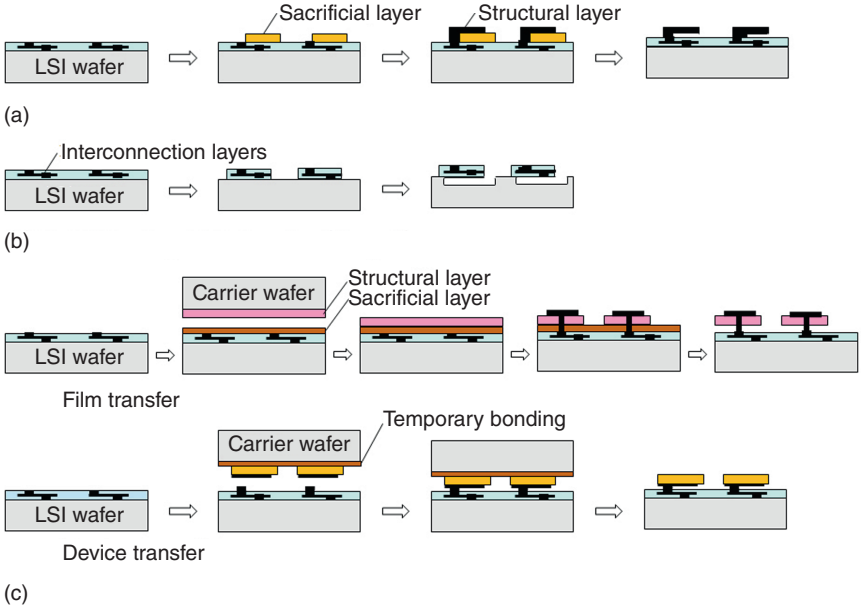

Figure 1.2 Various SoC MEMS by LSI first approach (a) Surface micromachining (deposition based) (chap. 4, 5, 6 and 7), (b) MEMS using CMOS wafer (chap. 8), (c) Wafer transfer (chap. 9 and 10).

MEMS by the surface micromachining integrated with n-channel MOS (NMOS) FET and complementary metal oxide semiconductor (CMOS) circuits are pioneered by Prof. R. T. Howe and Prof. R. S. Muller in the University of California, Berkeley, United States. The fabrication process of these will be explained later in Figure 1.3 and Figure 1.4, respectively. In recent years large-scale integration (LSI) uses standardized processes in foundries and the process is not flexible. For

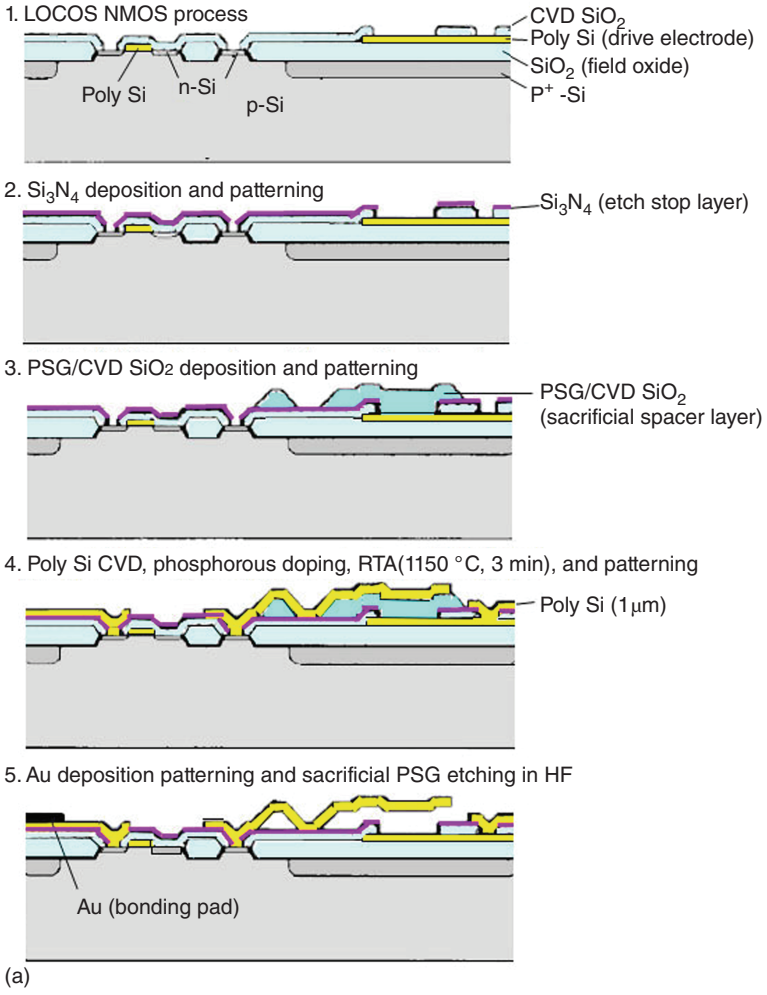

Figure 1.3 NMOS integrated poly Si resonant microstructure (SoC MEMS). (a) Fabrication process (b) Photographs of microstructure (c) Circuit with NMOSFET and resonator. Source: Putty et al. [1]. © 1989, Elsevier.

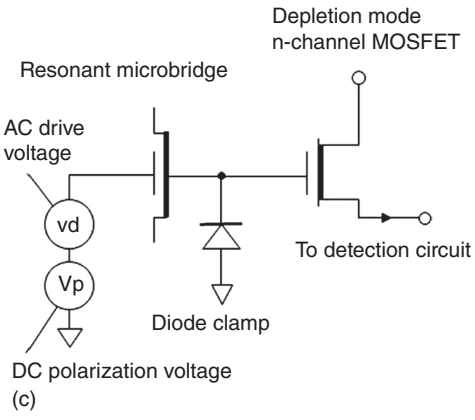

Figure 1.3 (*Continued*)

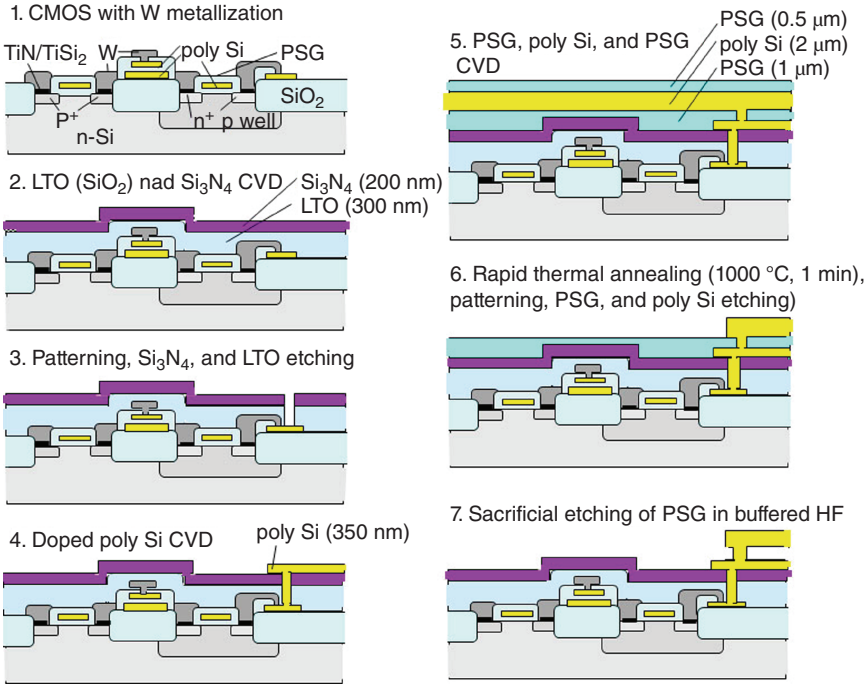

Figure 1.4 Fabrication process of surface-micromachined poly Si microstructures integrated with CMOS circuit. Source: Based on Yun et al. [2]; Bustillo et al. [3].

this reason, LSI first approach is commonly used as shown in Figure 1.2. This is required not to contaminate the LSI production line as well.

Polycrystalline Si (poly Si) surface micromachining uses poly Si as the structural layer. The surface micromachining using epitaxial poly Si (epi-poly Si) will be explained in Chapter 3. The poly Si has a good mechanical property as a material for spring, moving element, etc. and can be used for sensors or actuators as resonators. High temperature around 600 °C is required to deposit the poly Si by chemical vapor deposition (CVD). The co-fabricated IC has to stand this temperature. Resonant

microstructures made of poly Si were integrated with depletion type NMOS field effect transistor (FET) [4]. The fabrication process is shown in Figure 1.3a [1, 4]. The NMOS FETs that have poly Si gate are fabricated using conventional local oxidation of Si (LOCOS) technology. The poly Si layer for the gate of the FET is also used as a drive electrode for the resonator (1 in (a)). Si_3N_4 is deposited and patterned (etched after photoresist patterning) for the purpose of etch stop layer needed for the etching of the sacrificial layer (2 in (a)). Phosphosilicate glass (PSG) and SiO_2 are deposited by the CVD for the purpose of sacrificial spacer layer (3 in (a)). Poly Si is deposited at 600 °C and doped with phosphorous by ion implantation. It is patterned after rapid thermal annealing (RTA) at 1150 °C for three minutes. The RTA is needed to control the stress of the poly Si (4 in (a)). Au (gold) is deposited and patterned for bonding pads, and finally the PSG sacrificial layer is etched out in HF (hydrofluoric acid) to make poly Si microcantilever for the resonator (5 in (a)). The Au is used on behalf of conventional Al (aluminum) because the Au is not etched in HF. Photographs of the chip surface and the self-suspended poly Si cantilever fabricated are shown in Figure 1.3b. Circuit with the NMOS FET and the resonator (resonant microbridge) are illustrated in Figure 1.3c. The circuit for capacitance detection has to be monolithically integrated with the MEMS microstructure in order to minimize the influence of stray capacitance.

The surface-micromachined poly Si microstructures were integrated with CMOS circuit as well, being called modular integration of CMOS with microstructures (MICS) [2, 3]. The fabrication process is shown in Figure 1.4. The poly Si surface micromachining requires 600 °C for deposition, and the thermal budget requires metallization different from conventional Al. W (tungsten) and $TiN/TiSi_2$ were used for the metallization and diffusion barrier at the metal/silicon contacts, respectively, to stand the high temperature process (1 in the figure). Low-temperature oxide (LTO) (SiO_2) and Si_3N_4 are deposited by CVD (2 in the figure), and the Si_3N_4 and the LTO are patterned (3 in the figure). Doped poly Si is deposited and patterned (4 in the figure). PSG, poly Si, and 2nd PSG are deposited by CVD (5 in the figure). RTA is made and the PSG and the poly Si are patterned (6 in the figure). Movable poly Si microstructures are formed by sacrificial etching of the PSG in buffered HF (7 in the figure).

The thickness of the poly Si is limited to less than 2 μm because of its stress, which causes a bending of the wafer. On the other hand, low-stress epi-poly Si that makes a layer thickness of 20 μm or more possible was developed in Fraunhofer Institute for Silicon Technologies (ISIT) in Germany and Uppsala University in Sweden [5]. Surface micromachining using the epi-poly Si has been used for capacitive sensors as accelerometer and gyroscope. The lateral capacitance of micromechanical structure can be increased because of the thick epi-poly Si layer. The capacitance detection circuits need not to be monolithically integrated for the SoC MEMS. The epi-poly Si surface micromachining will be explained in Chapter 4.

The poly SiGe surface micromachining categorized in Figure 1.1 was developed to achieve low deposition temperature (410 °C) [6]. This will be explained in Chapter 5. Ge (germanium) is used as the sacrificial layer because it can be etched out selectively in H_2O_2 (hydrogen peroxide).

Metal surface micromachining was developed for the purpose of mirror array fabricated on a CMOS LSI. Metals can be deposited by sputtering or evaporation. Since it doesn't require high temperature, thermal damage to the CMOS LSI is not a problem and photoresist can be used as a sacrificial layer. The durability was improved by using amorphous metal. The mirror array has been used successfully for video projectors and other systems as will be explained in Chapter 6.

The other surface micromachining is a MEMS using AlN (aluminum nitride). The AlN is a piezoelectric material and can be deposited at low temperature by reactive sputtering. This enables SoC MEMS that have surface micromachined structures having piezoelectric material on a circuit. This will be explained in Chapter 7.

The MEMS using CMOS LSI wafer in Figure 1.1 is the SOC MEMS and schematically shown in Figure 1.2b. The multilayers for interconnection on a CMOS wafer and the bulk Si are used as the MEMS structure, and the Si under the MEMS structure can be under-etched if necessary. This will be explained in Chapter 8.

Wafer transfer methods shown in Figure 1.2c will be explained in Chapter 9. There are two ways. One is film transfer in which structural layer on the carrier wafer is transferred on an LSI wafer, and MEMS are fabricated on the LSI wafer. The other is device transfer in which MEMS are fabricated on the carrier wafer and transferred on the LSI wafer by using bump or other methods. The MEMS are left on the LSI wafer by etching out the carrier wafer or the temporary bonding layer, otherwise by debonding (laser lift-off) the MEMS from the carrier wafer. The advantage of the wafer transfer method is that the structural layer or MEMS are not fabricated on the LSI wafer but on the carrier wafer, and hence the fabrication process has flexibility. High temperature process can be applied on the carrier wafer.

Some piezoelectric material such as PZT (lead zirconate titanate) requires high temperature (700 °C) for deposition by sputtering. The wafer transfer method can be applied for the fabrication of the SoC MEMS with the PZT. The piezoelectric MEMS will be described in Chapter 10.

Monolithic SoC MEMS have been discussed earlier. The other approach is a hybrid type called SiP MEMS. MEMS chips and LSI chips can be connected with each other as shown in Figure 1.5. MEMS that have to be exposed as microphone use side-by-side configuration with LSI as shown in in Figure 1.5a. The side-by-side configuration of MEMS chip and LSI chip (Figure 1.5b) and the stacked configuration of MEMS chip on LSI chip (Figure 1.5c) are placed in a can or ceramic package. The side-by-side configuration of packaged MEMS chip and LSI chip (Figure 1.5d) and the stacked configuration of LSI chip on packaged MEMS chip (Figure 1.5e) can be molded with polymer. An advantage of the hybrid approach is that each MEMS and LSIs can be fabricated separately using optimized processes.

Unpackaged MEMS chips can't be molded with resin because these have moving elements on them. Packaging is needed for MEMS and especially a wafer level packaging plays important roles in MEMS [7]. Bonding, sealing, and interconnection are required for the MEMS process and the packaging. The packaged MEMS chip shown in Figure 1.5d,e uses glass frit (solder glass and low-melting-point glass) for the bonding and sealing. This will be explained using Figure 4.6 (Chapter 4) and Figure 17.35 (Chapter 17). Such elementary technologies for the MEMS packaging

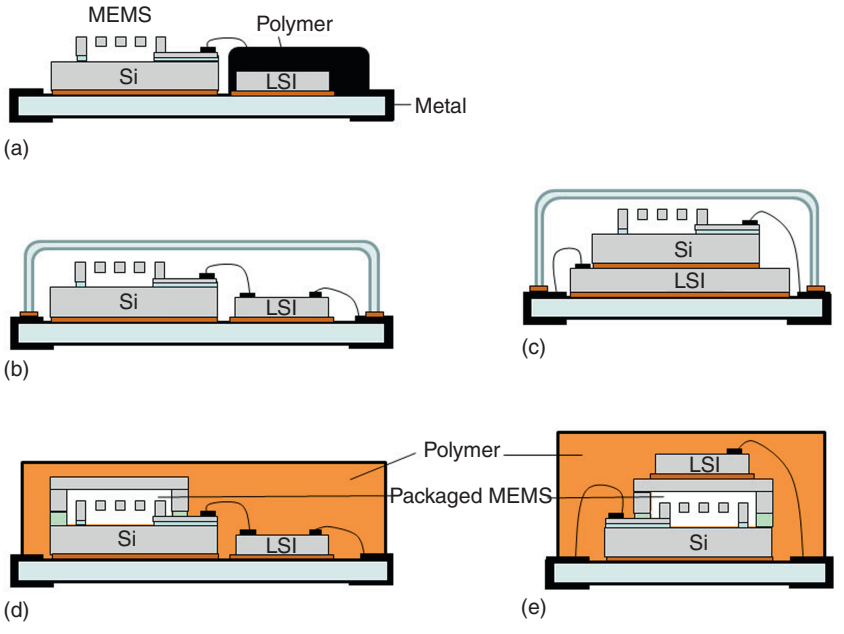

Figure 1.5 SiP MEMS (a) Side-by-side hybrid configuration of exposed MEMS chip and polymer coated LSI chip, (b) Side-by-side hybrid configuration of MEMS chip and LSI chip in can or ceramic package, (c) Stacked hybrid configuration of MEMS chip on LSI chip in can or ceramic package, (d) Side-by side hybrid configuration of packaged MEMS chip and LSI chip with polymer molding, (e) Stacked configuration of LSI chip on packaged MEMS chip with polymer molding.

Figure 1.6 Elementary technologies for MEMS packaging.

- Bonding
  - Anodic bonding (Chapter 11)
  - Direct bonding (Chapter 12)
  - Metal bonding (Chapter 13)
  - Reactive bonding (Chapter 14)
  - Polymer bonding (Chapter 15)
- Sealing and interconnection
  - Soldering by local heating (Chapter 16)
  - Packaging, sealing and interconnection (Chapter 17)
  - Vacuum packaging (Chapter 18)
  - Buried channel in monolithic Si (Chapter 19)
  - Through-substrate-vias (Chapter 20)

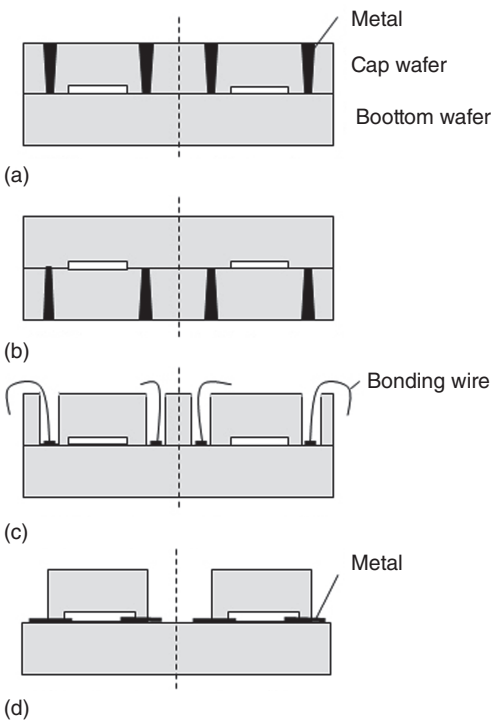

Figure 1.7 Interconnection methods from the packaged MEMS (a) Through-substrate-vias (cap), (b) Through-substrate-vias (bottom), (c) Wire-bonded through-Si vias, (d) Lateral feedthrough.

listed in Figure 1.6 will be explained from Chapter 11 to Chapter 20 of this book. Five bonding methods will be explained as follows. These are anodic bonding (Chapter 10), direct bonding (Chapter 11), metal bonding (Chapter 13), reactive bonding (Chapter 14), and polymer bonding (Chapter 15). Sealing and interconnection methods explained are soldering by local heating (Chapter 16), packaging, sealing, and interconnection (Chapter 17), vacuum packaging (Chapter 18), buried channel in monolithic Si (Chapter 19), and through-substrate vias (TSV) (Chapter 20). Interconnection methods from the packaged MEMS are categorized in Figure 1.7. The TSV in Figure 1.7a,b will be explained in Section 17.3.1 and Chapter 20. The technology called wire-bonded through-Si vias in (c) will be shown in Section 20.4.3.5 [8]. The lateral feedthrough interconnection in (d) will be discussed in Section 17.3.2.

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