

Contents

Volume 1

Preface *xiii*

Part I Silicon Carbide (SiC) 1

- 1 **Dislocation Formation During Physical Vapor Transport Growth of 4H-SiC Crystals** 3
Noboru Ohtani
- 2 **Industrial Perspectives of SiC Bulk Growth** 33
Adrian R. Powell
- 3 **Homoepitaxial Growth of 4H-SiC on Vicinal Substrates** 47
Birgit Kallinger
- 4 **Industrial Perspective of SiC Epitaxy** 75
Albert A. Burk, Jr., Michael J. O'Loughlin, Denis Tsvetkov, and Scott Ustin
- 5 **Status of 3C-SiC Growth and Device Technology** 93
Peter Wellmann, Michael Schöler, Philipp Schuh, Mike Jennings, Fan Li, Roberta Nipoti, Andrea Severino, Ruggero Anzalone, Fabrizio Roccaforte, Massimo Zimbone, and Francesco La Via
- 6 **Intrinsic and Extrinsic Electrically Active Point Defects in SiC** 137
Ulrike Grossner, Joachim K. Grillenberger, Judith Woerle, Marianne E. Bathen, and Johanna Müting

- 7 Dislocations in 4H-SiC Substrates and Epilayers 169**
Balaji Raghothamachar and Michael Dudley
- 8 Novel Theoretical Approaches for Understanding and Predicting Dislocation Evolution and Propagation 199**
Binh Duong Nguyen and Stefan Sandfeld
- 9 Gate Dielectrics for 4H-SiC Power Switches: Understanding the Structure and Effects of Electrically Active Point Defects at the 4H-SiC/SiO₂ Interface 225**
Gregor Pobegen and Thomas Aichinger
- 10 Epitaxial Graphene on Silicon Carbide as a Tailorable Metal–Semiconductor Interface 249**
Michael Krieger and Heiko B. Weber
- 11 Device Processing Chain and Processing SiC in a Foundry Environment 271**
Arash Salemi, Minseok Kang, Woongje Sung, and Anant K. Agarwal
- 12 Unipolar Device in SiC: Diodes and MOSFETs 319**
Sei-Hyung Ryu
- Volume 2**
- 13 Ultra-High-Voltage SiC Power Device 353**
Yoshiyuki Yonezawa and Koji Nakayama
- 13.1 Introduction 353
- 13.2 Ultra-high-voltage SiC PiN diode and SiC-IGBT 355
- 13.3 Reverse Characteristics of SiC Bipolar Device 356
- 13.3.1 Relationship Between Thickness and Density of Drift Layer and Breakdown Voltage 356
- 13.3.2 Termination Structure of SiC Bipolar Devices 357
- 13.4 Carrier Lifetime Dependence on the Characteristics of Bipolar Device 358
- 13.4.1 Forward Characteristics of pn Diode 360
- 13.4.1.1 Analysis of Characteristics Under Low-Level Injection 360
- 13.4.1.2 Analysis of Carriers in the Drift Layer Under High-Level Injection 362
- 13.4.1.3 Relationship Between Carrier Life, Drift Layer Thickness, and Drift Layer Voltage Drop 363
- 13.4.2 Reverse Characteristics of pn Diode 365

13.4.2.1	Reverse Leakage Current Characteristics	365
13.4.3	Dynamic Characteristics of pn Diode	365
13.4.3.1	Reverse and Forward Recovery of Characteristics	365
13.4.3.2	Open-Circuit Voltage Decay	366
13.4.3.3	Comparison of Reverse and Forward Recovery Characteristics and OCVD	368
13.5	Design and Device Performance of Bipolar Device	370
13.5.1	Carrier lifetime dependence	371
13.5.2	Loss Estimation of Bipolar Device	373
13.6	Current Status of SiC Bipolar Device	377
13.6.1	Device Performance of 16 kV Class SiC-IGBT	378
13.6.2	Device Characteristics of higher-than-20 kV Class SiC-IGBT	382
13.6.3	Other Bipolar Devices Issues	383
	References	384
14	SiC Reliability Aspects	387
	<i>Josef Lutz and Thomas Basler</i>	
14.1	Ruggedness and Overload Events	387
14.1.1	Short-circuit Ruggedness of SiC MOSFETs	387
14.1.2	Surge-current Ruggedness	394
14.1.3	Avalanche Capability	403
14.2	Cosmic-Ray Stability	412
14.3	Thermomechanical Reliability	414
14.3.1	Temperature-sensitive Electrical Parameters	416
14.3.2	Execution of Power-cycling Tests	419
14.3.3	Evaluation of SiC Power-cycling Tests	421
14.4	New Power-module Technologies with Sufficient Reliability	422
14.4.1	Improved Die-attach Technologies	422
14.4.2	Improved Top-Side Interconnections	424
	Acknowledgments	426
	References	426
15	Industrial Systems Using SiC Power Devices	433
	<i>Nando Kaminski</i>	
15.1	Introduction	433
15.1.1	Benefits of SiC Devices	433
15.1.2	Competition by Other Technologies	436
15.2	DC/DC Converters	437
15.3	Solid-State Transformer (SST)	443
15.3.1	Traction	443
15.3.2	Power Grid	444
15.4	Wireless Charging	445

15.5	Inductive Heating	446
15.5.1	Domestic Systems	446
15.5.2	Industrial Systems	446
15.6	Photovoltaic	447
15.6.1	Residential Systems	447
15.6.2	Commercial, Industrial, and Utility Size Systems	449
15.7	DC Grids	451
15.7.1	Low- and Medium-Voltage DC Grids	451
15.7.2	DC Breakers	452
15.8	High-Voltage DC (HVDC)	452
15.8.1	HVDC Transmission	452
15.8.2	HVDC Breakers	454
15.9	Drives	455
15.9.1	Industrial Drives	455
15.9.2	Wind Energy	457
15.9.3	Traction	458
15.10	Conclusions	459
	Acknowledgements	460
	References	460
16	Special Focus on HEV and EV Applications: Activities of Automotive Industries Applying SiC Devices for Automotive Applications	467
	<i>Kimimori Hamada, Keiji Toda, Hiromichi Nakamura, Shigeharu Yamagami, and Kazuhiro Tsuruta</i>	
16.1	Background (PDPlus LLC)	467
16.2	The Challenge of SiC Power Devices Introductions on Prototype HEVs and FCVs (TOYOTA MOTOR CORPORATION)	469
16.2.1	Progress of Electrification	469
16.2.2	Demonstration of Electrified Vehicles	470
16.3	Introduction of Boost Converter Using SiC Semiconductor for New FCV Drive (HONDA MOTOR CO., LTD.)	472
16.3.1	Introduction	472
16.3.2	Configuration of the Electric Power Plant System for New FCV	472
16.3.3	FCVCU	473
16.3.3.1	Circuit Configuration	473
16.3.3.2	Full SiC-IPM	473
16.3.3.3	Magnetic Coupling and Interleave Operation	474
16.3.3.4	Control Methods	475
16.3.3.5	Effects on Smaller Size and Higher Efficiency	477
16.3.3.6	Quietness	478
16.3.3.7	Noise Countermeasures	478

16.3.3.8	Structure of the FCVCU	479
16.3.4	Conclusions	480
16.4	Development of Module Technologies to Bring Out SiC Power Device Performances (TOYOTA MOTOR CORPORATION)	481
16.4.1	Power Card Structure for Double-Side Cooling Technology	481
16.4.2	New Transient Liquid Phase Structure for High-Temperature Applications	481
16.4.3	Ni Micro-Plating Bonding	483
16.5	SiC-MOSFET Switching Characteristics and Gate Driver Circuits for Automotive Application (NISSAN MOTOR CO., LTD.)	485
16.5.1	Introduction	485
16.5.2	Basics of Switching Characteristics	485
16.5.3	Various Gate Driver Circuits	487
16.5.4	Conclusion	489
16.6	R&D of SiC Power Devices for Automotive Applications (DENSO CORPORATION)	489
16.6.1	Introduction	489
16.6.2	Ultra-Low-Loss SiC-MOSFET for Cost Reduction	491
16.6.3	Proposed 4H-SiC Trench MOSFET Structure	491
16.6.4	Characteristics of the Developed MOSFET	494
16.6.4.1	Static Characteristics of the Optimized Structure	494
16.6.4.2	Dynamic Behavior of the Optimized Structure	495
16.6.5	Measurements of Reliability	497
16.6.6	Suppression of Bipolar Degradation in the Presented MOSFETs [30]	497
16.6.7	Summary	500
	Acknowledgments	500
	References	501
17	Point Defects in Silicon Carbide for Quantum Technology	503
	<i>András Csóré and Adam Gali</i>	
17.1	Introduction	503
17.2	Silicon Carbide: Polytypes and Types of Relevant Point Defects	504
17.3	Point Defect Single Photon Sources and Quantum Bits	507
17.3.1	Divacancy	508
17.3.2	Si-vacancy	510
17.3.3	Carbon Antisite-Vacancy Pair	513
17.3.4	Nitrogen-Vacancy Pair	514
17.3.5	Other Defects	515
17.4	Conclusion	517
	Acknowledgments	518
	References	518

Part II Gallium Nitride (GaN), Diamond, and Ga₂O₃ 529

- 18 Ammonothermal and HVPE Bulk Growth of GaN 531**
Robert Kucharski, Tomasz Sochacki, Boleslaw Lucznik, Mikolaj Amilusik, Karolina Grabianska, Malgorzata Iwinska, and Michal Bockowski
- 18.1 Introduction 531
- 18.2 HVPE Method – History and State of the Art 533
- 18.3 Ammonothermal Method – History and State of the Art 536
- 18.4 HVPE-GaN-on-Ammono-GaN – State of the Art 542
- 18.4.1 Bulk Growth – Challenges 543
- 18.4.2 Doping 546
- 18.4.2.1 Doping with Donors 546
- 18.4.2.2 Doping with Acceptors 549
- 18.5 Summary 550
- Acknowledgments 551
- References 551
-
- 19 GaN on Si: Epitaxy and Devices 555**
Hidekazu Umeda
- 19.1 Introduction 555
- 19.2 GaN Epitaxy on Si Substrate 556
- 19.2.1 GaN Epitaxial Method and Doping 556
- 19.2.1.1 Metal–Organic Chemical Vapor Deposition (MOCVD) 556
- 19.2.1.2 N, P-Type Doping 556
- 19.2.1.3 Doping for Semi-insulation Layer 557
- 19.2.2 Substrates for GaN Epitaxy 557
- 19.2.2.1 GaN 557
- 19.2.2.2 Sapphire 558
- 19.2.2.3 SiC 558
- 19.2.2.4 Si 559
- 19.2.3 Epitaxial Growth Technology on Si Substrate 559
- 19.2.3.1 Crystal Orientation of Si Substrate 559
- 19.2.3.2 Nucleation Layer 559
- 19.2.3.3 Buffer Layer 560
- 19.2.3.4 AlGa_N/GaN Active Layer with Polarization Effect 561
- 19.3 Lateral GaN Devices on Si Substrate 564
- 19.3.1 Device Structure and Fabrication Process 564
- 19.3.2 Structures for E-Mode Operation 566
- 19.3.3 E-Mode GaN Gate-Injection Transistor (GIT) on Si Substrate 567
- 19.3.3.1 Device Structure and Operational Principle 567
- 19.3.3.2 DC Performance of GIT 568
- 19.3.3.3 Switching Performance of GIT 570

19.4	Application of GaN HFET	571
19.5	Integration of Lateral GaN Devices	573
19.6	Summary	576
	Acknowledgments	577
	References	577
20	Growth of Single Crystal Diamond Wafers for Future Device Applications	583
	<i>Matthias Schreck</i>	
20.1	Introduction	583
20.2	High-Pressure High-Temperature (HPHT) Synthesis	584
20.2.1	Basic Concepts and Technical Realizations	584
20.2.2	The Temperature Gradient Method	586
20.2.3	Chemical Purity and Classification	587
20.2.4	Morphology and Structural Quality	588
20.2.5	State of the Art in Crystal Size	589
20.2.6	Boron Doping	590
20.3	Chemical Vapor Deposition (CVD)	591
20.3.1	Basic Principles	591
20.3.1.1	The Mechanism of Diamond Growth by CVD	591
20.3.1.2	Gas Mixtures for Diamond CVD	593
20.3.1.3	The Role of Trace Gases	594
20.3.1.4	Experimental Setups	595
20.3.1.5	Growth Rate and Gas Temperature	598
20.3.1.6	Nucleation by Seeding	599
20.3.1.7	Bias-Enhanced Nucleation (BEN)	599
20.3.2	Examples of Polycrystalline CVD Diamond Layers	601
20.3.3	CVD Growth of Single Crystals	602
20.3.4	Homoepitaxy	603
20.3.4.1	Homoepitaxial Growth on Different Crystals Faces	603
20.3.4.2	Single Crystal Seed Recovery	604
20.3.4.3	Size Increase and Mosaic Growth	605
20.3.5	Heteroepitaxy	605
20.3.5.1	Growth Substrates for Heteroepitaxy	605
20.3.5.2	Bias-Enhanced Nucleation on Iridium: Phenomenology and Mechanism	607
20.3.5.3	Structural Improvement with Film Thickness	609
20.3.5.4	Multilayer Substrates for Scaling to Wafer Size	611
20.3.5.5	The State of the Art in Scaling and Mosaic Spread	613
20.3.5.6	Intrinsic Stress and Its Correlation with Dislocations	614
20.3.5.7	Heteroepitaxy on (111)-Oriented Substrates	614
20.3.5.8	The Microneedle Approach	615

- 20.3.6 Advanced Concepts for Structural Improvement 617
- 20.3.6.1 Epitaxial Lateral Overgrowth 617
- 20.3.6.2 Dislocation Stopping by W or Ta Atoms 618
- 20.4 State of the Art and Outlook 619
- Acknowledgments 619
- References 619

21 Diamond Wafer Technology, Epitaxial Growth, and Device Processing 633

Hideaki Yamada, Hiromitsu Kato, Shinya Ohmagari, and Hitoshi Umezawa

- 21.1 Diamond Epitaxial Growth and Wafers 633
- 21.2 n-Type Doping and Processing 638
- 21.3 p-Type Doping and Processing 642
- 21.4 Devices 645
- References 650

22 Gallium Oxide: Material Properties and Devices 659

Masataka Higashiwaki

- 22.1 Introduction 659
- 22.2 Physical Properties of Ga_2O_3 660
 - 22.2.1 Polymorphs 660
 - 22.2.2 Material Properties of $\beta\text{-Ga}_2\text{O}_3$ 660
- 22.3 Melt Bulk Growth 662
- 22.4 Epitaxial Growth 662
 - 22.4.1 MBE 663
 - 22.4.2 HVPE 664
 - 22.4.3 MOCVD 664
 - 22.4.4 Mist CVD 665
- 22.5 Vertical Diodes 665
 - 22.5.1 SBD with HVPE-Grown Drift Layer 665
 - 22.5.2 Field-Plated SBD 666
 - 22.5.3 Field-Plated SBD with Guard Ring Formed by Nitrogen-Ion Implantation 666
 - 22.5.4 Trench SBD 667
 - 22.5.5 $\alpha\text{-Ga}_2\text{O}_3$ SBD 667
 - 22.5.6 Heterojunction p-Amorphous Oxide/n- Ga_2O_3 Diode 668
- 22.6 Lateral FETs 668
 - 22.6.1 MESFET 668
 - 22.6.2 Depletion-Mode MOSFET 669
 - 22.6.3 Field-Plated MOSFET 671
 - 22.6.4 Modulation-Doped FET 671
 - 22.6.5 Normally Off FET 672

22.7	Vertical FETs	672
22.7.1	Current Aperture FET	673
22.7.2	Fin Channel FET	673
22.8	Summary	674
	References	674
	Index	681

Contents

Volume 1

Preface *xiii*

Part I Silicon Carbide (SiC) 1

- 1 Dislocation Formation During Physical Vapor Transport Growth of 4H-SiC Crystals 3**
Noboru Ohtani
 - 1.1 Introduction 3
 - 1.2 Formation of Basal Plane Dislocations During PVT Growth of 4H-SiC Crystals 5
 - 1.2.1 Plan-View X-ray Topography Observations of Growth Front 5
 - 1.2.2 Cross-Sectional X-ray Topography Observations of Growth Front 9
 - 1.2.3 Characteristic BPD Distribution in PVT-Grown 4H-SiC Crystals 13
 - 1.2.4 BPD Multiplication During PVT Growth 15
 - 1.3 Dislocation Formation During Initial Stage of PVT Growth of 4H-SiC Crystals 18
 - 1.3.1 Preparation of 4H-SiC Wafers with Beveled Interface Between Grown Crystal and Seed Crystal 18
 - 1.3.2 Determination of Grown-Crystal/Seed Interface by Raman Microscopy 19
 - 1.3.3 X-ray Topography Observations of Dislocation Structure at Grown-Crystal/Seed Interface 22
 - 1.3.4 Formation Mechanism of BPD Networks and Their Migration into Seed Crystal 23
 - 1.4 Conclusions 28
 - References 30
- 2 Industrial Perspectives of SiC Bulk Growth 33**
Adrian R. Powell
 - 2.1 Introduction 33

2.2	SiC Substrates for GaN LEDs	33
2.3	SiC Substrates for Power SiC Devices	34
2.4	SiC Substrates for High-Frequency Devices	35
2.5	Cost Considerations for Commercial Production of SiC	35
2.6	Raw Materials	36
2.7	Reactor Hot Zone	37
2.8	System Equipment	39
2.9	Yield	39
2.10	Turning Boules into Wafers	41
2.11	Crystal Grind	41
2.12	Wafer Slicing	42
2.13	Wafer Polish	44
2.14	Summary	44
	Acknowledgments	45
	References	45
3	Homoepitaxial Growth of 4H-SiC on Vicinal Substrates	47
	<i>Birgit Kallinger</i>	
3.1	Introduction	47
3.2	Fundamentals of 4H-SiC Homoepitaxy for Power Electronic Devices	47
3.2.1	4H-SiC Polytype Replication for Homoepitaxial Growth on Vicinal Substrates	48
3.2.2	Homoepitaxial Growth by Chemical Vapor Deposition (CVD) Process	52
3.2.3	Doping in Homoepitaxial Growth	53
3.3	Extended Defects in Homoepitaxial Layers	55
3.3.1	Classification of Extended Defects According to Glide Systems in 4H-SiC	56
3.3.2	Dislocation Reactions During Epitaxial Growth	57
3.3.3	Characterization Methods for Extended Defects in 4H-SiC Epilayers	59
3.4	Point Defects and Carrier Lifetime in Epilayers	62
3.4.1	Classification and General Properties of Point Defects in 4H-SiC	62
3.4.2	Basics on Recombination Carrier Lifetime in 4H-SiC	64
3.4.3	Carrier Lifetime-Affecting Point Defects	65
3.4.4	Carrier Lifetime Measurement in Epiwafers and Devices	68
3.5	Conclusion	69
	Acknowledgments	70
	References	70
4	Industrial Perspective of SiC Epitaxy	75
	<i>Albert A. Burk, Jr., Michael J. O'Loughlin, Denis Tsvetkov, and Scott Ustin</i>	
4.1	Introduction	75
4.2	Background	76
4.3	The Basics of SiC Epitaxy	76
4.4	SiC Epi Historical Origins	78
4.5	Planetary Multi-wafer Epitaxial Reactor Design Considerations	80

4.5.1	Rapidly Rotating Reactors	81
4.5.2	Horizontal Hot-Wall Reactors	82
4.6	Latest High-Throughput Epitaxial Reactor Status	82
4.7	Benefits and Challenges for Increasing Growth Rate in all Reactors	86
4.8	Increasing Wafer Diameters, Device Processing Considerations, and Projections	86
4.9	Summary	89
	Acknowledgment	90
	References	90
5	Status of 3C-SiC Growth and Device Technology	93
	<i>Peter Wellmann, Michael Schöler, Philipp Schuh, Mike Jennings, Fan Li, Roberta Nipoti, Andrea Severino, Ruggero Anzalone, Fabrizio Roccaforte, Massimo Zimbone, and Francesco La Via</i>	
5.1	Introduction, Motivation, Short Review on 3C-SiC	93
5.2	Nucleation and Epitaxial Growth of 3C-SC on Si	95
5.2.1	Growth Process	95
5.2.2	Defects	98
5.2.3	Stress	102
5.3	Bulk Growth of 3C-SiC	103
5.3.1	Sublimation Growth of (111)-oriented 3C-SiC on Hexagonal SiC Substrates	104
5.3.2	Sublimation Growth of 3C-SiC on 3C-SiC CVD Seeding Layers	105
5.3.3	Continuous Fast CVD Growth of 3C-SiC on 3C-SiC CVD Seeding Layers	110
5.4	Processing and Testing of 3C-SiC Based Power Electronic Devices	117
5.4.1	Prospects for 3C-SiC Power Electronic Devices	117
5.4.2	3C-SiC Device Processing	117
5.4.3	MOS Processing	118
5.4.4	3C-SiC/SiO ₂ Interface Passivation	120
5.4.5	Surface Morphology Effects on 3C-SiC Thermal Oxidation	121
5.4.6	Thermal Oxidation Temperature Effects for 3C-SiC	122
5.4.7	Ohmic Contact Metalization	123
5.4.8	N-type 3C-SiC Ohmic Contacts	126
5.4.9	Ion Implantation	126
5.5	Summary	127
	Acknowledgements	127
	References	127
6	Intrinsic and Extrinsic Electrically Active Point Defects in SiC	137
	<i>Ulrike Grossner, Joachim K. Grillenberger, Judith Woerle, Marianne E. Bathan, and Johanna Müting</i>	
6.1	Characterization of Electrically Active Defects	141
6.1.1	Deep Level Transient Spectroscopy	141
6.1.1.1	Profile Measurements	143

6.1.1.2	Poole–Frenkel Effect	143
6.1.1.3	Laplace DLTS	143
6.1.2	Low-energy Muon Spin Rotation Spectroscopy	144
6.1.2.1	μ SR and Semiconductors	144
6.1.3	Density Functional Theory	145
6.2	Intrinsic Electrically Active Defects in SiC	146
6.2.1	The Carbon Vacancy, V_C	147
6.2.2	The Silicon Vacancy, V_{Si}	152
6.3	Transition Metal and Other Impurity Levels in SiC	153
6.4	Summary	159
	References	163
7	Dislocations in 4H-SiC Substrates and Epilayers	169
	<i>Balaji Raghathamachar and Michael Dudley</i>	
7.1	Introduction	169
7.2	Dislocations in Bulk 4H-SiC	170
7.2.1	Micropipes (MPs) and Closed-core Threading Screw Dislocations (TSDs)	170
7.2.2	Basal Plane Dislocations (BPDs)	171
7.2.3	Threading Edge Dislocations (TEDs)	171
7.2.4	Interaction between BPDs and TEDs	171
7.2.4.1	Hopping Frank–Read Source of BPDs	171
7.2.5	Threading Mixed Dislocations (TMDs) in 4H-SiC	173
7.2.5.1	Reaction Between Threading Dislocations with Burgers Vectors of $-c + a$ and $c + a$ Wherein the Opposite c -Components Annihilate Leaving Behind the Two a -Components	174
7.2.5.2	Reaction Between Threading Dislocations with Burgers Vectors of $-c$ and $c + a$ Leaving Behind the a -Component	175
7.2.5.3	Reaction Between Opposite-sign Threading Screw Dislocations with Burgers Vectors c and $-c$	175
7.2.5.4	Nucleation of Opposite Pair of $c + a$ Dislocations and Their Deflection	175
7.2.5.5	Deflection of Threading $c + a$, c and Creation of Stacking Faults	177
7.2.6	Prismatic Slip during PVT growth 4H-SiC Boules	180
7.2.7	Relationship Between Local Basal Plane Bending and Basal Plane Dislocations in PVT-grown 4H-SiC Substrate Wafers	181
7.2.8	Investigation of Dislocation Behavior at the Early Stage of PVT-grown 4H-SiC Crystals	181
7.3	Dislocations in Homoepitaxial 4H-SiC	184
7.3.1	Conversion of BPDs into TEDs	184
7.3.2	Susceptibility of Basal Plane Dislocations to the Recombination-Enhanced Dislocation Glide in 4H Silicon Carbide	184
7.3.3	Nucleation of TEDs, BPDs, and TSDs at Substrate Surface Damage	188
7.3.4	Nucleation Mechanism of Dislocation Half-Loop Arrays in 4H-SiC Homo-Epitaxial Layers	191

7.3.5	V- and Y-shaped Frank-type Stacking Faults	192
7.4	Summary	192
	Acknowledgments	195
	References	195
8	Novel Theoretical Approaches for Understanding and Predicting Dislocation Evolution and Propagation	199
	<i>Binh Duong Nguyen and Stefan Sandfeld</i>	
8.1	Introduction	199
8.2	General Modeling and Simulation Approaches	200
8.3	Continuum Dislocation Modeling Approaches	201
8.3.1	Alexander–Haasen Model	201
8.3.2	Continuum Dislocation Dynamics Models	202
8.3.2.1	The Simplest Model: Straight Parallel Dislocation with the Same Line Direction	203
8.3.2.2	The “Groma” Model: Straight Parallel Dislocations with Two Line Directions	203
8.3.2.3	The Kröner–Nye Model for Geometrically Necessary Dislocations	204
8.3.2.4	Three-dimensional Continuum Dislocation Dynamics (CDD)	204
8.4	Example 1: Comparison of the Alexander–Haasen and the Groma Model	206
8.4.1	Governing Equations	206
8.4.2	Physical System and Model Setup	206
8.4.3	Results and Discussion	209
8.5	Example 2: Dislocation Flow Between Veins	211
8.5.1	A Brief Introduction to Dislocation Patterning and the Similitude Principle	211
8.5.2	Physical System and Model Setup	213
8.5.3	Geometry and Initial Values	214
8.5.4	Results and Discussion	215
8.6	Summary and Conclusion	219
	References	220
9	Gate Dielectrics for 4H-SiC Power Switches: Understanding the Structure and Effects of Electrically Active Point Defects at the 4H-SiC/SiO₂ Interface	225
	<i>Gregor Pobegen and Thomas Aichinger</i>	
9.1	Introduction	225
9.2	Electrical Impact of Traps on MOSFET Characteristics	225
9.2.1	Sub threshold Sweep Hysteresis	226
9.2.2	Preconditioning Measurement	231
9.2.3	Bias Temperature Instability	233
9.2.4	Reduced Channel Electron Mobility	235
9.3	Microscopic Nature of Electrically Active Traps Near the Interface	237
9.3.1	The P _{bc} Defect and the Subthreshold Sweep Hysteresis	237

- 9.3.2 The Intrinsic Electron Trap and the Reduced MOSFET Mobility 238
- 9.3.3 Point Defect Candidates for BTI 240
- 9.4 Conclusions and Outlook 242
- References 243

10 Epitaxial Graphene on Silicon Carbide as a Tailorable Metal–Semiconductor Interface 249

Michael Krieger and Heiko B. Weber

- 10.1 Introduction 249
- 10.2 Epitaxial Graphene as a Metal 249
- 10.3 Fabrication and Structuring of Epitaxial Graphene 250
 - 10.3.1 Epitaxial Growth by Thermal Decomposition 250
 - 10.3.2 Intercalation 251
 - 10.3.3 Structuring of Epitaxial Graphene Layers and Partial Intercalation 252
- 10.4 Epitaxial Graphene as Tailorable Metal/Semiconductor Contact 253
 - 10.4.1 Ohmic Contacts 254
 - 10.4.2 Schottky Contacts 256
- 10.5 Monolithic Epitaxial Graphene Electronic Devices and Circuits 257
 - 10.5.1 Discrete Epitaxial Graphene Devices 257
 - 10.5.2 Monolithic Integrated Circuits 259
- 10.6 Novel Experiments on Light–Matter Interaction Enabled by Epitaxial Graphene 260
 - 10.6.1 High-Frequency Operation and Ultimate Speed Limits of Schottky Diodes 260
 - 10.6.2 Transparent Electrical Access to SiC for Novel Quantum Technology Applications 263
- 10.7 Conclusion 264
- Acknowledgments 265
- References 265

11 Device Processing Chain and Processing SiC in a Foundry Environment 271

Arash Salemi, Minseok Kang, Woongje Sung, and Anant K. Agarwal

- 11.1 Introduction 271
- 11.2 DMOSFET Structure 271
- 11.3 Process Integration of SiC MOSFETs 273
 - 11.3.1 Lithography 283
 - 11.3.2 SiC Etching 283
 - 11.3.3 Ion Implantation and Activation Annealing 290
 - 11.3.4 Oxidation and Oxide 293
 - 11.3.5 Post Oxidation Annealing 296
 - 11.3.6 Poly-Si Deposition 298
 - 11.3.7 Backside Thinning and Waffle Substrates 300
 - 11.3.8 Ohmic Contacts and Metallization 301
 - 11.3.9 Polyimide Deposition 302

- 11.4 Commercial Foundries for Si and SiC Devices 303
 - 11.4.1 Cost Model 303
 - 11.4.1.1 Cost Roadmap for WBG Devices 303
 - 11.4.2 New Equipment and Processing Requirements 305
- 11.5 Dedicated Foundries vs. Commercial Foundries 306
 - References 307

12 Unipolar Device in SiC: Diodes and MOSFETs 319

Sei-Hyung Ryu

- 12.1 Introduction 319
- 12.2 Unipolar Diodes – 4H-SiC JBS Diodes 320
 - 12.2.1 Optimization of 4H-SiC JBS Diodes 323
 - 12.2.1.1 Injection from the p⁺ Regions for Surge Operation 324
 - 12.2.1.2 Trench JBS Diodes 326
 - 12.2.1.3 Use of Low Work Function Metal for Anode Metal 327
- 12.3 Unipolar Switches: Power MOSFETs 329
 - 12.3.1 4H-SiC Power MOSFET Structures 332
 - 12.3.1.1 DMOSFETs 332
 - 12.3.1.2 Trench MOSFETs 337
 - 12.3.2 Advanced Power MOSFET Structures in 4H-SiC 342
 - 12.3.2.1 Superjunction MOSFETs in 4H-SiC 342
 - 12.3.2.2 Integrated JBS Diodes in 4H-SiC Power MOSFETs 345
- 12.4 Summary 346
 - References 348

Volume 2

13 Ultra-High-Voltage SiC Power Device 353

Yoshiyuki Yonezawa and Koji Nakayama

14 SiC Reliability Aspects 387

Josef Lutz and Thomas Basler

15 Industrial Systems Using SiC Power Devices 433

Nando Kaminski

16 Special Focus on HEV and EV Applications: Activities of Automotive Industries Applying SiC Devices for Automotive Applications 467

Kimimori Hamada, Keiji Toda, Hiromichi Nakamura, Shigeharu Yamagami, and Kazuhiro Tsuruta

17 Point Defects in Silicon Carbide for Quantum Technology 503

András Csóré and Adam Gali

Part II Gallium Nitride (GaN), Diamond, and Ga₂O₃ 529

- 18 Ammonothermal and HVPE Bulk Growth of GaN 531**
Robert Kucharski, Tomasz Sochacki, Boleslaw Lucznik, Mikolaj Amilusik, Karolina Grabianska, Malgorzata Iwinska, and Michal Bockowski
- 19 GaN on Si: Epitaxy and Devices 555**
Hidekazu Umeda
- 20 Growth of Single Crystal Diamond Wafers for Future Device Applications 583**
Matthias Schreck
- 21 Diamond Wafer Technology, Epitaxial Growth, and Device Processing 633**
Hideaki Yamada, Hiromitsu Kato, Shinya Ohmagari, and Hitoshi Umezawa
- 22 Gallium Oxide: Material Properties and Devices 659**
Masataka Higashiwaki
- Index 681**