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Packaging and Test of Photonic Integrated Circuits (PICs)

Stéphane Bernabé[1], Tolga Tekin[2], Bogdan Sirbu[2], Jean Charbonnier[4], Philippe Grosse[1], and Moritz Seyfried[3]

[1] Université Grenoble Alpes, Photonics Division, CEA LETI, Minatec Campus, 17, rue des martyrs, F38054 Grenoble, France
[2] Fraunhofer IZM, Photonic and Plasmonic Systems, Gustav-Meyer-Allee 25, 13355 Berlin, Germany
[3] ficonTEC Service GmbH, Research and Development, Rehland 8, 28832 Achim, Germany
[4] Université Grenoble Alpes, Silicon Devices Division, CEA LETI, Minatec Campus, 17, rue des martyrs, F38054 Grenoble, France

> *The chief commercial advantage of the PIC is in its reduction in the number of component coupling and packaging steps. The result is greater reliability, lower cost and power, and smaller size.*
>
> Ivan P. Kaminow (2008)

1.1 Introduction

Compared to semiconductor electronic integrated circuits (EIC), packaging and testing of photonic integrated circuits (PIC) require specific methods and processes. It is due to the particularity of their optical I/Os and in some cases the thermal sensitivity of integrated photonic functions. These constraints prevented industrial processes to reach the same cost breakdown as electronic ICs: today, the major part (up to 80%) of a photonic module cost still lies in packaging and test operations, not in the circuit itself. As explained previously in this book, various technologies exist to fabricate PICs, using various types of materials and structures, with few standards or roadmap relating to packaging and testing.

PIC integration into a module follows an assembly sequence which includes wafer-level test, chip dicing, coupling of optical I/Os to an optical fiber or a laser diode, electrical interconnect to an EIC, and finally the PIC integration into a package or onto a module board. These main steps will be examined in this chapter, reviewing also the main challenges, guidelines, and technologies required by next-generation photonic modules, such as photonic chiplets or photonic interposers.

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1.2 Challenges and Specificities of PIC Packaging and Test

Integration of PICs into a module, embedded in a system (e.g. a switch unit in a 1U blade used in a datacenter rack) requires several specific steps, which will contribute to the final module cost. The final packaged device has to meet the application specifications in terms of operating temperature and environmental standards (e.g. Telcordia GR-468-CORE: Generic Requirements for Optoelectronic Devices Used in Telecommunications Equipment). Figure 1.1 shows a typical assembly flow, involving a silicon photonics-based circuit to achieve a high data rate (e.g. 400 Gbps) datacom transceiver module for intra data center interconnects.

This typical assembly flow is shared by most of PIC-based modules, with slight variations depending on the targeted application and performances. For example, for data rates of 25 Gbps per channel and above, photoreceivers may require high bandwidth transimpedance amplifiers (TIA) add-ons, flip-chipped onto Photonic chips [1] using copper pillar interconnects to lower parasitics and shorten wire length. Figure 1.2 shows the motherboard of a previously released 40 Gbps datacom silicon photonics-based transceiver from Luxtera (10 Gbps per channel).

As well as for semiconductor devices, PICs packaging and testing are mainly driven by interconnects management. Interconnects achieve the PIC connection to the motherboard, sometimes through an intermediate printed circuit board or package (e.g. BGA laminate, or ceramic package). Quite obviously, by contrast to EICs, two types of PICs interconnects can be distinguished:

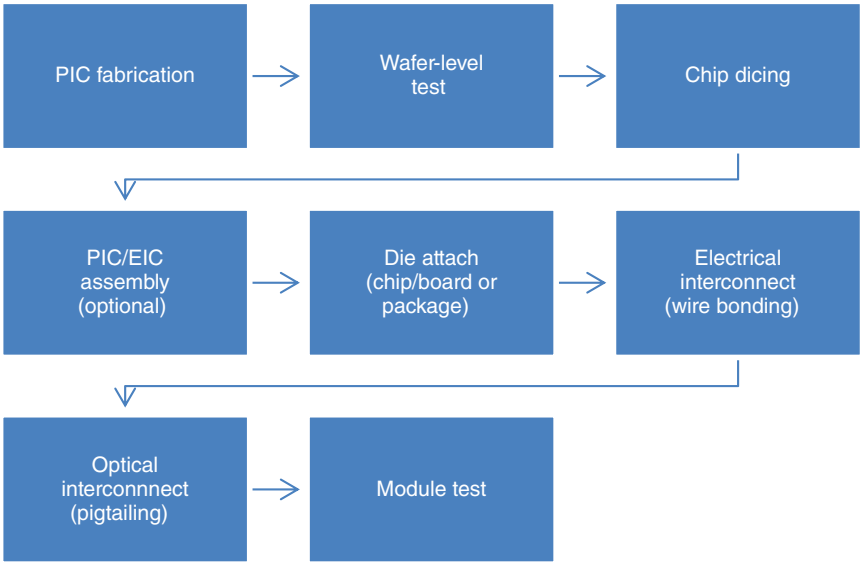


Figure 1.1 Typical assembly flow for the packaging of a silicon photonics PIC into a datacom transceiver module.

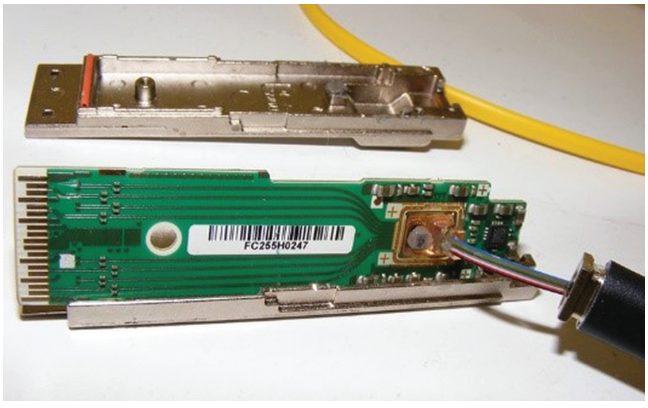


Figure 1.2 Typical content of a silicon photonics module (with QSFP chassis). Source: C. Kopp, CEA-Leti.

- **Optical interconnects**, allowing the connectivity of the PICs integrated optical waveguides to an external waveguide, for example, an optical fiber, with a maximized transmitted optical power. Optical coupling may be the most discussed obstacle to achieve low-cost photonics. By contrast to laser diode packaging, optical coupling of PICs generally involves multiple optical channels, leading to the use of fiber ribbons or multicore fibers (MCF). Fibers are thus mounted into glass V-groove fiber arrays (FA) to be handled during test or packaging processes.
- **Electrical interconnects**, which may be an RF line allowing the proper transmission of a high data rate modulated electrical signal to or from an integrated active photonic device (e.g. phase modulator, photodiode).

1.2.1 Optical Interconnects

From the earliest demonstration of planar waveguide circuits, the challenge of low loss, high yield connection to an optical fiber, or another external waveguide (e.g. a III–V laser) has been identified as a key challenge to allow further adoption of the PIC technology at an industrial level. These challenges are fairly independent on the PIC fabrication technology (lithium niobate oxide, doped glass, silicon photonics, polymer), especially when single-mode waveguides are considered [2–4]. In this chapter, we will focus on single-mode waveguides, which can be found in many application fields, especially in the long-range telecommunications, data center high-speed interconnects, and may compete with VCSEL links for short reach interconnects such as CPU to memory in the near future.

The main parameter that has to be optimized for efficient optical interface – actually, by targeting the lowest possible value – is the coupling loss (CL). It is related to the linear coupling efficiency η, which is the ratio between the coupled optical power into the external waveguide (P_1) and the available optical power at the output of the PIC optical port (P_0), by Eq. (1.1)

$$\mathrm{CL\ (dB)} = -10 \log \eta = -10\ \log \frac{P_1}{P_0} \tag{1.1}$$

This CL is a positive value and it is typically wavelength dependent. Some authors use the logarithmic coupling efficiency $CE = 10\log(\eta)$, which is negative. Additional to the CL, some applications require the amount of reflected power to the input waveguide to be minimized. This results in reducing the corresponding return loss (RL), defined as $RL = -10\log(P_r/P_0)$, where P_r denotes the reflected optical power.

Analytical expression of the CL can be obtained by using Kolgelnik's electromagnetic theory of laser beams. In the case of single-mode waveguides, the coupling efficiency is obtained by calculating the overlap integral between the respective field amplitudes of the fundamental modes E_0 and E_1 related to the PIC and the external waveguide (secondary waveguide) (Eq. (1.2)), in a reference plane (x, y) orthogonal to the z optical axis

$$\eta = \frac{\left|\iint E_0(x,y)\cdot E_1^*(x,y)\,\mathrm{d}x\,\mathrm{d}y\right|^2}{\iint |E_0(x,y)|^2\mathrm{d}x\,\mathrm{d}y\cdot\iint |E_1(x,y)|^2\mathrm{d}x\,\mathrm{d}y} \tag{1.2}$$

References [5–9] provide expressions of η, in the case the output beam from the PIC can be approximated by a Gaussian beam with a waist denoted ω. This approximation is valid for most of the optical waveguide obtained by microtechnologies fabrication processes.

Several cases can be distinguished here. The simplest coupling scenario that could be considered is **butt coupling**, with no gap between the two waveguides. In this case, E_0 is the amplitude of the field at the output of the PIC, and E_1 is the amplitude of the external waveguide's field. Another possible configuration is the case of **lens-assisted coupling**: one or several lenses are inserted between the PIC and the external waveguide, allowing beam refocusing of the PIC's beam to the external waveguide input plane. The same Eq. (1.2) should be used, considering E_0 as the field obtained by propagating the PIC's output beam through the optical system, overlapping with the external waveguide at the entrance plane of the latter.

In the case of a perfect alignment of the waveguide's axis, Eq. (1.2) can be solved analytically, considering the respective beam's waists radii ω_0 and ω_1 (Eq. (1.3)), in the axes x and y, respectively.

$$\eta = \frac{4}{\left(\frac{\omega_{0x}}{\omega_{1x}} + \frac{\omega_{1x}}{\omega_{0x}}\right)\left(\frac{\omega_{0y}}{\omega_{1y}} + \frac{\omega_{1y}}{\omega_{0y}}\right)} \tag{1.3}$$

From this equation, the **mode-matching condition** can be determined: the maximum coupling (i.e. minimum CL) is obtained for $\omega_{0x} = \omega_{1x}$ and $\omega_{1y} = \omega_{1y}$. Whether the considered external waveguide is a laser diode, an optical fiber, or another PIC, an optimum packaging or probe test of a given PIC will target a minimum CL by achieving this condition.

In addition, an analytical expression of η can also be obtained in the case of optical axis misalignment (caused by an offset or a tilt): this leads to the knowledge of the **alignment tolerances** of the system, which is a key parameter to be considered at the packaging or the test level. A convenient way to evaluate alignment tolerance is to calculate the misalignment (tilt or offset) resulting in a 1 dB excess CL (called

"1 dB tolerance"). For lateral misalignment of circular beams (perpendicularly to the optical z-axis) the 1 dB tolerance is given by Eq. (1.4) [10], with waists expressed in micrometers.

$$\eta_{(1\text{ dB})} = 0.33\sqrt{\left(\omega_0^2 + \omega_1^2\right)} \tag{1.4}$$

Depending on the PIC fabrication technology and the nature of the optical waveguide, it may be not possible to reach the mode-matching condition. Knowing the waist parameters will however enable to calculate optimum coupling and alignment tolerances by solving the analytical equations or by simulating coupling by using dedicated software (beam propagation modeling or physical optical propagation module from optical design softwares).

1.2.2 Coupling Structures

Coupling structures are PIC features enabling the light extraction/injection from/into the PIC, possibly including some spot size converter (SSC) function to achieve the mode-matching condition when connection to an optical fiber or another external waveguide is needed. Indeed, in many cases, the used integrated waveguide exhibit mode waists much smaller compared to the waist of the external waveguide due to the use of high index material for the photonic waveguide (e.g. Si or InP) – in the case of silicon photonics, it can be submicrometric. The most critical configuration is for pigtailing (coupling to a single-mode optical fiber) as the fiber's waist (aka mode field radius or MFR) of a standard single-mode fiber (SMF) is typically about 5 μm in the telecommunication wavelength range.

One can distinguish between three types of coupling structures [11–13]. Depending on the used configuration, mode-matching condition (and thus minimum CL), operating wavelength range, polarization-dependent loss (PDL), misalignment tolerance, and manufacturing scalability may be different.

1.2.2.1 Edge Coupler

This kind of structure enables lateral (in plane) direct coupling to an optical fiber or a laser diode by locally modifying the beam waist of the guided mode at the proximity of the PIC facet, if required. It is a broad wavelength solution, with low PDL (<1 dB). Several edge couplers are reported in literature, depending on the waveguide technology. Waveguides with large cross sections (approx. 10×10 μm) exhibit large waists and can be directly coupled to a SMF by dicing and polishing the chip facet. For SiN, InP, or thick SOI waveguides, simple edge coupling without any spot size conversion leads to the use of lensed fiber to achieve the mode-matching condition (waists are typically in the 1–3 μm range). For silicon photonics relying on thin SOI (typically 220 nm thick), SSC is required to achieve waists compatible with commercialy available lensed or flat cleaved fibers.

Spot size conversion is obtained by:

- gradually increasing the physical size of the waveguide (**3D adiabatic taper**) along light propagation axis (z-axis).

- using **inverted tapers**, gradually reducing the lateral waveguide size in the *z*-axis, down to the minimum possible size at the tip (defined by the used lithographic node), resulting in a decrease of the effective index and thus a less confined mode.
- use of **metamaterial structures** exhibiting low effective index.
- adiabatically transferring of the optical power to a **super waveguide** made of another material of lower index (e.g. silicon nitride on the top of a tapered silicon waveguide).

All these different structures (Figure 1.3) provide beam enlargement, with alignment tolerances directly related to the beam size; however, a suitable surface quality of the facet requires polishing at the die level (after dicing or cleaving) or a final etching process step performed at the wafer level. In any case, wafer-level test remains challenging.

1.2.2.2 Vertical Grating Coupler (VGC)

Vertical grating coupler (VGC) relies on diffractive elements integrated at the end of a PIC waveguide (Figure 1.4), deflecting the propagating beam out of plane, at nearly 90° (current designs target 82°), while intrinsically converting the beam size. This feature is very popular in silicon photonics-based circuits, as the high

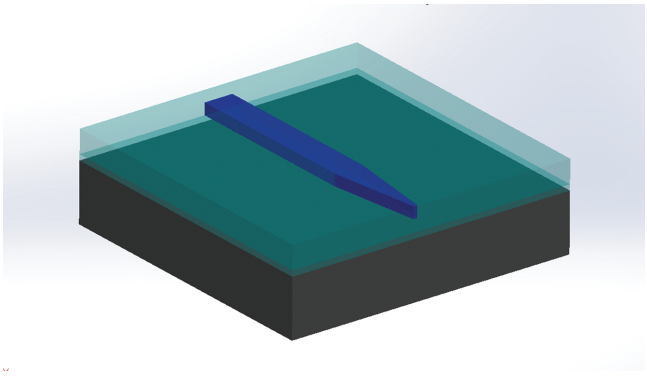


Figure 1.3 Edge coupling structure obtained by inverted taper design. Source : S. Bernabé, CEA-Leti.

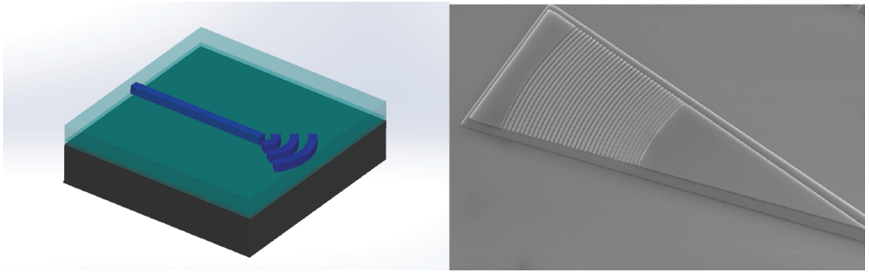


Figure 1.4 Scheme and SEM view of a single polarization grating coupler (SPGC). Source: S. Bernabé, CEA-Leti.

index contrast of silicon waveguide core to silica cladding allows high diffraction efficiency of periodical or quasi-periodical gratings. VGC enables mode matching with SMF, making wafer-level test and multifiber packaging much more convenient compared to edge couplers. Additionally, VGCs can be placed at any location on the PIC surface, and do not require any post-process such as polishing or cleaving. VGC exhibits limited bandwidth (<30 nm) and polarization dependency which can be improved to <0.5 dB by designing two-dimensional structures, sometimes referred to as 2D-VGC. These structures, close to photonic crystals arrays, act as polarization splitters/combiners, with typical CL of 3.5 dB [12].

Arrays of VGC can also be used to enable coupling to a multi core fiber (MCF).

1.2.2.3 Evanescent Coupling

This approach, which allows efficient wavelength-dependent coupling between two adiabatically tapered waveguides (Figure 1.5), has been basically used to perform rough testing of earlier generations of waveguide. It relies on the evanescent coupling in a region where the two deconfined modes overlap.

Through optimization of tapered designs, it is now possible to use it to achieve efficient coupling from a buried waveguide in the PIC to an external waveguide positioned above it, at an optimum distance. This external waveguide can be embedded in a flex substrate, or be a polished or tapered fiber. This configuration typically exhibits large (>50 nm) 1 dB tolerance along the waveguide optical axis (z-axis), and is intrinsically broadband in terms of spectral bandwidth [11].

1.2.3 Wafer-level Test

In the past years, wafer-level test strategies have been developed to test PICs with similar processes as for semiconductor chips. Particularly, wafer-level test aims at enabling a deep range of measurements and tests at the end of the chip fabrication process, allowing a screening of the fabricated chips and identification of known good dies (KGD) before the packaging steps. Here also, the specificity of PICs in terms of optical I/Os prevents from directly applying test techniques developed for microelectronics circuits – i.e. probe tester-based wafer-level test. These well-known test methods need to be slightly adapted, depending on the type of used coupling structures and the complexity of electro-optical (E/O) tests to be performed.

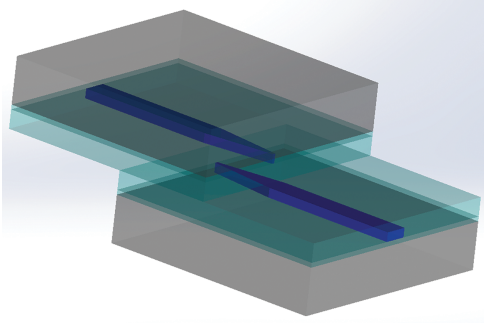


Figure 1.5 Evanescent coupling between two PICs with adiabatic couplers. Source: S. Bernabé, CEA-Leti.

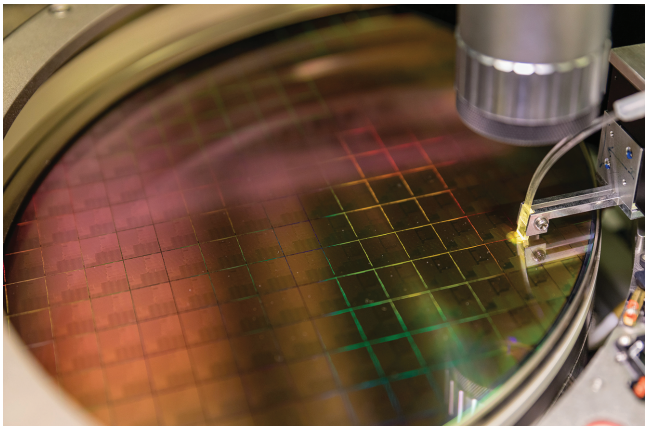


Figure 1.6 Optical on-wafer test of silicon photonics PICs using a V-groove fiber array. The wafer is hold on the prober chuck using vaccum. Source: P. Jayet, CEA-Leti.

Using VGC as coupling structure is the most common case for silicon photonics PICs. In this configuration, it is possible to adapt standard electrical probe testers by adding optical probes, i.e. bare optical fiber or FA (fiber array) to launch or collect the light to or from the PIC (Figure 1.6). This allows the test of existing test structures embedded in the PIC, or to directly test some functionalities of the circuit itself, at the wafer level, before dicing.

The accuracy of the positioning system needs to be higher than that for a pure electronic test station. 1 µm accuracy over a 300 mm wafer instead of 5 µm is needed to guarantee the accurate positioning of a standard SMF on the top of a grating coupler. As a result, relying on the movement of the wafer vs. chuck only is not sufficient, and the optical probe has to be moved accurately too, by attaching it to a high-resolution (10 nm) multi-axis micro positioning system, e.g. a piezoelectric actuator. Practically, the test sequence will use both the displacement of the chuck to switch from a PIC to the following; however, for each PIC, a realignment of the fiber probe to the optical port is needed, through the additional micro-positioning system. The alignment sequence typically starts with the 2D scan of the beam profile out of the PIC, followed by a Gaussian fit, which allows to determine the position for optimum coupling efficiency. Piezoelectric microactuators may be controlled by a driver which is able to simultaneously control the moves and acquire synchronously an electrical signal proportional to the coupled power. This signal can also be used to maintain the coupling in real time, thanks to an additional digital signal processor (DSP) unit using dedicated algorithm [14, 15].

Using FAs exhibits several advantages: scalability (simultaneous handle and test using typically 8 fibers, potentially up to 128), robustness, lower sensitivity to vibrations, and possibility an efficient use of polarization-maintaining fibers. However, an additional degree of freedom in rotation is needed. In this case, two fibers have to be aligned on two optical ports, requiring a rotation adjustment. In addition, an accurate control of the parallelism of the fiber array toward the PIC surface may require

one or two additional rotation degrees of freedom, making six axis positioning system (e.g. hexapod) the best solution for such configurations.

Until recently, applying the above approach to edge coupling structures was a challenge, as the edge emission requires the PIC to be diced first before any optical test, forbidding wafer-level test. Solutions have been developed to enable the use of wafer probe testers relying on optical probes embedding reflectors [16]. This requires front-side cavities to be processed during the PIC fabrication process, at the tip of the fiber coupler structure. This cavity has to be large enough to allow the insertion of a beveled probe to be inserted (Figure 1.7), typically 200 µm wide and 150 µm deep. This probe can be a glass waveguide array with a 45° reflector at the end, for example, a waveguide array to fiber transposer (WAFT) interface from Teem Photonics. This transposer array acts simultaneously as a reflector, a spot size convertor, and a pitch convertor to test dense waveguide arrays and connect them to standard 250 µm pitch fiber ribbons. Using this technique, measurement range >60 dB has been demonstrated.

Additional to the mechanical challenges described in this section, efficient electro-optic measurements also require some modification of standard test and measurement systems. Indeed, in addition to electrical measurement devices, optical measurements have to be performed, particularly spectrum acquisition. This is achieved by using a tunable laser source at the input of the device under test (DUT) and a wideband photodetector at the output. The overall characterization time of a typical step-by-step measurement can be reduced by the use of a triggered sweeped approach, which can drastically reduce the acquisition time. In this configuration, a tunable laser source sweeps freely in a determined wavelength range. A wavelength meter (usually a fiber interferometer) delivers a signal used to trigger an optical meter acquisition and record data in a buffer. The data are recovered only at the end of the laser sweep. Using this setup, it is possible to obtain spectra with a 1 p.m. resolution and 100 nm bandwidth within 10 seconds. Optical measurement can be combined to any electrical test to perform E/O measurement, e.g. response of a photodiode vs. input wavelength, DC phase shifter transmission, or even RF characteristics of an electro-optic modulator by applying RF signals employing RF probes connected to a vector network analyzer (VNA), simultaneously measuring the modulated optical signal (Figure 1.8).

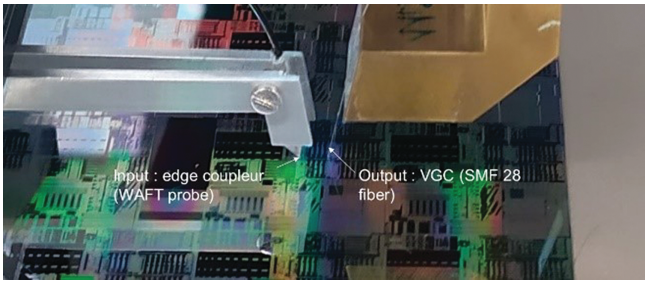
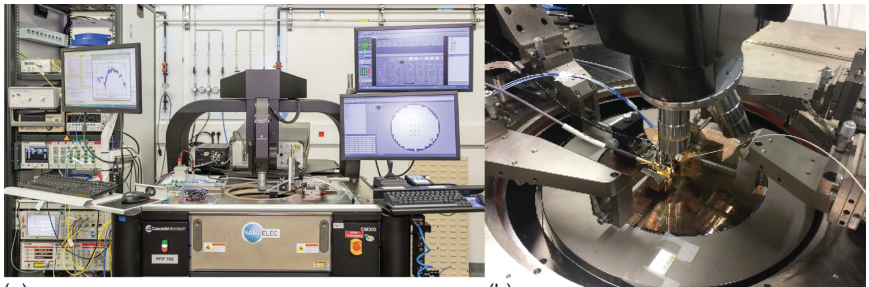


Figure 1.7 Wafer-level test of PICs with edge couplers using reflective glass probes. Source : S. Bernabé, CEA-Leti.



(a) (b)

Figure 1.8 Automated probe tester with dedicated test and measurement instrument for electro-optical test (a) and close view of a PIC under simultaneous RF + optical test (b). Source: P. Grosse, CEA-Leti.

1.2.4 Module Packaging

Wafer-level test, described in the previous section, enables a KGD approach, by picking the chips meeting the targeted specifications for further module integration. The next assembly step generally consists in dicing then die attach and electrical interconnect to a board. The related challenges of electrical-optical integration, thermal management, and mechanical stability of the package, when so many different materials are involved, are also significant design considerations [17].

The design of an integrated photonics package is an iterative process. The typical design steps after the PIC is already designed are the following: first of all the material to work with should be selected, then the thermomechanical aspects should be taken into consideration, and lastly, the RF behavior of the package should be optimized. Depending on the target application using the PIC, some packages might require to comply with a certain standardization form factor, it might need to be hermetical or it might be used for high-power applications, requiring a certain mechanism to dissipate the heat form the package. Therefore, material selection is crucial in the package design and is fully linked to the application. To ensure the reliability of the packages, the thermomechanical design is fundamental. Figure 1.9 shows an example of such thermomechanical simulation environment, where a high-speed PIC package has been modeled employing a commercially available software.

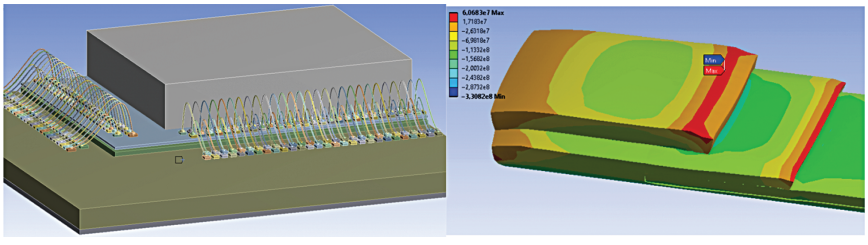


Figure 1.9 FEM thermomechanical simulation model of a wire-bond-based PIC package module with the typical material deformation maps due to mechanical stress and/or heat within the package. Source: B. Sirbu/Fraunhofer IZM.

The typical aspects to be considered for the mechanical design step are among others the characteristics of the components, which kind of assembly process and which materials are going to be used during the assembly process, and of course the thermal constraints of the package. The thermal aspect is particularly important when it comes to the PIC packaging as many of the employed building blocks on the PICs such as lasers and ring resonators are extremely sensitive to any kind of thermal cross talks resulting in an unwanted functionality of the designed PIC. Moreover, thermal instabilities can turn into mechanical stresses due to the coefficient of thermal expansion (CTE) differences of the materials that eventually can affect the functionality and integrity of the package. Therefore this aspect cannot be neglected during the package design. Thermal stability of the PIC packages is typically done employing thermoelectric coolers (TEC) and thermistors.

The final aspect which should be taken into consideration in the successive package design iterations is the RF behavior. Figure 1.10 shows an example of a simulation model used to optimize the RF characteristics of a PIC package involving several parts which have to work together such as the PCB design, Si/Glass interposer where the PIC is assembled and the wire-bonds or bumps interconnecting the interposer to the PCB.

Packaging design rules (PDR) are extremely important in this case, since they are dictating the package specifications with eventual channel limitations, pitch

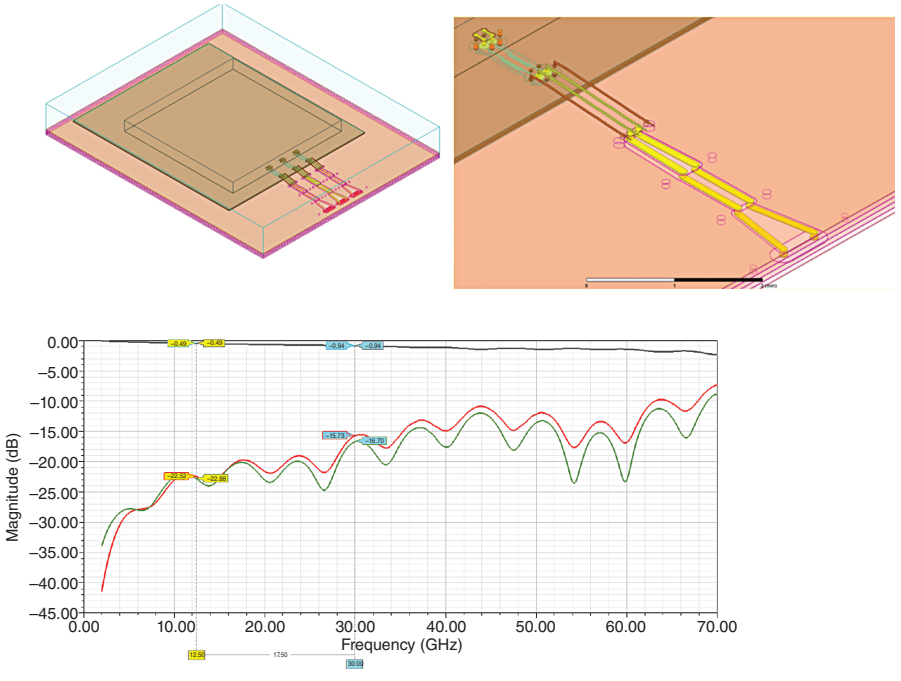


Figure 1.10 HF simulation model of a PIC package with the typical S-parameter curves of the HF traces on the package (involving transmission lines on PCB, Si Interposer, and wire-bonds). Source: B. Sirbu/Fraunhofer IZM.

between the electrical lines, maximum I/O counts, or the impedance of the connectors on the package. Electrical interfaces are necessary for optoelectronic components, for power distribution, and data signal transmission. For HF applications, the electrical interfaces have to comply with some dynamic characteristics such as propagation delay, attenuation, noise, crosstalk, and the rise and fall times to ensure the signal integrity requirements of the package. For this purpose, the impedance-matched transmission lines are crucial to minimize reflections and propagation losses. Additionally, the power integrity aspects for the supporting ASICs shall be considered with respect to co-packaging.

As it can be seen, satisfying all the electrical, optical, and thermomechanical design considerations of integrated photonic devices requires a holistic approach to photonic packaging. The expected performances of the designed modules will have to be confirmed through testing: first, the separate modules are normally individually characterized to confirm their expected behavior, and finally, the entire package is characterized once all assembly steps are finalized.

1.2.5 Fiber Optic Assembly (Pigtailing)

Fiber optic assembly, commonly known as pigtailing, is generally relying on an active alignment of the external waveguide to the PIC, using an accurate six-axis positioning system, and by monitoring the coupled power – just as during the wafer-level test step. However, once the maximum optical power is reached, the optimum position has to be permanently frozen. This is done either by using UV-curing adhesives or laser welding. Several categories of optical assemblies have to be distinguished though [18].

1.2.5.1 PIC Alignment to a Lensed Fiber

This method is used in the edge coupling configuration (Figure 1.11), where the PIC I/O characteristic mode size (waist) is not matching a standard SMF MFR, due to limitation of the PIC waveguide fabrication technology (e.g. InP-based PICs). To ensure mode matching, a high numerical aperture fiber is needed, which can be a lensed fiber. Several technologies can be used to obtain such a fiber: laser machined lensing, chemical etching, fiber tapering using thermal processes, or Gradissimo structure, achieving a focusing lens at the tip of the fiber by splicing a short rod of graded index fiber. Coupling losses (CLs) around 1 dB with 3 dB spectral bandwidth of several hundreds of nanometers have been reported [19]; however, the value is highly dependent on the mode matching to the lensed fiber.

1.2.5.2 PIC Butt Coupling to a Standard Cleaved Single-mode Fiber

This method is quite popular when the mode-matching condition is reached. It is the case by using VGCs at the optical I/O of a silicon photonics PIC, or edge coupler at the optical I/O of PICs made from technologies allowing wide spot sizes (c. 10 μm) at the output (e.g. glass waveguide based circuit, lithium niobate circuit, thick SOI). This method is widely used in commercial products, especially parallel optics modules requiring a fiber ribbon to be assembled in a single step, using

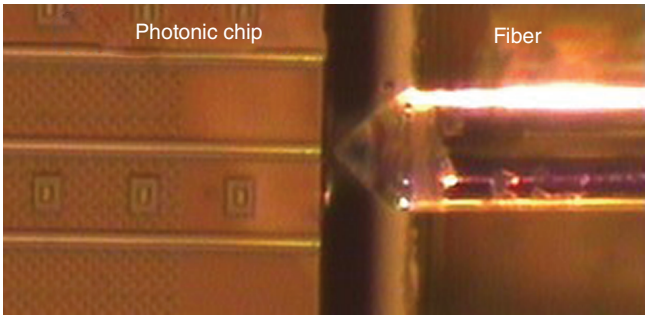


Figure 1.11 Lensed fiber to silicon photonics chip coupling. Source: S. Bernabé, CEA-Leti.

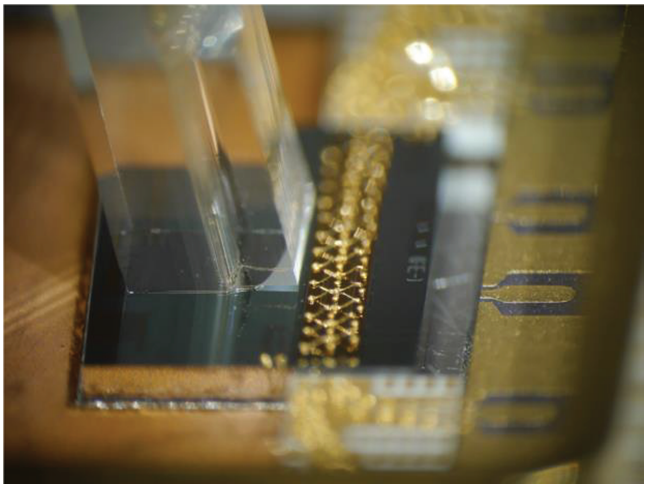


Figure 1.12 Butt coupling assembly of a silicon photonics PIC and a V-groove fiber array. Source: O.Castany, CEA-Leti.

a fiber array (Figure 1.12). UV-curing epoxy is used to fasten the assembly. Using optimized apodized VGC, CL as small as 1 dB has been reported after alignment and fixing, with lateral offset tolerance of +/−2 µm [20].

Efficient (<1.5 dB CL, PDL < 0.5 dB) coupling between thin SOI silicon photonics circuits and standard cleaved fiber have been demonstrated too [21] by using optimized spot size converting edge couplers, leading to potential multifiber alignment of fibers using this configuration.

1.2.5.3 Lens Coupling Scheme

This approach (Figure 1.13), widely used for the packaging of single chip laser diodes for optical fiber networks, achieves the mode-matching condition to a SMF by inserting an optical system of magnification $M = \omega_1/\omega_0$. It can be made of a single focusing lens or a dual-lens optical train. This second option is a good approach when an optical isolator has to be put in the optical beam to limit any optical feedback to the PIC. The first lens is used to collimate the beam, allowing the isolator to be put in the

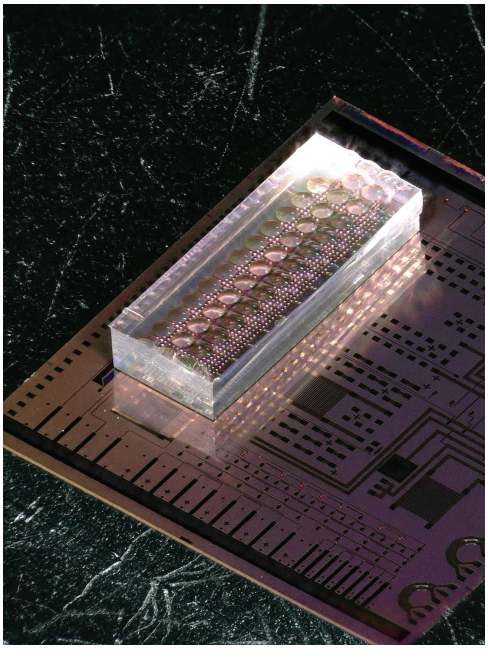


Figure 1.13 Microlens array assembled on the top a silicon photonics PIC to perform beam collimation. Source: O. Castany, CEA-Leti.

collimated beam, and the second lens is acting as a focusing lens to form the image of the PIC optical port at the input of the fiber. In reference [22], microlenses are used on both a VGC array and a FA array, fiber-to-PIC grating-coupling has been achieved with a CL of 1.7 dB (i.e. a coupling efficiency of 68%) at 1300 nm, and a 1 dB alignment tolerance of ±30 μm).

1.2.5.4 Optical Waveguide Interposer Coupling

An intermediate integrated waveguide can also be inserted between the PIC and the optical fiber, potentially acting as a SSC (e.g. glass waveguide obtained by ion-exchange process). In this case, active alignment using UV-curing adhesive remains the main option for assembly. An external waveguide, for example, a polymer waveguide on a flexible substrate can also be used to perform evanescent coupling between a PIC and an external fiber ribbon (Figure 1.14).

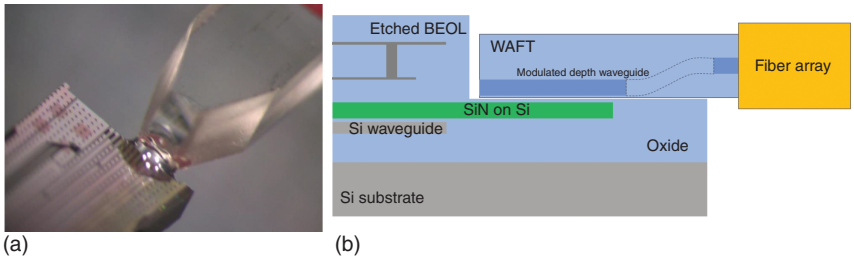


Figure 1.14 Glass interposer connected to a PIC, using (a) edge coupling approach (b) evanescent coupling. Source: A. Billat/Teem Photonics.

Using a three-stage coupler made of a Si–SiN–glass stack, <1.9 dB CLs have been demonstrated [23] at the SiN–glass transition, with low PDL (<0.4 dB) over a wide spectral range (>100 nm). Assembly has been performed using a flip-chip precision bonder from SET.

1.2.6 Emerging Trends for Module Mass Manufacturing

Driven by silicon photonics technology, PIC-based modules are now able to address applications requiring volume manufacturing (e.g. data centers, LIDARs) and in a second step dense integration of complementary metal-oxide-semiconductor (CMOS) and photonic circuitry for next-generation computing (e.g. manycore architectures using an internal optical bus). Indeed, silicon photonics comes with the promise of integrating CMOS electronics and photonics by using either monolithic integration or hybrid approaches, changing the paradigm of PICs by leveraging the semiconductor ecosystem in terms of design tools (electronic design automation – EDA) and foundries, with the related scalability in terms of circuit complexity and mass manufacturing capability. Even though legacy packages, inherited from telecommunication single laser diode package, are still used for small layout and prototyping ("*Gold Box*" approach) [24], they are making way to cheaper approach such as **PIC-on-board approach**, where the PIC is typically glued and wire-bonded to a PCB for the DC/HF connectivity [25]. Figures 1.15 and 1.16 show an example of both approaches.

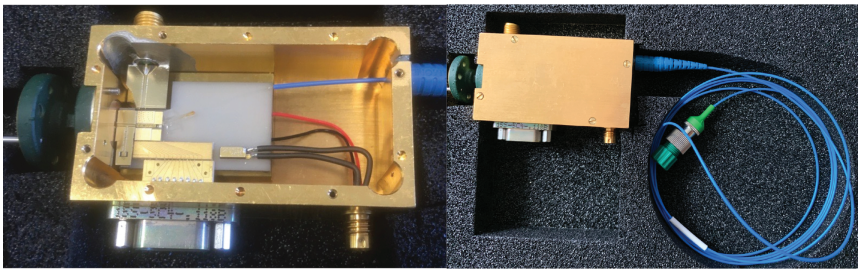


Figure 1.15 Gold box package developed within the EU-founded iPhos project. Source: B. Sirbu/Fraunhofer IZM.

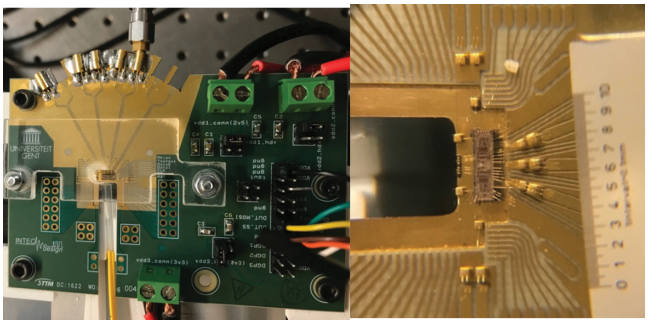


Figure 1.16 PIC-on-board package developed within the EU-founded 5G-PHOS project. Source: B. Sirbu/Fraunhofer IZM.

The expected next milestones of this evolution have been described in more detail in [13]:

- **Improved manufacturing flow for front panel modules (datacom) and emerging high-volume markets (e.g. LiDARs, …).**
  The integration of PICs in modules currently relies on legacy technologies, with inherent limitations in terms of throughput and thus cost. To address this, an adoption and optimization of all existing assembly and test technologies are required for the mass fabrication of modules, despite their high level of integration and complexity. The existing building blocks are leveraging new packaging approaches for the simplification of the assembly while rendering it simultaneously more robust. Obviously, the reduction of fabrication cost can be reached by pushing the boundaries of optoelectronic packaging automation from stand-alone assembly machines to integrated assembly lines, considering a new assembly flow. This is obtained by leveraging vision-assisted alignment at every step of the assembly process to drastically reduce assembly time for any assembly step which do not deserve accurate submicrometric alignment. For example, in the European Project MASSTART, a silicon photonics-based transceiver (400 Gbps) has been developed, intended to be packaged in a standard QSFP-DD chassis (Figure 1.17).
  The optical engine, which is the basis of the module, is made of seven optical components (1 laser array, two lens arrays, one isolator, one prism, the PIC, and one fiber array). These various components are assembled on a silicon optical bench (SiOB) using mostly vision-assisted techniques ("passive steps"), active alignment steps are used for the laser lens array and fiber array only.
- **Development and adoption of next-generation small footprint modules, i.e. Optical Engines and Co-package modules (CPO).**
  In a next step, the emerging applications such as high-speed optical networks, high-performance computing, and storage applications benefit from packaging

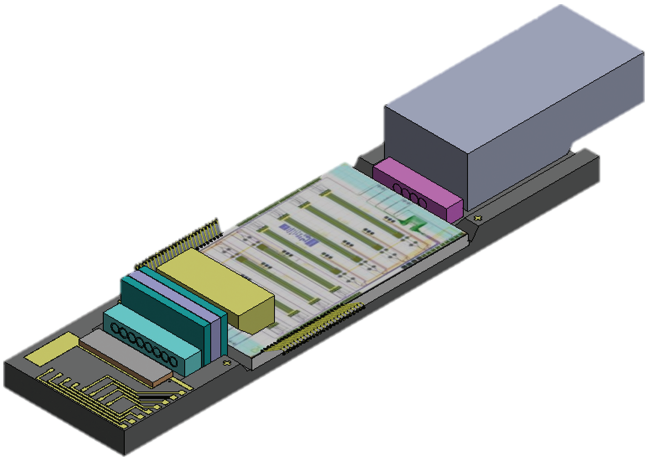


Figure 1.17 Microoptics assembly of a 400 Gbps Datacom transceiver (MASSTART project).

of photonics devices and electronic chips (e.g. ethernet switches, CPU, FPGA) together in a single package. This approach is known as co-package optics (CPO) [26, 27]. This rapidly growing technology is leading to the reduction of power consumption, thermal effects, and the required footprints. An area of considerable potential for CPO is in the high-speed industrial interconnect sector, where classical SerDes approaches may run out of steam over the coming decade. As high-speed interconnects become ubiquitous – in aerospace, video, and military applications – the market for CPO-based interconnects will increase.

Especially, in the field of data center interconnects, the data rate of network switches and transceivers is doubling every 18 months [13]. Today switches aggregated throughput is 5 Tbps and will reach 51.2 Tbps in 2025. Transceivers data rate will increase from 100 Gbps to 800 Gbps and the number of transceivers per switch will grow from 4 to 16 or 32. Therefore the density of data transfer in switches will increase tremendously, resulting in important integration and thermal challenges. CPO is therefore a key enabler for next-generation switches (Figure 1.18).

A promising approach to build CPO modules is the development of silicon photonics PICs-based "**photonic chiplet**," namely ultradense photonic transceivers, able to be co-packaged on a common BGA substrate together with the host CMOS chip [28]. This new paradigm will raise several new challenges at the packaging level, as it is analyzed in [29]:

- Very dense electrical interconnectivity, requiring high bandwidth (>50 GHz) maybe through silicon vias (TSV)-based architecture regarding the PIC.
- Reflow compatibility of the optical fiber connectors, enabling easy assembly of the BGA module on the motherboard. From this point of view, lensed coupling schemes are advantageous to avoid direct epoxy-based attachment of fiber pigtails.

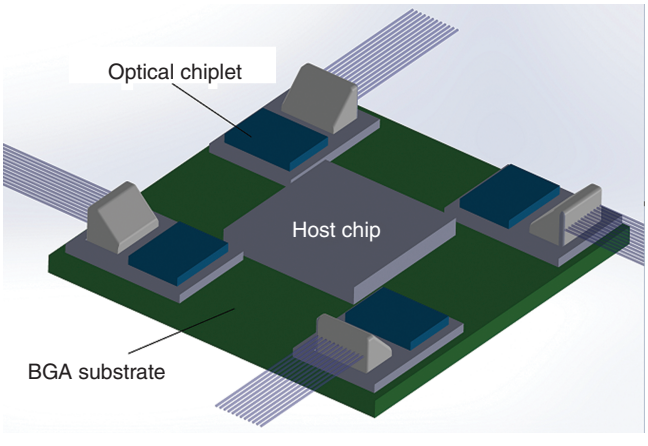


Figure 1.18 Co-packaging approach: the host chip is surrounded by optical chiplet providing high-speed transmitter/receiver capabilities, sharing the same package.

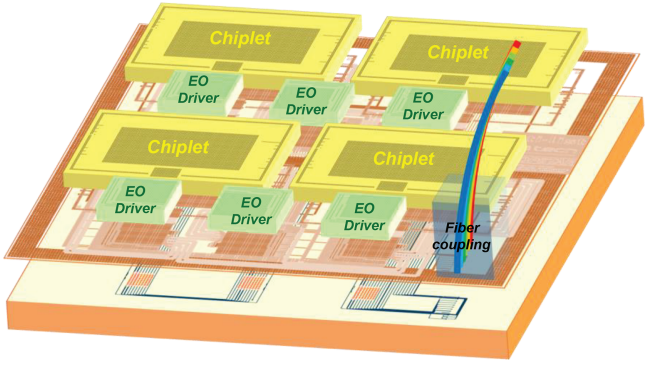


Figure 1.19 Photonic interposer, showing optical routing between several CMOS dies (multicore processors or memories). Source: CEA-Leti.

- Laser integration management, requiring smart laser to PIC integration or external lasers relying on low-cost packaging solutions.
- Thermal design preventing thermal crosstalk between the optical chiplet and the highly dissipating host chip.

These emerging approaches will surely see in a near future PIC packaging move from legacy technologies inherited from telecommunication markets (active alignment, pigtailed modules) to advanced optical coupling strategies, and the convergence between semiconductor packaging building blocks (TSV, flip-chip, etc.) and photonic circuits, through the massive use of 3D integration.

- **Dense co-integration of PICs and CMOS to build optical interposer-based architectures.**

  An ultimate co-integration of PICs and CMOS is the use of PIC circuits (especially silicon photonics PICs) as photonic interposers, enabling optical routing between several CMOS chips, such as CPUs to build manycore architectures [30]. In such an approach, 3D packaging (TSV) is expected to be widely used to connect the motherboard to the CMOS chips through the photonic interposer with back-side Controlled Collapse Chip Connection (C4) bumping, especially for supplies and service signaling [31], while high-speed optical IO will extend the architecture out of the package (Figure 1.19).

1.3 Advances in Optical Coupling Strategies

Active alignment strategies for optical coupling, despite a massive use in today's fabrication flow, remain limited in terms of fabrication throughput and scalability. They rely upon one of the following steps:

- External laser or integrated active devices (in PIC) activation. In case of external laser, optical power is launched in an optical fiber patchcord and then injected to the PIC from this fiber.

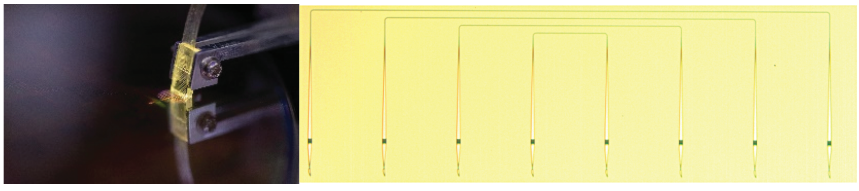
- Measurement of the optical power at one or several output ports of the PIC, or measurement of the photocurrent at the output of an integrated photodiode. As soon as a first light is detected, an active alignment process is engaged, using specific power optimization algorithm (e.g. "hill climb")
- When the maximum power is reached, the alignment is fixed by using the chosen technique (UV curing or laser welding).

Typically, for multiple optical I/Os PICs, an integrated optical loop (sometimes called optical shunt) is used to perform the alignment of a fiber array (Figure 1.20). Only two fibers are required to launch and collect light, while at the end of the alignment step, the remaining fibers of the arrays are aligned to functional optical ports of the PIC, because of their relative well-controlled position in the V-groove array.

1.3.1 Toward Passive Alignment Strategies

To achieve optical coupling without any activation of laser sources or photodetectors, alternative approaches have been developed, called passive alignment techniques [32].

Actually, these methods can be classified in several categories [33], depending on the use of open or closed loop to perform the alignment (Figure 1.21). Active



(a) (b)

Figure 1.20 Active alignment of a V-groove array embedding a single-mode fiber ribbon (a) and top view of a PIC showing vertical grating couplers type optical ports (b). Source: S. Bernabé, CEA-Leti.

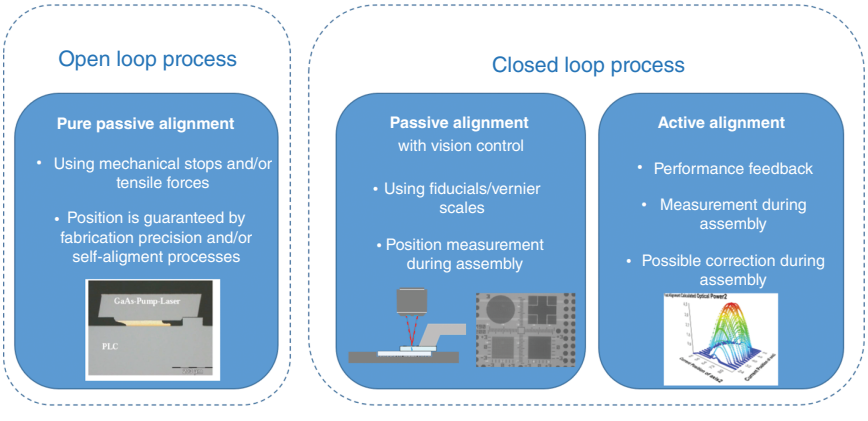


Figure 1.21 Active and passive techniques for automated optical coupling.

alignment is definitely a closed-loop approach, making use of an optical or electrical measurement. Another option is to use vision control to perform the mutual alignment of the PIC to an external waveguide, resulting in a continuous measurement of the relative position of the optical parts during the assembly steps, thanks to fiducials. Another class of passive alignment processes is open loop, relying on the accuracy of some mechanical features preprocessed in the optical parts to be assembled to ensure a final accurate position of the parts. It can be obtained by using mechanical standoffs. This class of alignments is sometimes referred to as self-alignment techniques.

The following subsections will examine technological approaches developed to obtain vision-assisted or self-alignment based assembly processes.

1.3.2 Advanced Technologies for Vision-Assisted Technologies

Generally, vision-assisted alignment can be divided into the two groups of open-loop alignment and closed-loop alignment (see Figure 1.21). One of the main limiting factors when it comes to alignment accuracies for vision-based assemblies lies in the movement between the position where the reference marks are measured and the final position where the part needs to be placed. To increase the alignment accuracy this distance needs to be kept as small as possible and can be down to a few microns in case of closed-loop alignment.

1.3.2.1 Open-Loop Alignment

In case of an open-loop alignment, the reference marks on the substrate and on the die are measured with an optical system while both are a certain distance away from the final assembly position. In typical configurations, a down-looking camera measures the reference marks on the substrate (Figure 1.22a) while an up-looking camera measures the reference marks on the bottom side of the die (Figure 1.22b). As both cameras are referenced with respect to each other the relative movement of the die to the final assembly position can be calculated (Figure 1.22c). This is, e.g. a classical approach for flip-chip assemblies where the reference marks at least of the die are not visible after alignment anymore.

The drawback of such systems is the dependence of the final alignment accuracy on the repeatability of the motion between the measurement and placement position, which themselves, depend strongly on changing environmental parameters. Typical alignment accuracies are in the range of a few micrometers which can be improved to hundreds of nanometers with more complex systems.

1.3.2.2 Closed-Loop Alignment

The highest passive alignment accuracies can be achieved with closed-loop alignments. Ideally, the reference marks are visible within one camera field of view, hence preventing any need for a movement of the camera over the parts. Possible configurations are either using a down-looking camera with which substrates/dies with reference marks on the top side can be aligned. In case of flip-chip processes that have the alignment mark on the bottom side of the die split-screen approaches can

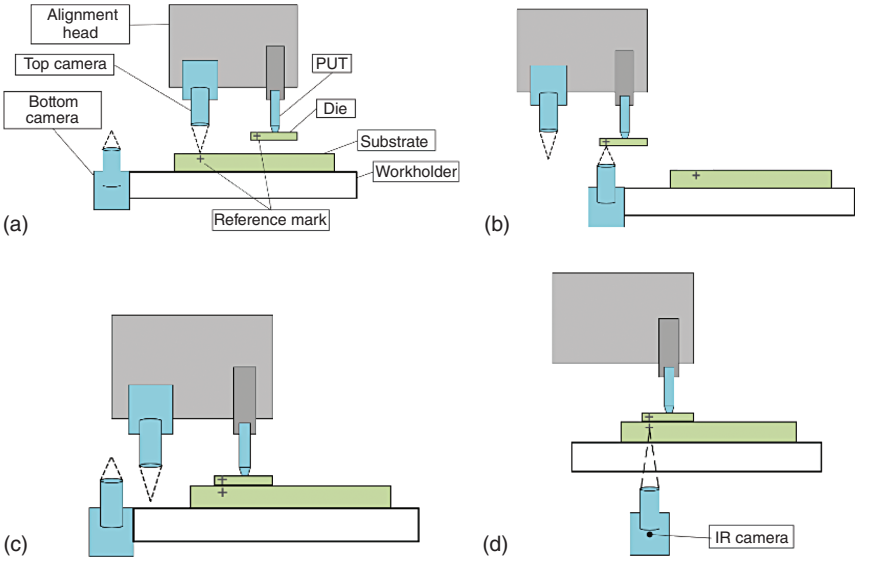


Figure 1.22 (a) Configurations for top camera measuring reference mark of substrate. (b) Configuration for bottom camera measuring reference mark on die. (c) Final alignment configuration. (d) Configuration for IR-based alignment.

be used to overlay pictures of the reference marks on the die and substrate in one picture on the camera. The drawback is that after the alignment a gap in the range of several millimeters must be closed before bonding the components together, leading again to a certain inaccuracy due to the axis movement.

An innovative and very promising technique is the use of infrared optical systems for the alignment. With such systems, reference marks and optical features such as waveguides can be detected through a silicon PIC. This technique allows a closed-loop alignment of flip-chip assemblies while both reference marks are in the same plane of focus; hence, practically no axis movement is required after alignment (Figure 1.22d). With such systems, the alignment accuracies of passive assembly processes can be dramatically increased reaching regions for which up to now an active alignment was required.

1.3.3 Advanced Technologies for Self-alignment Strategies

Self-alignment of optical parts mainly relies on the use of melted metallic features (solder pads, solder balls, …), leveraging tensile forces to ensure self-positioning of the assembled parts, in addition to electrical interconnects through the same features. This is generally combined to silicon etching processes using established MEMS processes (wet etch, DRIE Bosch process) to generate alignment features for optical fibers (V-grooves) or standoffs.

The following paragraphs are detailing typical achievements using self-alignment approaches.

1.3.3.1 Self-alignment of Fiber to PIC Through an Silicon Optical Bench Using Flip-Chip

Presented by Wale and Edge in their 1990 seminal paper [34], the module architecture relies on solder balls employed to attach the PIC to a SiOB carrying optical fibers and V-grooves and electrical connection patterns, with resulting excess loss of 1 dB. This approach, which relies on the accuracy of the photolithographic steps used to pattern the SiOB, has been used in several fiber optic modules assemblies from various companies to couple light from a single flip-chipped laser diode to a SMF [32]. In recent papers, Barwicz et al. demonstrated efficient coupling of fibber ribbons to silicon photonics PICs by etching V-grooves in the PIC in front of edge couplers obtained by metamaterial-based edge couplers ensuring spot size conversion [35] (Figure 1.23).

The resulting assembly exhibits 1.3–2.2 dB CL over 100 nm spectral bandwidth and low PDL.

Coupling of laser arrays to optical fibers ribbons using mechanical stops (standoffs) to the previous Wale's architecture has been demonstrated in 1995 by Hunziker et al. [36]. Coupling of laser arrays to fibers placed in etched V-grooves in a SiOB has been achieved, the laser being positioned in front of the fibers with help of mechanical mesas, resulting in <0.5 dB excess losses. This process can be applied to laser to PIC coupling too, as described in the next section.

1.3.3.2 Self-alignment-assisted Microlenses Assembly

Microlenses can efficiently be used to perform PIC to fiber coupling by using one or two lens coupling schemes (Section 1.2.1). In such an approach, the microlens position toward the PIC's optical port has to be controlled with submicronic accuracy. Using microbumps with self-alignment capability due to capillary forces during reflow has been demonstrated to be a good option to obtain <0.5 μm positioning accuracy [37] (Figure 1.24).

1.3.3.3 Self-alignment of Polymer Waveguides

In 2014, Barwicz et al. demonstrated the effectiveness of passive alignment strategies to perform alignment of polymer waveguides to silicon photonics PICs [38].

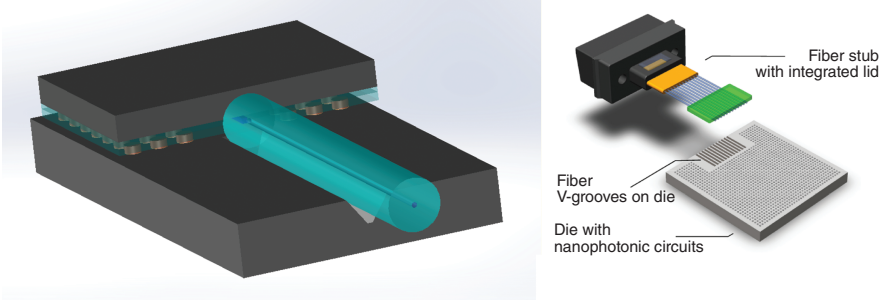


Figure 1.23 Passive coupling of optical fiber to a PIC using V-groove (a) using solder bumps and a SiOB [Wale & Edge] (b) with direct etching of the V-groove in the PIC (Barwicz). Source: S. Bernabé, CEA-Leti. Barwicz et al. [35]/IEEE.

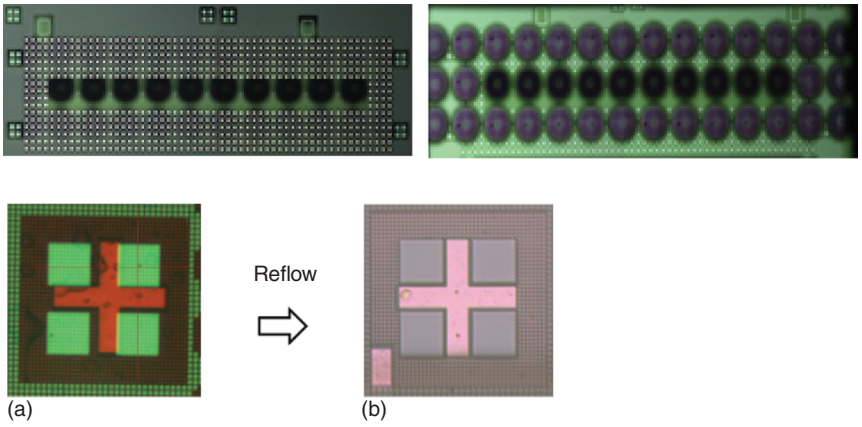


Figure 1.24 (a) View of a microlens array made of silica, with post-processed metal pads on the bottom side (left) and microlenses on the top side (right). (b) The chip is pre-aligned with a pick-and-place equipment and the alignment pattern shows initial misalignment (left). Self-alignment occurs during thermal reflow, resulting in a properly aligned chip (right). Source: S. Bernabé, CEA-Leti.

In the experiment, PICs are processed with etched cavities and polymer waveguides are providing mechanical structures to perform passive assembly with <2 μm accuracy, and robustness to initial 10 μm misalignment. In this case, optical coupling is obtained by using evanescent coupling between the PIC waveguides and the assembled polymer waveguides (Figure 1.25).

The complete assembly, including a MT style connector assembled with the polymer flex, exhibits 1.6 to 2.1 dB loss over a ~100 nm bandwidth and is polarization independent.

1.3.3.4 Self-alignment of Optical Plug

Israel et al. [40] developed an advanced strategy for relaxed tolerance coupling between a silicon photonic PIC and an optical plug holding fibers. This approach relies on a double-curved reflector optical scheme providing a collimated beam between the two reflectors, thus drastically relaxing in-plane tolerances (Figure 1.26). Spherical reflectors are micromachined on both sides using grayscale lithography. The architecture shows a relative 0.5 dB excess loss over a 40 μm lateral positioning, and additional 0.6 dB loss due to the mirror reflectance.

1.3.4 Laser/PIC Coupling

Addressing the topic of photon source integration (laser diode) with the photonic circuit remains a key challenge to maintain the fabrication cost of PIC modules low. Depending on the used PIC technology, the chosen approach may be different. For InP-based PICs, the **monolithic integration** of the laser diode within the PIC is the most suitable. For silicon photonics-based circuits, three main technologies exist. The first one relies on III–V die to PIC direct bonding [41, 42]. It consists of achieving

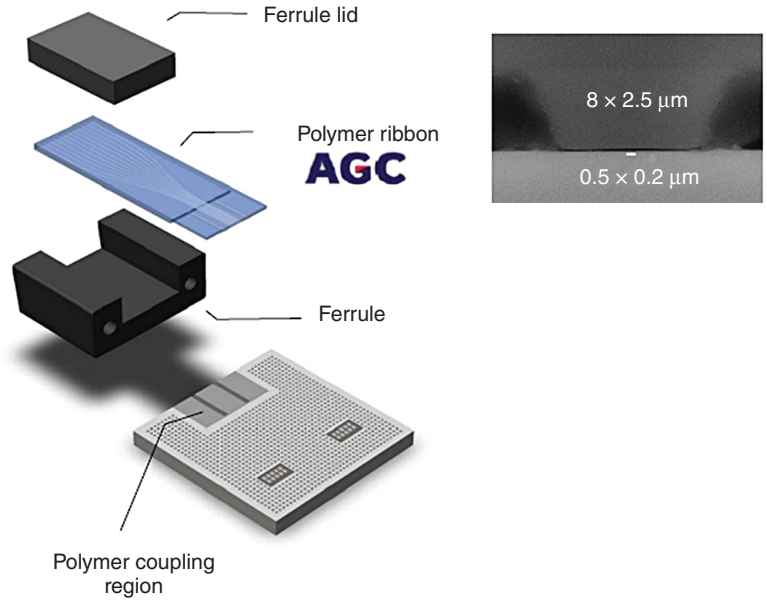


Figure 1.25 Passive alignment of an optical flex embedding polymer waveguides, to a silicon photonics PIC. Source: Barwicz, et al. [39], Optica Publishing Group.

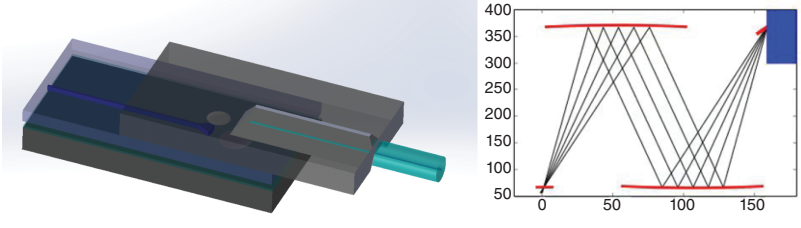


Figure 1.26 Relaxed tolerance assembly using an optical plug with two reflecting mirrors (units = microns). Source: S. Bernabé, CEA-Leti. Israel et al. [40].

a molecular bonding between the upper oxide layers of a PIC and a piece of III–V material made of a stack of epitaxially grown layers, able to provide optical gain in the system. These III–V dies (also known as coupons) are bonded at a given distance above SOI waveguides. Further process steps are done to build a waveguide in the III–V material, allowing optical coupling between both SOI and III–V waveguide, forming the gain section of the laser.

The second approach has been developed by Luxtera [43]. It consists in the active alignment and fixing of a **micropackaged laser diode** above a VGC. The laser

Figure 1.27 Fraunhofer IZM self-alignment assembly technique: (a) schematics of self-alignment concept with mechanical stops, (b) cross section of one of the test-vehicles demonstrating the accuracy of the self-assembly concept. Source: H. Oppermann/ Fraunhofer IZM.

micropackaging is obtained by assembly of a III–V laser diode die on a SiOB, together with a Faraday rotator and a focusing microlens. A hermetically sealed silicon etched cap is acting as a reflector to redirect the beam to the PIC. Assembly and sealing steps are done at wafer level. The final wafer assembly is diced in a final step to get the single lasers.

Finally, a third approach is the **heterogeneous assembly** of a diode laser or a diode laser array in front of the PIC's optical waveguides using microassembly techniques. This kind of assembly is popular for passive PICs made of glass or SiN waveguides, as well as for silicon photonics devices. The assembly is ruled by the coupling laws described earlier in this chapter, with the aim of accurately aligning the laser's beam and the PIC's optical port's optical axis. As for optical fiber coupling, active alignment is feasible by using dedicated equipment, but passive processes have been demonstrated, e.g. [44–46] in Figure 1.27:

In these demonstrators, the laser die is post-processed with UBM pads, and flip-chip onto corresponding solder bumps on the PIC top surface. During the reflow process, the surface tensions moves the laser die in contact with lithographically etched stops machined on both sides, leading to a final submicronic alignment in the three dimensions.

1.4 Electronic/Photonic Convergence

To achieve dense heterogeneous integration of photonic and electronic IC chips, 3D interconnections can offer interesting approaches. In this section, an overview of die-to-die interconnections and intra-die connections (or intra-connections) will be first given, followed by discussions concerning fan-out wafer-level packaging and interposers structures. Full descriptions and detailed process flows can in found in literature focusing on 3D integration for CMOS devices [47, 48].

1.4.1 Flip-chip Interconnects

1.4.1.1 Standard Die-to-die interconnects

To interconnect two dies or more, various approaches are available and described in Figure 1.28. It is possible to distinguish three families of flip chip processes: welding, adhesive joining, and soldering. The following sections will describe some particular examples of die-to-die interconnects, from the standard industrial processes to the more advanced strategy.

Soldering of AuSn Solder Bumps Eutectic AuSn solder bumps are widely used in flip-chip assembly of optoelectronic devices [49]. AuSn has unique physical properties with respect to stability, melting temperature, corrosion resistance, wetting behavior, and surface tension. AuSn soldering does not require flux, which is an advantage for optoelectronics packaging and for hermetic sealing applications. The AuSn can be created by multilayer deposition or electroplating of Au and Sn in successive process steps followed with a reflow process [50]. The liquefying and wetting process of AuSn can be controlled with an appropriate temperature profile in the reflow oven. The standoff gap height is controlled by the bump height and it allows in combination with mechanical features a self-alignment process enabling a low-cost passive assembly process. Typical pitch of the interconnects is in the range of 50 µm, but in some cases, it can go down to 20 µm while the typical bump diameter is in the range of half the pitch values.

Soldering of Copper Pillars/Bumps Most die-to-die interconnections are achieved thanks to the soldering of the upper die onto the lower die or wafer after the reflow of a dedicated melting alloy. From the range of 500–100 µm interconnection diameter, tin–silver ball placement or screen printing of tin–silver paste processes are available [51]. These solutions offer processes with high throughput and low cost. While reducing the diameter and so the pitch of the interconnection from 200 to 20 µm [52] or even experimentally 5 µm [53], pillars of copper are used on

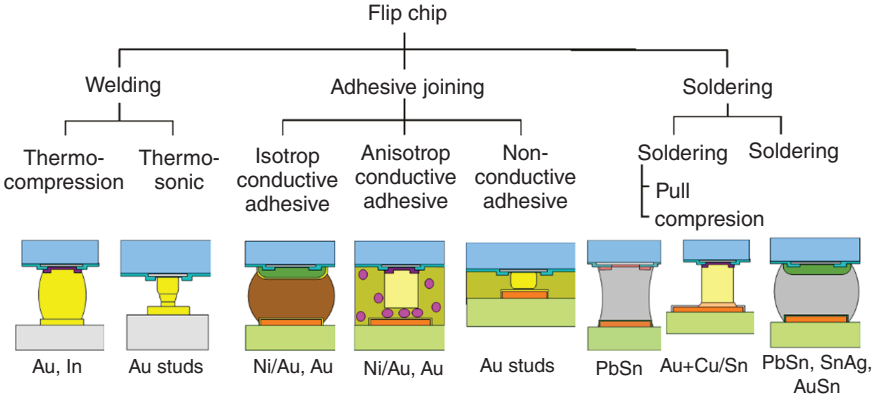
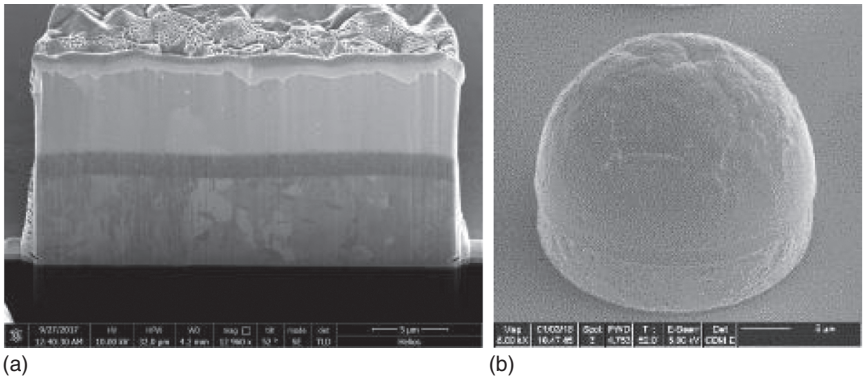
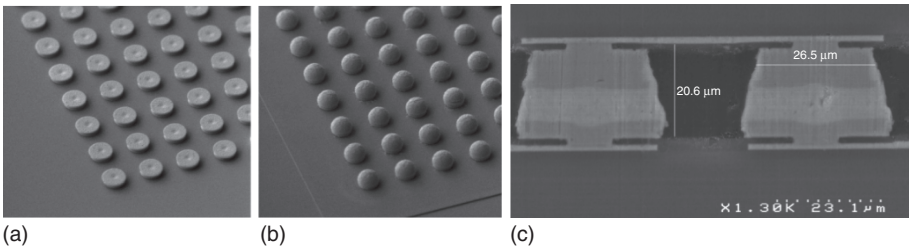


Figure 1.28 Landscape of the main flip chip processes with interconnections materials. Source: H. Oppermann/Fraunhofer IZM.



(a) (b)

Figure 1.29 Cross section of a 25 μm diameter copper bump before reflow with from bottom to top, copper, nickel, and tin–silver alloy metallic stack (a) and the tilt SEM view of the copper bump after reflow (b). Source: J. Charbonnier, CEA-Leti.



(a) (b) (c)

Figure 1.30 Example of 50 μm pitch copper pillars (a), copper bumps (b), and their assembly (c). Source: J. Charbonnier, CEA-Leti.

each dies. Classically, top die pillars have a solder finish; these pillars are then called copper bumps and the bottom die a gold finish on the pillars called copper pillars (Figures 1.29 and 1.30). Each of them features a nickel barrier from 1 to 2 μm thick to prevent any copper diffusion into the alloy. The thickness of these copper bases can be optimized by electroplating process time to avoid short circuits between soldering compounds and to set the standoff between the dies facilitating the further underfilling process. This approach for interconnection pitches of 40 μm and greater is now in high-volume production at several OSATs.

1.4.1.2 Advanced Interconnects for Future Needs

Nanoporous Au Use of pure gold bumps is an interesting option to reduce mechanical stress by plastic deformation due to their ductile behavior. Large deformations take place in case of joining two metal interfaces to planarize the contact surfaces and to remove contamination or oxide layers, which accompany by perpendicular flow of the material, changing the bump shape from a cylinder to a barrel and reducing the space between bumps. Here, by using porous, cellular structures a high compressibility can be achieved compared to their bulk counterparts. Furthermore, by decreasing the pore size to nano- or mesoscale the highly reactive surface leads

to a reduction of the bonding temperature. The Au foam can be produced by extracting Ag component from Au–Ag alloy leaving an open-porous structure, so-called de-alloying process. The wafer-level deposited open-porous Au bumps can be used in thermo-compression flip-chip bonding. The bonding process temperature can be reduced along with lower bonding pressure. The technology does not require the planarization of the surface and improves the yield during bonding process [54].

Indium Micro Balls In parallel to copper pillars and copper bumps interconnection, Indium micro balls offer an interesting approach for low pitch and dies of heterogeneous substrate. For example, AsGa or InGaAs substrate exhibits an important mismatch of CTE with silicon standard substrate. This implies a risk of delamination and failure of the interconnection between the two types of substrate due to shear stress during the assembly process which frequently involves temperatures up to 260 °C for the soldering processes on PCB substrate. Indium deposition is done by means of evaporation on a patterned resist followed by a lift-off process. Despite the higher cost of this process due to indium material itself, an interconnection pitch of 7.5 µm can be reached [55].

Hybrid Bonding If a higher level of integration and reliability is needed, wafer-to-wafer or die-to-wafer hybrid bonding interconnections are indicated. The process involves two extra levels of copper damascene, designed with dedicated rules on local density, for each upper and lower wafer and cautious chemical mechanical polishing steps before direct bonding with alignment and final annealing. Using this approach, interconnection pitches as low 1 µm have been demonstrated for wafer-to-wafer stack with excellent reliability properties [56]. One drawback of hybrid bonded structures could be the thermal dissipation and RF cross talk since the chips are in then close contact without any standoff.

Table 1.1 introduces a synthesis of die-to-die or die-to-wafer interconnections. Due to the size of optical devices like ring modulator, in the range of the tens of microns, architecture requiring interconnection pitches lower than these values are not expected at the moment. However, the emergence of manycore architecture involving optical routing could change this fact. Figure 1.31 shows an overview of the most popular bump and assembly technologies used for PICs, underlining the

Table 1.1 Results for the comparison of processes.

Interconnection	AuSn	Sn alloys balls	Copper pillars bumps	Nonporous gold	In balls	Hybrid bonding
Typical dimension (µm)	50–20	500–150	150–5	5–3	150–5	10–<1
Substrate heterogeneity	Possible	Possible	Possible	Possible	Favorable	No
Post processing	No	No	Limited	No	No	Yes
Cost	Low	Low	Medium	Low	High	High

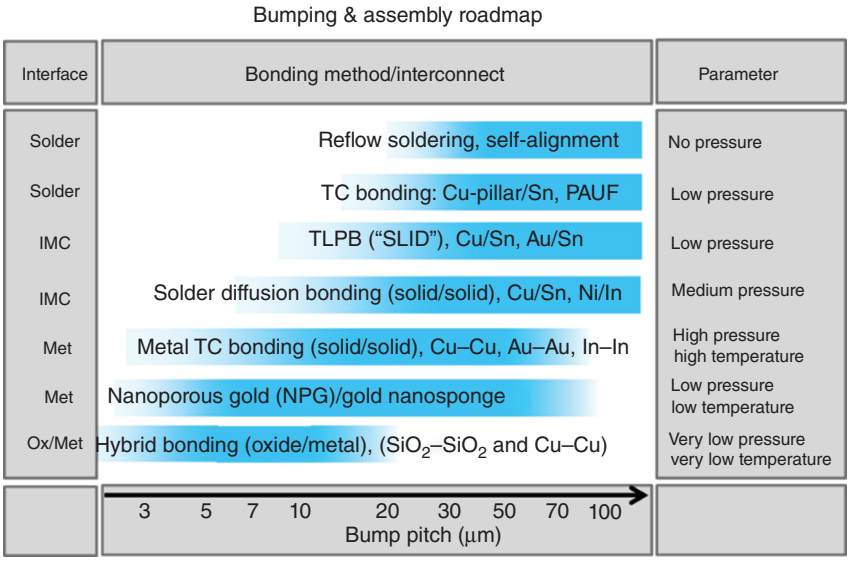


Figure 1.31 Overview of the different bump and assembly technologies. Source: H. Oppermann/Fraunhofer IZM.

difference in bump pitch which can be achieved, different interface materials, or the requirements in terms of pressure or temperature for each of the mentioned assembly technologies.

1.4.2 Intra-connections (Through Silicon Vias and Through Glass Vias)

To access to electrical pads from the backside of chips, intra-connections such as TSV have been developed since 15 years with first application for CMOS image sensors [57]. The principle consists in etching the silicon substrate to form vias that will then be metalized to connect the front side of the devices from the back side. It is possible to identify two main families of TSV called "TSV last process" where TSV are processed after the front side process (FEOL and BEOL) straight from the back side and "TSV middle process" where TSV are formed between the FEOL and the BEOL. The bottom electrical contact of the TSV is made from the backside afterwards. Both types of TSV will be described hereafter.

1.4.2.1 TSV Last Process

The main difference between these two TSV fabrication processes lies in the fact that for the TSV last process, the via integration is done after the complete wafer processing. In the via last case, the TSV is processed through a thick BEOL oxide and requires keep-out zones in FEOL and BEOL for via integration, being necessary to have landing pads in BEOL for TSV connection. Due to conformality consideration of the via insulation and contact opening at the via bottom, the diameter of via last is usually ranging from 40 to 80 µm with resistances of few milliohms thanks to a thick copper liner. Hence they require large contact or bonding pad on front side

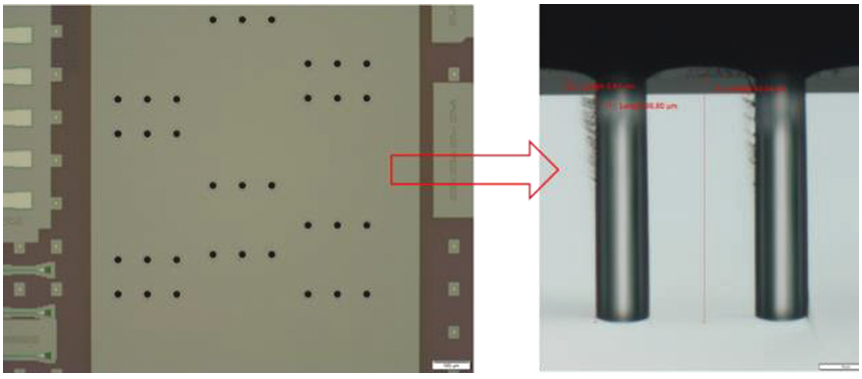


Figure 1.32 TSV last process at Fraunhofer IZM (top view and cross-section). Source: K. Zoschke/Fraunhofer IZM.

to be implemented. Figure 1.32 shows the TSVs developed within the EU Founded MASSTART project where this TSV last fabrication process has been employed to integrate high-speed TSVs with bandwidth higher than 60 GHz by Fraunhofer IZM on CEA-Leti SiPh wafers.

1.4.2.2 TSV Middle Process

Compared to TSV last process, TSV middle process (also called TSV mid) starts just after transistors or active devices contact and before first metal layer. In some particular cases, the TSV can be formed between metal layers inside the BEOL stack. As there is no need for temporary bonding of the substrate for the TSV formation, the process does not have the limitation in terms of process temperatures compared to TSV last process. After deep reactive ion etching of the via, this allows dielectric deposit processes at 400 °C.

At this temperature, standard PECVD dielectric deposit or SACVD dielectric process is conformal, in aggressive aspect ratio TSV from 5 : 1 to 10 : 1.

Various sizes of TSV middle process have been successfully integrated in this aspect ratio range (diameter × height): 5 × 30 µm (A*STAR), 5 × 50 µm (IMEC) or 10−12 × 100 µm (Leti, TSMC, ASE, GF, A*STAR). Concerning the metallization, TSV middle process requires to be fully filled with copper to be compatible with the following BEOL layers integration. MOCVD or iPVD process is used for titanium nitride or tantalum diffusion barrier deposit along the TSV sidewalls followed by copper PVD and or CVD layers as seed layer for the electroplated copper filling using a dedicated bottom-up chemistry [52, 58] (Figure 1.33).

After the formation and metallization of TSV mid and completion of front-side processes, the wafer is then flipped and bonded to a temporary carrier thanks to an organic adhesive. The substrate is then back grinded to keep 10 µm of silicon on the top of the TSV mid-bottom. A selective reactive ion-etching process allows revealing the bottom of TSV also called copper nails. These nails are then insulated with a low-temperature PECVD dielectric and planarized thanks to a chemical mechanical polishing process.

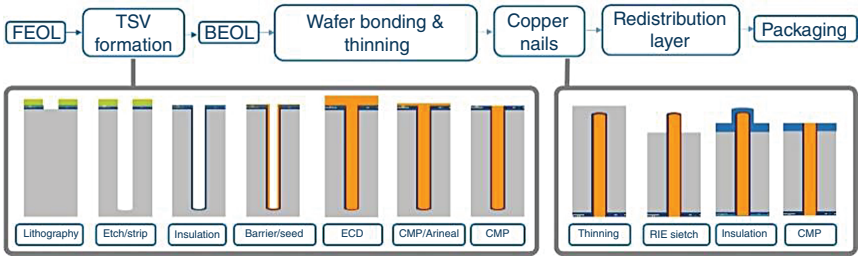


Figure 1.33 Overview of TSV mid-process flow.

1.4.2.3 Through Glass Via (TGV)

To provide electrical feedthrough connection between both sides of the glass substrate through glass vias (TGV) have been developed for advanced packaging solutions where glass is used as platform material such as glass interposers. Glass as substrate material with its properties insulation, smooth surface, good chemical durability, low dielectric constant, low CTE, high E-modulus becomes an alternative solution in 3D integration. Compared to the TSV processes the realization of TGV becomes challenging due to the properties and processing boundaries of glass itself. Following the formation of through-holes in glass thicknesses (50–500 µm), a common metallization method of TGVs is done by galvanic deposition, which requires an electrical conductive seed layer [59].

1.4.3 Fan-out Wafer-level Packaging (FOWLP)

One of the latest packaging trends in microelectronics and PIC is fan-out wafer level packaging (FOWLP). It enables a substrate-less package with low thermal resistance and high RF performance due to shorter interconnects together, making it attractive for the PIC packaging. By using thin-film metallization instead of the traditional wire bonds or flip chip bumps, a direct IC connection with low parasitic effects can be established, leading to a potential increase in the frequency operation. Additionally, the PIC or the passives (R, L, C) can be embedded in the redistribution layer to enhance the acceptance in multi-chip packaging for system in package (SiP) and heterogeneous integration.

There are two main approaches for embedded PIC technologies:

- Fan-out wafer-level integration, where dies are embedded into polymer encapsulants.
- 3D vertical integration, where dies are embedded into the substrate.

FOWLP applied to multichip EIC/PIC modules has been started in volume production for mobile and wireless applications (mainly wireless baseband) and is now moving toward more advanced PIC packaging for automotive and medical applications.

Two basic process flows can be encountered: the “Mold first” and the “RDL (redistribution layer) first” approaches (Figure 1.34). By now, for the “Mold first”

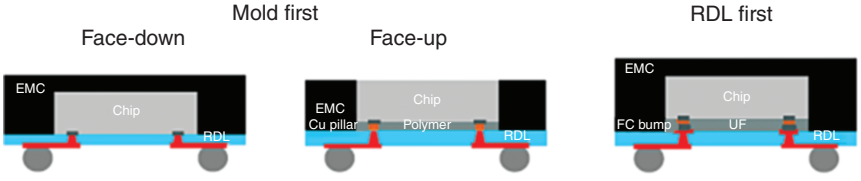


Figure 1.34 Fan-out wafer-level package structures from different process flow options. Source: T. Braun/Fraunhofer IZM.

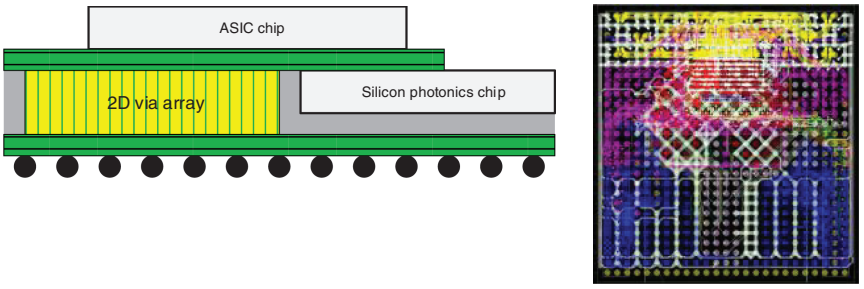


Figure 1.35 Massive routing and design for FOWLP, Industrial data center application, routing over19 layers for ASIC: 2300 I/Os, 130 and 80 µm pitch, Si-Photonics: 900 I/Os, 80 µm pitch, BGA: 750 I/Os, 500 µm pitch, Signal integrity (28 GHz), Power integrity. Source: B. Sirbu/Fraunhofer IZM.

process, a facedown and a faceup option exist. Both variants are already in mass production.

The "mold first" facedown approach has the shortest HF interconnect with a direct plated via. This may lead to the best RF performance at higher frequencies due to there being lowest loss, especially when the chip-to-chip connection is considered. "Mold first" faceup needs a Cu pillar in combination with a plated via, and "RDL first" even needs a soldered interconnect. Figure 1.35 shows one of the FOWLP packaging concepts developed at Fraunhofer IZM, where the PIC and a 2D via array have been embedded in the package using the "mold first" with faceup approach. As it can be seen in the following picture, the RDL layers cannot cover the entire surface of the package, an exclusion area in the RDL being necessary for the assembly of the optical interconnect to the PIC.

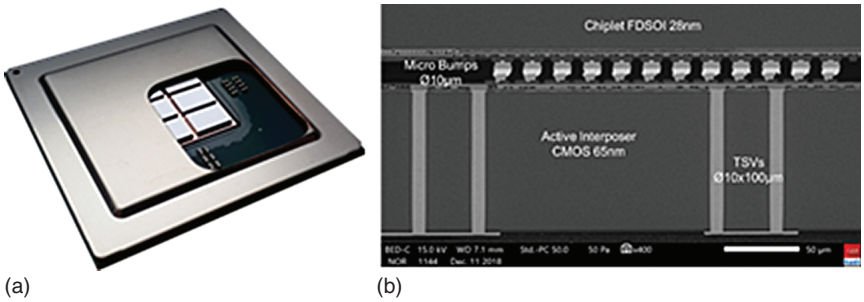
1.4.4 Interposers Integration Approach

With the growing need of heterogeneous integration, the interposer concept, enabling interconnections between generic heterogeneous dies, proposes an interesting alternative to classical 2D packaging. This section will first briefly described the different flavor of interposer's technology and then focus on the last studies concerning their integration in photonic system on chip, through the novel concept **of photonic interposer**.

1.4.4.1 Interposers for Electronic Integrated Circuits (CMOS)

The first developments, concerning passive interposers, have been pushed 10 years ago by the need of dense interconnection between dies as for example high bandwidth memory and processors, overcoming the limitation of BGA substrates in terms of line/space dimensions, and interconnection pitch. Silicon and standard processes of back end of line (BEOL) routing have so been used to develop silicon interposer with interconnection pitch below 1 µm [58, 60]. These types of interposers requires front-side interconnections for die stacking, front-side routing levels, TSVs last or mid depending on the routing density required by the application, optional backside routing levels, and backside balls to connect to the substrate. When high-frequency signals are involved, glass interposer thanks to their low dielectric constant, compared to silicon substrate, will end with reduced parasitic inductances and so offers interesting solutions [59]. Recently, a demonstrator of **active silicon interposer** for High-Performance Computing (HPC) applications has been introduced in Figure 1.36 [52]. The concept is to add active circuits inside the interposer which become a full circuit for specialization and system optimization. Due to the large size of the interposer, a mature technology has been chosen to ensure a high yield and to keep the costs low. The technology features six 22 mm^2 FDSOI 28 nm chiplet connected to a 200 mm^2 CMOS 65 nm interposer with 10 µm diameter micro bumps with a pitch of 10 µm for 25 000 interconnections per die. The interposer is crossed by 14 000 TSVs of diameter 10 by 100 µm height.

This last approach opens new perspectives in terms of increased interconnections bandwidth and density with typical network-on-chip (NoC) architecture. The communication from any chip to any chip of the system is now possible compared to passive interposer architecture limited to chip-to-chip and side-by-side connection. However, even this approach is not able to face the major challenges in terms of bandwidth, latency, and power for communications between cores and memories with more than four to six chips network due to intrinsic limitations of electrical routings. Photonic interposers are thus the new players to pursue the roadmap.



(a) (b)

Figure 1.36 Active interposer, (a) INTACT prototype with opened lid to observe the structure, (b) technology cross sections with top FDSOI 28 nm dies and Active Interposer in CMOS 65 nm node technology. Source: J. Charbonnier, CEA-Leti.

1.4.4.2 Photonic Interposer and Photonic Systems on Chip

As previously introduced in Section 1.4, photonic interposers or modules exhibit disruptive perspectives in terms of communication bandwidth and latency. Among the most advanced research group, IMEC and A*STAR together with Fraunhofer and Leti have proposed several approaches as described in Figure 1.37 [61–63]. IMEC and Leti focus on 10 or 12 µm diameter and 100 µm height TSVs, Fraunhofer 20 µm diameter 100 m height TSVs.

From a system point of view, it possible to distinguish data-communication applications from HPC ones. In the first case, the photonic interposer and its driver/TIA is essentially an optical interface between the outside world, meaning the optical fiber and the FPGAs or ASICs of the system. Hence, the electrical routing between the ASIC/FPGA and the optical module will have to be adapted to high-frequency signals in the range of 50 GHz or more. This is one of the main challenges of these systems extensively studied. Concerning HPC applications and chiplet partitioning, the concept of optical network on chip (ONoC) has been developed recently from thermal microring wavelength stabilization [64] to full system topology and architecture [31].

Independent from their targeted applications, the compatibility of 3D technologies, as previously introduced, and silicon photonics integration has been proven to define photonic interposers generic design rules. This work has been carried out in terms of keep-out zone between microring and TSVs of diameter [65, 66].

As can be seen in Figure 1.38, co-integration of TSV and sensible microring resonator (MRR) has been achieved without any impact on MRR properties even at a distance of 1 µm. These results pave the way for dense integration of MRR and TSVs.

A Si photonics interposer has been developed within the Phoxtrot project, where Fraunhofer IZM has been involved in the recent years [67]. This silicon photonics interposer had router functionality and comprises a single-mode silicon photonics layer designed for 1.55 µm wavelength, assembled high-speed VCSELs and PD arrays driven by respective RF Driver/TIAs 3D integrated on the active interposer (Figure 1.39). The silicon photonics Interposer was assembled on a glass carrier, providing the electrical signals driving the optoelectronic components and chip-to-board optical interfaces. This integration concept enables a high

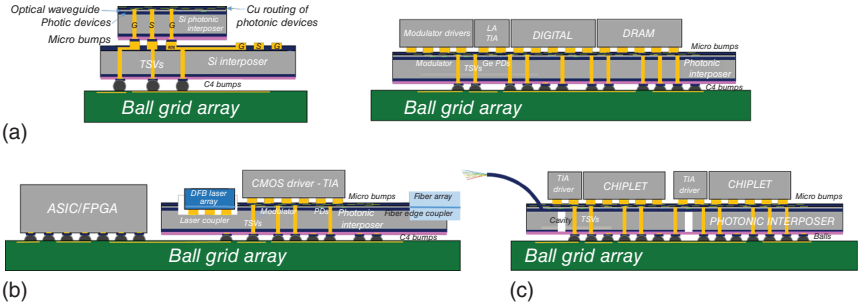


Figure 1.37 System overviews including photonic interposer, (a) A*STAR scheme, (b) IMEC & Fraunhofer integration, (c) Leti Integration. Source: J. Charbonnier, CEA-Leti.

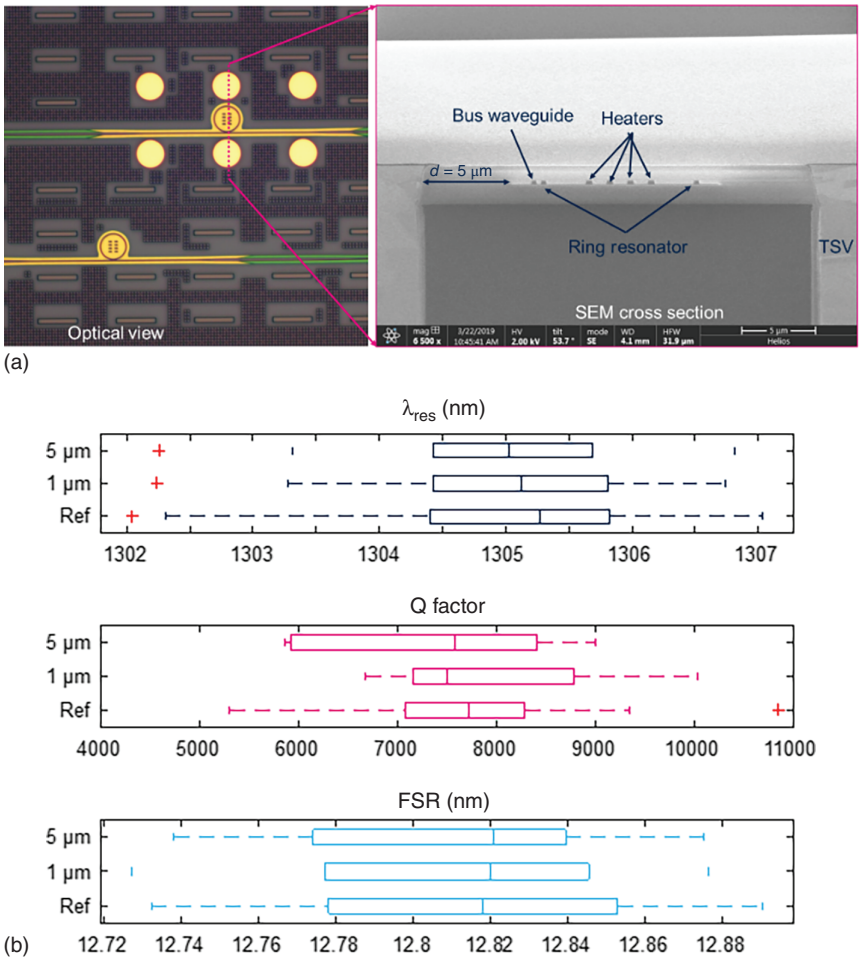


Figure 1.38 (a) Optical and SEM cross section of ring modulator with 10 µm diameter TSV in the vicinity. (b) impact on the ring modulator resonance wavelength, quality factor, and free spectral range of the position of the TSV at 1, 5 µm, and without for reference. Source: J. Charbonnier, CEA-Leti.

connection density (Gbps/mm^2) by assembling 40 Gbps per channel opto-electrical components on both sides of the interposer. Communication between components on both sides of the interposer is enabled by optical and electrical TSVs with a 3 dB bandwidth >28 GHz. The 3D silicon photonics interposer supports a data throughput of 1.28 Tbps as on-board photonic interconnection for data centers.

Leti is currently in the fabrication process of an ONoC [31]. The photonic interposer is designed to host 4 chiplets of 16 cores each and 6 Transceiver chips. All the interposer-to-chips interconnections will be performed thanks to copper pillars 20 µm diameter, 20 µm space, and the interposer to PCB interconnection thanks to 10 µm diameter 100 µm height TSV mid landing on backside RDL and bumps. To compensate global thermomechanical deformations, during the packaging steps,

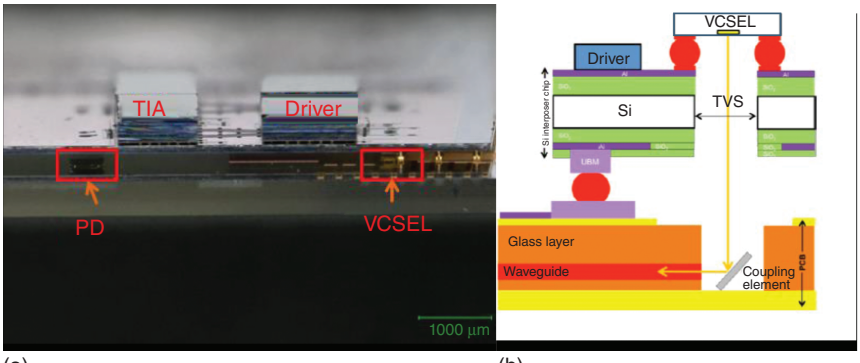


Figure 1.39 (a) Phoxtrot project demonstrator showing the 3D integration concept of driver, TIA, PD, and VCSEL chips on a Si Interposer. (b) Schematics of the Phoxtrot Si Interposer concept. Source: B. Sirbu/Fraunhofer IZM.

the backside copper RDL density has been optimized to balance front-side metallic levels stress using recommendation from [68]. Moreover, the resonance wavelength tunable range of the MRR has been increased on purpose using specific backside cavities designed for thermal insulation and thus better efficiency of the MRR heaters. This concept is developed in [69] and allows energy savings as high as 72% on the global ONoC energy consumption budget.

1.5 Toward an Ecosystem in Test and Assembly of PICs

With PIC-based optoelectronic devices becoming increasingly popular, and targeting application with expected higher volumes, PIC industry is progressively adopting a design and fabrication environment adapted from the semiconductor industry (e.g. design tools such as EDAs and automated test) [70, 71]. Naturally, test and packaging are intrinsically linked to this design flow and suitable Packaging Design Rules (PDR) have to be applied by PIC designers to ensure proper test and packaging of the PICs during the manufacturing phase. Assembly equipment are also evolving to cope with emerging requirements in terms of automation and throughput. The development of this full comprehensive ecosystem is essential to ensure better statistical process control, scalability, and reliability of future products [72].

1.5.1 Design Rules for Packaging and Test

As mentioned earlier in this chapter, to ensure a robust packaging of PICs, several different design steps which might seem to be fairly independent and sequential such as optical layout design, electrical connectivity, high-frequency modeling, thermal, or mechanical constraints will have to be considered simultaneously, and this requires the development of PDR up front at the PIC design point. Optoelectronic integration is a crucial part of any complete device and its development

can strongly affect the overall performance and price of both the product as of its development.

The first step is to decide upon the type of packaging which suits the most the application whether is prototyping, low-volume, or high-volume intended. The final approach can be the "Golden Box" or "PIC-on-board" (refer to Section 1.2.6) with the following topics, having crucial impacts on the PIC dimensions and layout, to be addressed

RF interconnects: the whole design of the PIC and package should be driven by the targeted maximum operation frequency and the acceptable crosstalk. Standard gold box packages (typically using Kovar cases with ceramic feedthrough) can host up to four RF inputs/outputs up to 40 GHz and multiple optical ports connected to the package through a fiber array, possibly providing hermeticity. Nonstandard configurations have higher cost and longer lead time, as there might be components that will have to be ordered or might require parts to be designed and simulated first. RF interconnects from the package to the PIC are generally managed by using ribbon bonding, whose length should be kept as short as possible to limit RF losses and extra parasitics due to the wire inductance, which are causing signal integrity deterioration. For PIC-on-board, RF lines have to be properly designed to carry the signal in and out of the PIC, and possibly on the PIC itself to connect the active devices (e.g. modulators). The most common configurations used for PICs are the microstrip lines or the coplanar waveguides either standard or differential. One additional important aspect which should be taken into account is the impedance matching between the connectors on the package and the high-speed transmission lines on the PIC. In case the HF specifications of the PIC do not match the ones of the package, special techniques involving impedance transformers must be applied at PIC level.

DC Interconnects: when it comes to the PIC layout, typically the electrical and optical I/Os are not allowed to be placed on the same side of the chips and most of the time there is a limitation even for the DC and HF ports which are normally placed on different sides of the PICs. There is usually a maximum size of the optical chips that can be accommodated in this kind of package. The count of electrical I/Os is limited and their location is controlled with a specific pitch. The pads of the DC connections must have a certain minimum size which is typically in the range of 80×80 μm to allow reliable wire bonding from the PIC to the package. Other limitations may apply to minimize the wire-bonding risks (such as short-circuiting, risk of bond or wire breaking over module life) which are among others a well-defined pad metallization, maximum length of the wire, maximum height, diameter of the wire or even lateral offset between the pads on the PIC and the package.

Thermal management: in gold box approaches, the thermal management of the PIC is ensured by the integration of TEC and NTC thermistors within the box. For PIC-on-board approach, heat dissipation is typically managed by using a high-conductive socket underneath the PIC. If an EIC is flip-chipped on the PIC, an additional finned heat sink will be applied on the backside of the EIC and attached with a high thermal conductive silver-filled epoxy.

Optical interconnect: several aspects should be taken into account when it comes to the design rules. Firstly, if the PIC has multiple channels, the pitch of the optical I/Os must be matching the standard pitch of the FA, 127, 250 or 500 μm being the most common values for the pitch between the optical ports. Then, the coupling configuration (edge coupling or VGC) have to be chosen by taking into account the following considerations

- Number of parallel optical I/O.
- Maximum acceptable level of optical feedback.
- Polarization sensitivity.

1.5.1.1 3D Packaging

Nowadays, one of the most popular packaging solutions is the advanced 3D approach, usually based on a Si or Glass interposer. The PIC can be either embedded within the interposer or it can be assembled together with other add-ons such as control electronics, drivers, or TIAs on both sides of the interposer. The connectivity between the two sides of the interposer can be provided via high-speed TSVs/TGVs and the entire electrical signal routing can be done through several RDL layers on both sides of the Interposer. Finally, the entire 3D assembly is mounted via high-count BGAs on a conventional PCB. Figure 1.40 shows such 3D packaging approach, where the PIC is embedded within the Si interposer [67].

3D assembly technology uses very short interconnects (bumps) which can achieve good impedance matching to the transmission lines on the PICs and offer much denser number of interconnects per unit of size when compared to the wire-bonding suitable PICs. The unwanted parasitics and cross talks between the channels can be minimized by employing special techniques such as underfiller between PIC and PCB. Moreover, the 3D assembly suitable PICs are typically based on an interposer which can be either Si or glass which employs TSV or TGV technologies, respectively, as high-speed interconnects between the top and bottom sides of the Interposer. On the downside, there are several challenges introduced by the 3D assembly technology such as chemical fluxes and solvents required for assembly that might

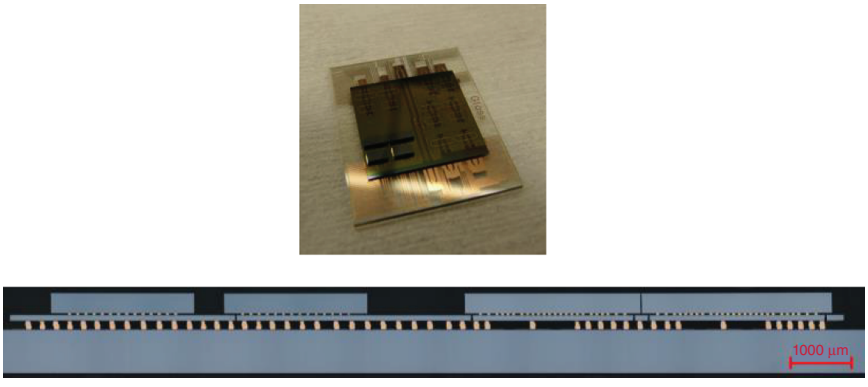


Figure 1.40 3D package developed within the EU-founded PhoxTrot project. Source: B. Sirbu/Fraunhofer IZM.

contaminate the optical interfaces of the PIC. These substances might cause adhesion problems between the PIC and the fiber optics, reducing the yield and long-term stability of the package. Another potential problem of the 3D stacking of components is caused by the high-dissipated power in the electronics that might affect thermally the PIC which is placed in the immediate proximity and cause unwanted effects that lead to the degradation of the PIC performances. Special techniques can be considered here for thermal management involving heat sinks, thermal "vias" between the PIC and electronic-IC or TEC integration within the package, but they only increase the complexity and they might add additional stress to the package.

1.5.1.2 Design Rules for Testing

Automation of PIC testing needs some Design Rules to be observed to ease efficient and fast testing of the devices at the wafer level. [70–73] mention some of these design rules, which have to be taken into account at the early stage of design, in accordance with other PDR, for example by using specific EDA layers in the used Circuit design software, defining test scripts, etc. Some structures have to be set, regarding die orientation, and placement of optical and electronic ports, leading to the implementation of PIC templates in design software tools. For example, depending on the optical probe test used for wafer-level test (bare fiber, fiber array), a keep-out-zone should be set in the PIC design, with no electrical pads designed within the zone, which could lead to mechanical mismatch during testing. Usage of RF probes should also be considered through keep-out zone to enable simultaneous electrical–optical test. Some simple design rules can also ease automated tests, e.g. avoid any rotation of the wafer during test by aligning pads or optical ports with the same orientation, constant pitches, and so on…

All the aforementioned design rules are currently being standardized, for example through initiatives such as the PIXAPP project [71].

1.5.2 Advanced Techniques for Wafer-level Test

Regarding wafer-level test, some enhancements have been recently proposed [73] to improve the acquisition time of E/O measurement of test structures at the wafer level is the use of massive parallelization combined to the massive use of electrical measurement. In this approach, built-in photodetectors are processed within the tested structures. It is fair to assume that these photodetectors will exhibit the same characteristics in terms of spectral response and photocurrent. Using this approach, the test structure area will be dramatically reduced, and the optical acquisition system will be replaced by a parallel acquisition electrical system, which is a very standard and low-cost solution. Another advantage of this technique is also the capability to add integrated monitoring photodiodes to measure the coupled input power, just after the input port (e.g. by using a 90/10 taper coupler). By doing so, it is possible to normalize the measured signal, making it insensitive to any external perturbation. Figure 1.41 shows an implementation of this test solution, using a commercial multiprobe. A small PCB is directly plugged on top of the probe. This PCB embeds

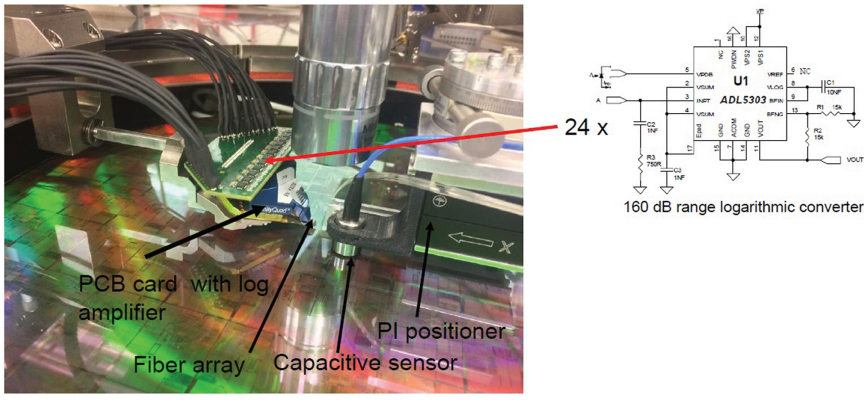


Figure 1.41 PIC under test using built-in photodetector strategy with a specific probe. Source: P. Grosse, CEA-Leti.

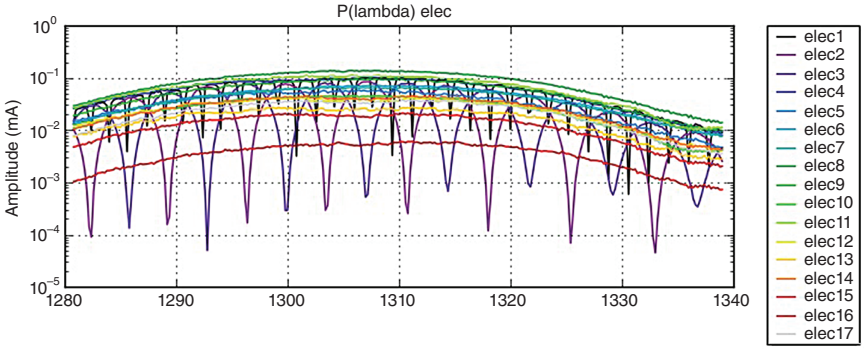


Figure 1.42 Current measured at the output of various devices, embedded in a test cell. Source: P. Grosse, CEA-Leti.

25 high dynamic TIA. These TIA convert the photodiode currents using a logarithmic compression scheme. Currents ranging from 10 pA to 1 mA can be measured. The 25 voltage values are then measured with a 32-channel ADC card triggered by a wavelength analyzer.

Figure 1.42 shows a measurement obtained on a test cell. Several devices like reference waveguides, bends, DC couplers, and microring resonators (MRRs) are tested in the same time. The obtained measurements are very clean and smooth, with a very high measurement dynamic range. 17 channels have been measured simultaneously: this kind of test method is very promising for in-line testing – in clean room environment, using a single input fiber to perform measurement of monitoring cell to characterize the quality and repeatability of the fabrication process.

1.5.3 Recent Achievements and Future Aspects in Assembly Machines

For several applications, photonics micro-assembly technology is currently undergoing a transition to a "microchip" approach, much as that experienced by the

electronics industry some four decades ago. Multiple functionality and components are integrated onto a single chip or a small hybrid chip assembly utilizing PICs. Instead of modules aiming at an overall production quantity of 100–1000 seconds, PIC approaches are designed for numbers in the 100 000 seconds and millions. This in turn means the adoption of wafer level or at least in-line processes, both in assembly and in testing, and where equipment amortization is no longer measured via initial capital investment, but in cost/part.

The ongoing machine design strategy enables an in-line, high-volume automated approach to photonics assembly and testing. Another very important aspect is the flexibility of the assembly line systems. With the increasing need for shorter and shorter time to market as well as with the need to adapt the assembly processes to constantly changing products, a flexible machine design is a key aspect. In case of an assembly line, this can be taken care of by an arrangement of standard machines, which only need to be slightly modified to the specific product as well as standard interfaces for workholders and part handling tools which can be easily adapted to new products.

For this high-volume manufacturing, we are seeing three different approaches.

- **Separate machines with a cassette-to-cassette capability**
  These are standalone machines which in addition to the assembly cell have an input and output feeding system allowing for a much longer automated machine operation without the necessity of an operator changing components regularly. A conveyor mechanism is transporting the components from the input feeding system into the assembly area in the center machine and, after the assembly, to the output feeding system (see left side of Figure 1.43).
- **Single machines with multiple stations**
  By reducing the footprint of the individual assembly stations and using one common feeding system (e.g. a robot as shown in the concept in the right side of in Figure 1.43) multiple stations can be included next to each other into one assembly machine. This approach is increasing the number of assembly stations per machine footprint, hence increasing the overall throughput of the assembly machine.
- **In-line systems**
  In in-line systems, multiple machines are combined and connected via a conveyor system. By this approach, the different functionalities required to build a product like sorting, passive and active assembly steps, gluing, soldering, and marking can be done in separated machines which are optimized for the specific process step. This increases the throughput and precision of the overall assembly while still allowing for complicated multisteps assemblies to be done completely independent of any operator. Figure 1.44 shows a complex assembly line from ficonTEC which was developed for the fully automated photonic sensor production and consists of a total of 16 individual stations, combining multiple tray loading systems, complex passive and active assembly steps end of line test, laser marking, and blister loader.

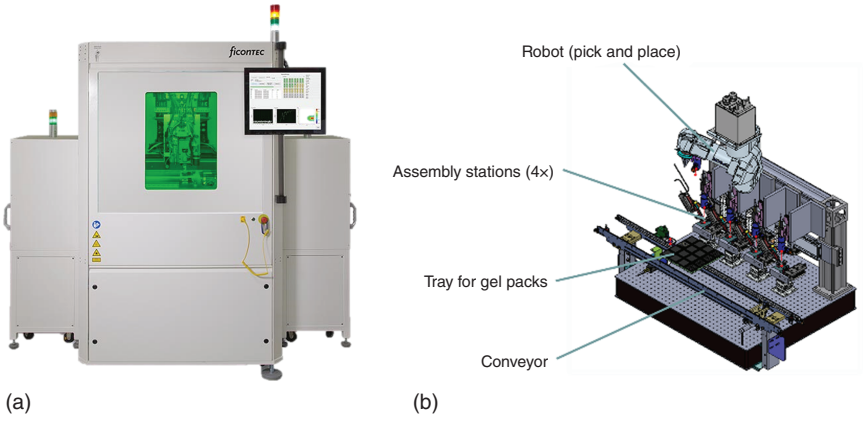
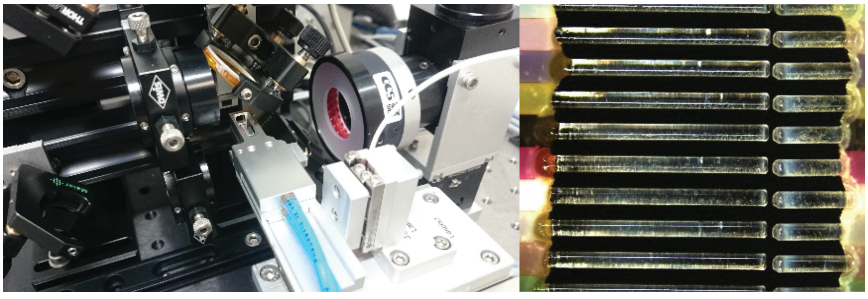


Figure 1.43 (a) ficonTEC Fiber attach station with input and output feeders. (b) A high-volume concept with four multiple assembly stations within one assembly machine. For the pick and place of the components onto the assembly stations one common robot is used. Source: M. Seyfried/ficonTEC.

Figure 1.44 FiconTEC fully automated inline configuration for a photonics sensor production. Source: M. Seyfried/ficonTEC.

To allow for such a completely automated assembly process flow producing autonomously over a long period of time multiple different steps must be fully automized. Besides the obvious transportation of modules and components into the assembly machine and out of it also steps like e.g. the connection of fiber plugs to telecommunication modules before starting active alignment must also be automated. For exactly this purpose so-called auto-fiber connectors have been developed consisting of a complex system of pneumatic sliders, clamps, and actuators allowing a process driven highly repeatable coupling of optical single-mode connectors. In the meantime, such systems exist for a variety of connectors ranging from classical MPO connectors to the recently developed SN connectors and are field proven in industrial assembly machines. A further increase in automation is expected to be available when complete fiber preparation systems can be included directly into assembly machines. Recent R&D activities have paved the way toward automated CO_2-based fiber strip and cleave systems which are now available for a full integration into assembly and packaging machines. Figure 1.45 shows the lab demonstrator as well as the first results achieved within the Lasclad project which are transferred into a fully autonomous CO_2-based fiber ribbon strip and cleave unit allowing the usage of fibers directly from the roll within an assembly machine. Such



(a) (b)

Figure 1.45 (a) development setup of the fiber strip and cleave system with the fiber in the center of the image below the 45° optics, (b) fiber array after strip and cleave. Source: M. Seyfried/ficonTEC.

systems are highly favorable as they increase the level of automation and reduce the problems with contaminations on the fibers when being brought into the assembly machine via external systems. This fiber preparation technique is a key element for the passive V-groove assembly strategies discussed in Section 1.3.3.

Whereas the abovementioned techniques mainly focus on increasing the automation level of assembly equipment, completely new alignment and assembly approaches are also developed in parallel. These methods may be including faster alignments but also fixation techniques of chips and fibers to the modules. For the latter one, a new and epoxy-free solution is developed within the PICWeld project by Fraunhofer IZM. In this approach, a polarization-maintaining optical fiber is aligned to the edge of a glass-based waveguide structure in four degrees of freedom. Instead of using UV-curable epoxy for the fixation, a glass welding process is implemented. The benefits of such a technique are multifold and expand from faster fixation times to higher reliability and the avoidance of epoxy outgassing.

An already well-established fixation technique in PIC packaging is solder joints. The most common system is the eutectic AuSn solder with a melting temperature of around 280 °C. For mass manufacturing often pre-deposited solder is used reducing the complexity during assembly. For means of high throughput and localized soldering laser-based heating systems are offered for years from companies such as ASMPT Amicra. The typical wavelengths used in such laser soldering systems lie in the 950–980 nm range where cost-efficient powerful diode lasers are available as heat sources. These lasers are, however, absorbed within the first few micrometers of the silicon. From this point on the heat distributes into all directions within the device. More sophisticated approaches use longer laser wavelength in the near-infrared from 1064 to 1500 nm for which the absorption in silicon is strongly reduced. Depending on the exact wavelength the absorption happens either within the silicon material or even only at the opposite side of the silicon substrate within special absorption layers. By carefully choosing the laser wavelength the absorption area can be tailored to the specific customer needs and is allowing to significantly reduce the heat-affected zone. This allows a much closer assembly of dies on one common substrate or close to heat-sensible elements (Figure 1.46).

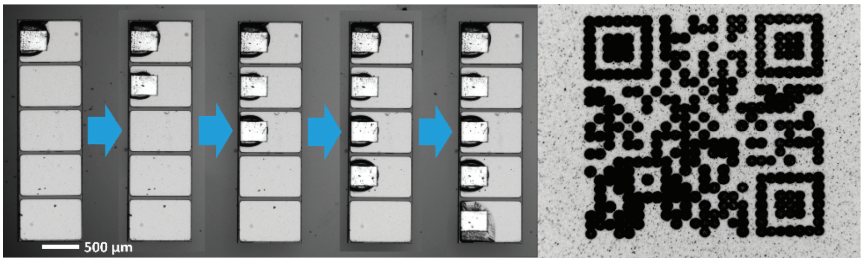


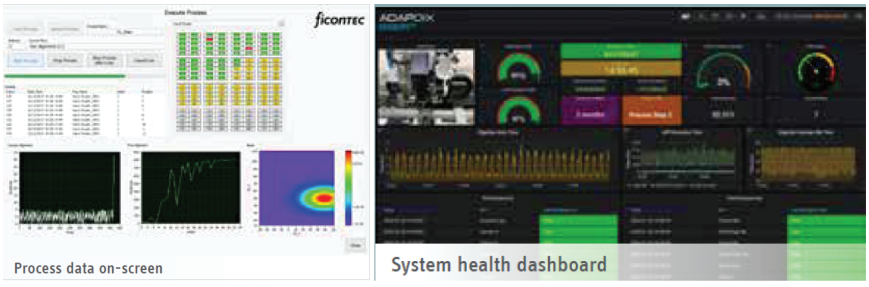
Figure 1.46 Through silicon laser soldering experiments performed within the Larebo project. (a) successively population of laser diodes on one common silicon substrate with different solder pads (b) different solder spots of roughly 200 µm diameter in one homogeneous AuSn layer. Source: M. Seyfried/ficonTEC.

With respect to innovative alignment techniques, the exploitation of the infrared wavelength region is very promising for the mainly silicon-based PICs. As mentioned earlier in this chapter one of the main challenges for flip-chip processes is the reference marks not being visible with standard illumination techniques once the components are placed on top of each other. Therefore, no closed-loop alignment, which is allowing the highest accuracy, can be performed in the visible spectral range.

However, when shifting the illumination wavelength into the near-infrared spectral region one can exploit the dramatically reduced absorbance of silicon which is allowing to detect structures and reference marks on the backside of the PICs (see pictures in Section 1.3.2). This technique, being common for post-alignment inspection, can also be used for a vision-based closed-loop alignment of two chips with respect to each other. Exploiting sophisticated sub-pixel vision alignment routines step sizes as small as 100 nm has been detected repeatably leading to the first successful build of customer modules. This technique of IR alignment becomes even more interesting when being combined with the aforementioned laser soldering approach establishing an assembly system ideally suited for wafer-level assemblies. First commercial assembly machines based on this technique are shipped to leading customers worldwide.

Whereas the hardware of an assembly machine is the most visible part, the importance of the underlying software and assembly processes will become more and more important in future. The software must orchestrate and is the connecting element between all hardware components making the assembly system more than just the sum of the individual components. When aiming for assembly machines for mass manufacturing applications also the software must be set up in a way to allow an easy and reliable process adaption to the different challenges compared to stand-alone systems.

Different machines which are connected to in-line system or individual assembly stations in one machine need to exchange information about their production state



(a) (b)

Figure 1.47 (a) ficonTEC Software screenshot, (b) System-health monitoring system from Adapdix. Source: M. Seyfried/ficonTEC.

with each other or a higher line control system as well as different databases. Only this structure is allowing full traceability of the assembled or tested components. This traceability needs to be enabled from the individual component level as well as the subassembly (Figure 1.47).

In each assembly and testing machine a numerous amount of data from different data sources like axes positions and errors, pressure of pneumatic and vacuum levels, alignment power, and cycle times is available which can easily be stored in a database. However, up to now, there is barely any use of all this data for machine and process improvements like yield and cycle time increment. Companies like Adapdix are entering this field and are making use of all the sensor data to feed underlying self-learning models to supervise and in situ improve the machine performance. This capability will not only allow to dramatically increase the machine and process performance but will also be extremely helpful for preventive maintenance measures of the machines and reduction of the machine downtime. Permanent monitoring and evaluation of data coming from all sensors, motion systems, and the products during assembly will enable the machine to learn and adapt to, e.g. incoming part variation.

1.6 Conclusion

With the current widespreading of PIC-based modules, notably in datacenter interconnects, optoelectronic module packaging is facing a change in the assembly paradigm, to cope with increasing manufacturing volumes and expected reduced costs. Advanced technologies for optical coupling are now considered, such as electronic/photonic convergence strategies, through 3D packaging. This evolution also comes with a renewed environment in terms of design procedures, equipment automation for assembly and test, contributing to increased throughput and reliability. This development may pave the way to the adoption of PICs in many new applications, especially thanks to the emergence of two new concepts: photonic chiplets and photonic interposers.

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